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# FCD380N60E

## N-Channel SuperFET® II Easy-Drive MOSFET

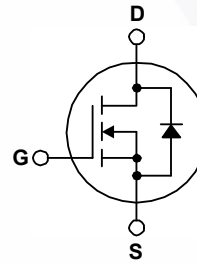
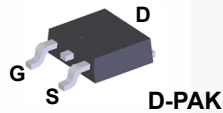
600 V, 10.2 A, 380 mΩ

### Features

- 650 V @  $T_J = 150^\circ\text{C}$
- Typ.  $R_{DS(on)} = 320\text{ m}\Omega$
- Ultra Low Gate Charge (Typ.  $Q_g = 34\text{ nC}$ )
- Low Effective Output Capacitance (Typ.  $C_{oss(eff.)} = 97\text{ pF}$ )
- 100% Avalanche Tested
- An Integrated Gate Resistor
- RoHS Compliant

### Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance,  $dv/dt$  rate and higher avalanche energy. Consequently, SuperFET II MOSFET easy-drive series offers slightly slower rise and fall times compared to the SuperFET II MOSFET series. Noted by the "E" part number suffix, this family helps manage EMI issues and allows for easier design implementation. For faster switching in applications where switching losses must be at an absolute minimum, please consider the SuperFET II MOSFET series.



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FCD380N60E	Unit
$V_{DSS}$	Drain to Source Voltage	600	V
$V_{GSS}$	Gate to Source Voltage	- DC	$\pm 20$
		- AC ( $f > 1\text{ Hz}$ )	$\pm 30$
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	10.2
		- Continuous ( $T_C = 100^\circ\text{C}$ )	6.4
$I_{DM}$	Drain Current	- Pulsed (Note 1)	30.6
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	211.6
$I_{AR}$	Avalanche Current	(Note 1)	2.3
$E_{AR}$	Repetitive Avalanche Energy	(Note 1)	1.06
$dv/dt$	MOSFET $dv/dt$	100	V/ns
	Peak Diode Recovery $dv/dt$	(Note 3)	
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	106
		- Derate Above $25^\circ\text{C}$	0.85
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FCD380N60E	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.18	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	100	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCD380N60E	FCD380N60E	DPAK	Tape and Reel	330 mm	16 mm	2500 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 10\text{ mA}, T_J = 25^\circ\text{C}$	600	-	-	V
		$V_{GS} = 0\text{ V}, I_D = 10\text{ mA}, T_J = 150^\circ\text{C}$	650	-	-	
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$ , Referenced to $25^\circ\text{C}$	-	0.67	-	$\text{V}/^\circ\text{C}$
$BV_{DS}$	Drain to Source Avalanche Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 10\text{ A}$	-	700	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}$	-	-	5	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	-	-	20	
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	2.5	-	3.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 5\text{ A}$	-	0.32	0.38	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 5\text{ A}$	-	10	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	1330	1770	pF
$C_{oss}$	Output Capacitance		-	945	1260	pF
$C_{rss}$	Reverse Transfer Capacitance		-	60	90	pF
$C_{oss}$	Output Capacitance	$V_{DS} = 380\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	25	-	pF
$C_{oss(eff.)}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$	-	97	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 380\text{ V}, I_D = 5\text{ A}, V_{GS} = 10\text{ V}$	-	34	45	nC
$Q_{gs}$	Gate to Source Gate Charge		-	5.3	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		(Note 4)	-	13	-
ESR	Equivalent Series Resistance	$f = 1\text{ MHz}$	-	6	-	$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 380\text{ V}, I_D = 5\text{ A}, V_{GS} = 10\text{ V}, R_G = 4.7\ \Omega$	-	17	44	ns
$t_r$	Turn-On Rise Time		-	9	28	ns
$t_{d(off)}$	Turn-Off Delay Time		-	64	138	ns
$t_f$	Turn-Off Fall Time		(Note 4)	-	10	30

### Drain-Source Diode Characteristics

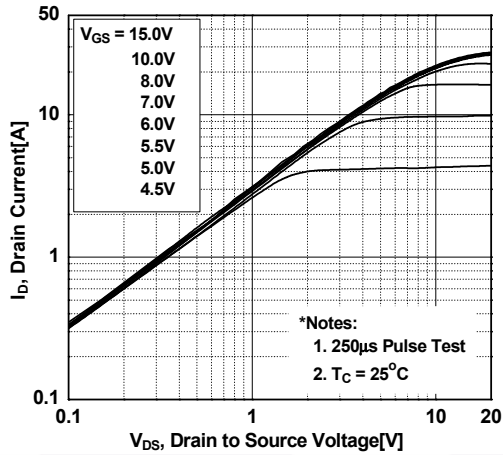
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	10.2	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	30.6	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 5\text{ A}$	-	-	1.2	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 5\text{ A}, di_F/dt = 100\text{ A}/\mu\text{s}$	-	240	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	3	-	$\mu\text{C}$

#### Notes:

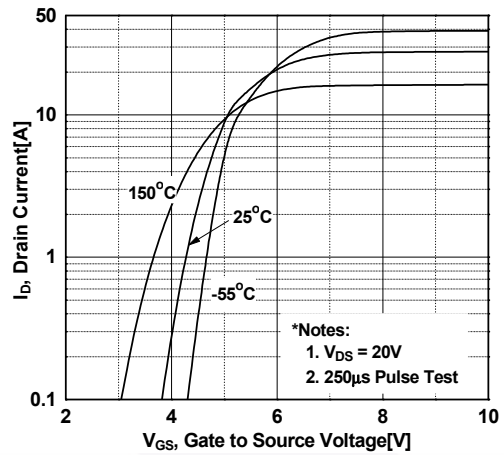
1. Repetitive rating; pulse-width limited by maximum junction temperature.
2.  $I_{AS} = 2.3\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 5.1\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

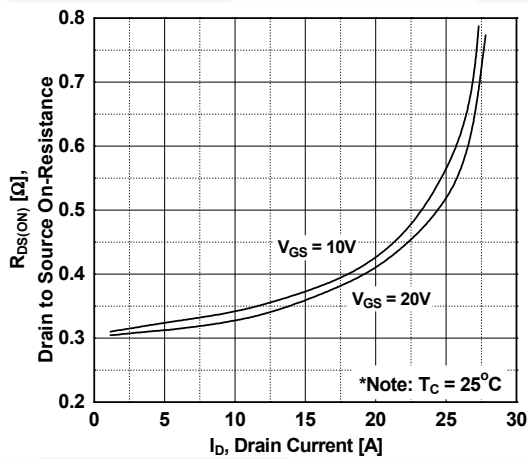
**Figure 1. On-Region Characteristics**



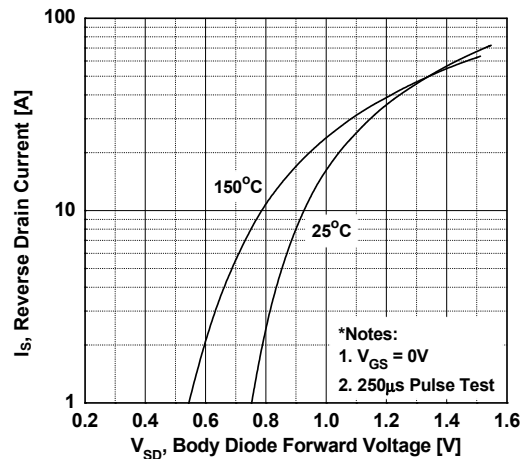
**Figure 2. Transfer Characteristics**



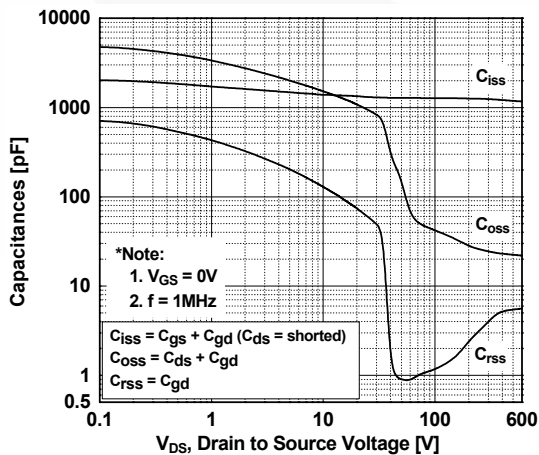
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



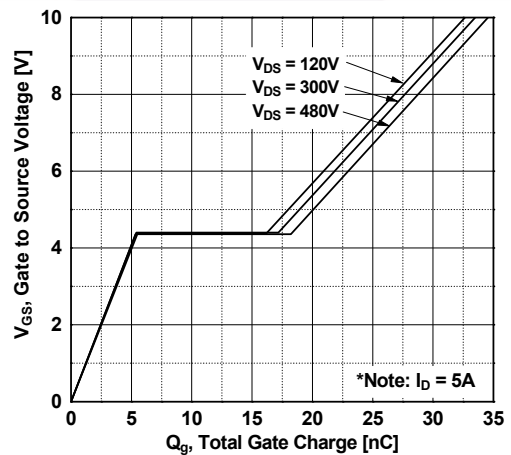
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

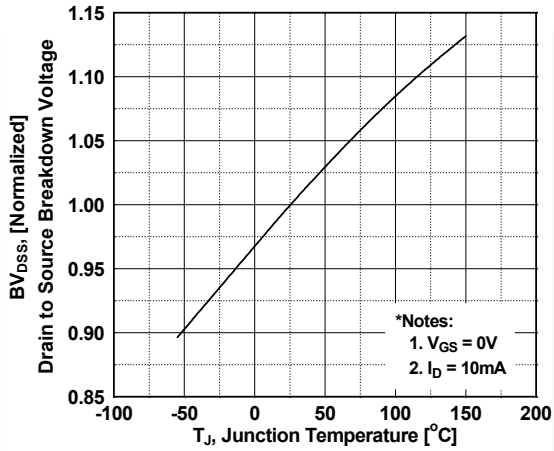


**Figure 6. Gate Charge Characteristics**

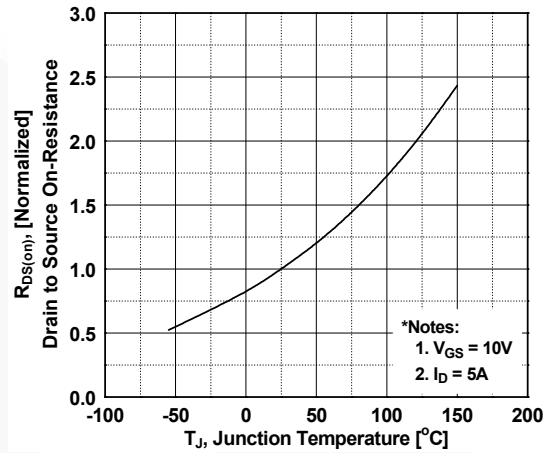


**Typical Performance Characteristics** (Continued)

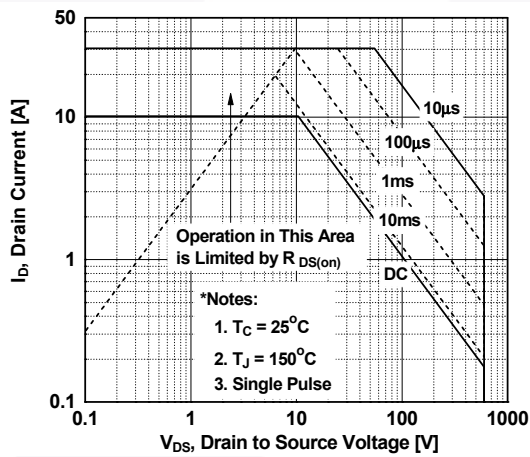
**Figure 7. Breakdown Voltage Variation vs. Temperature**



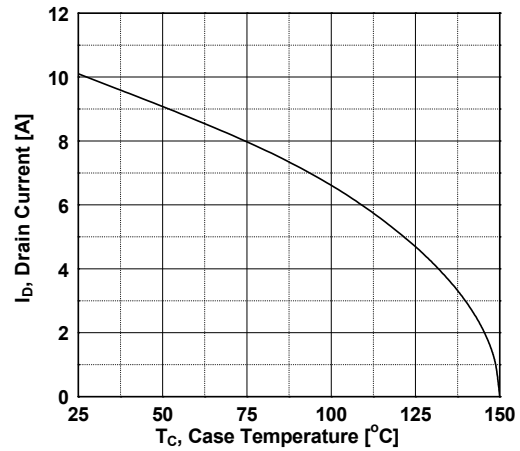
**Figure 8. On-Resistance Variation vs. Temperature**



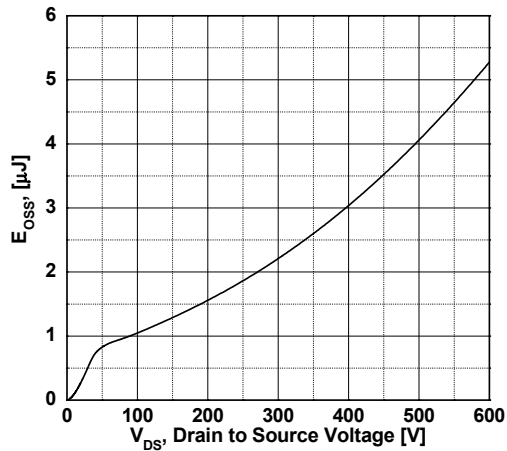
**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**

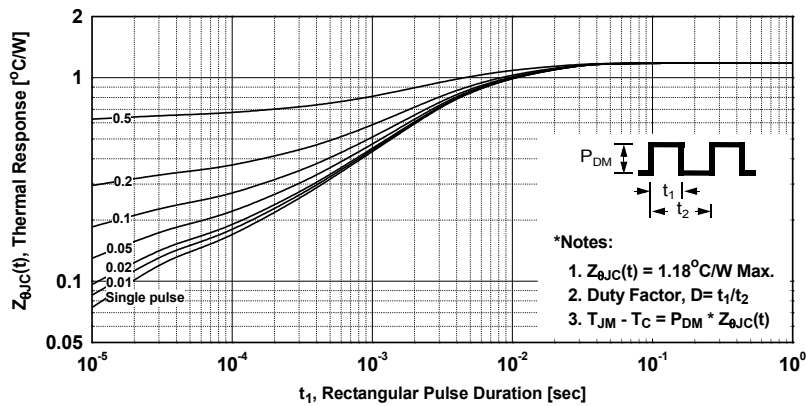


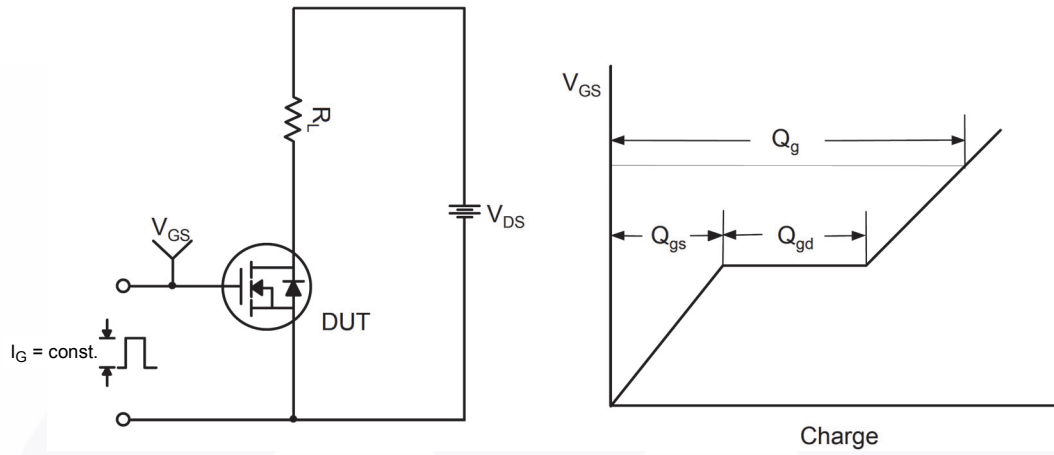
**Figure 11. E\_oss vs. Drain to Source Voltage**



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve





**Figure 13. Gate Charge Test Circuit & Waveform**



**Figure 14. Resistive Switching Test Circuit & Waveforms**



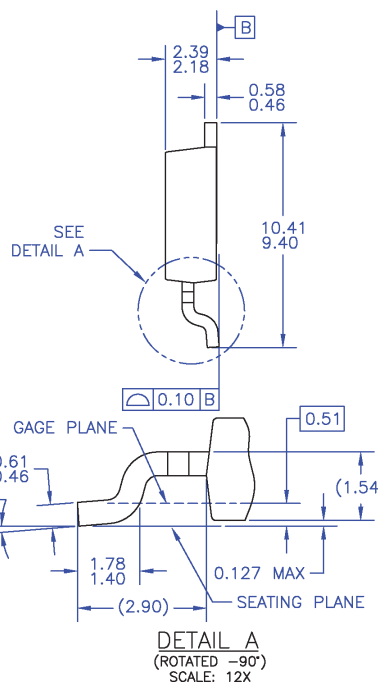
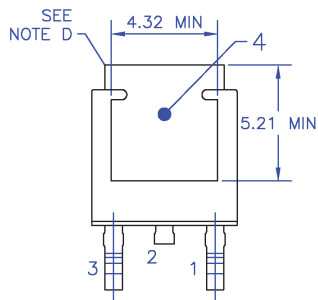
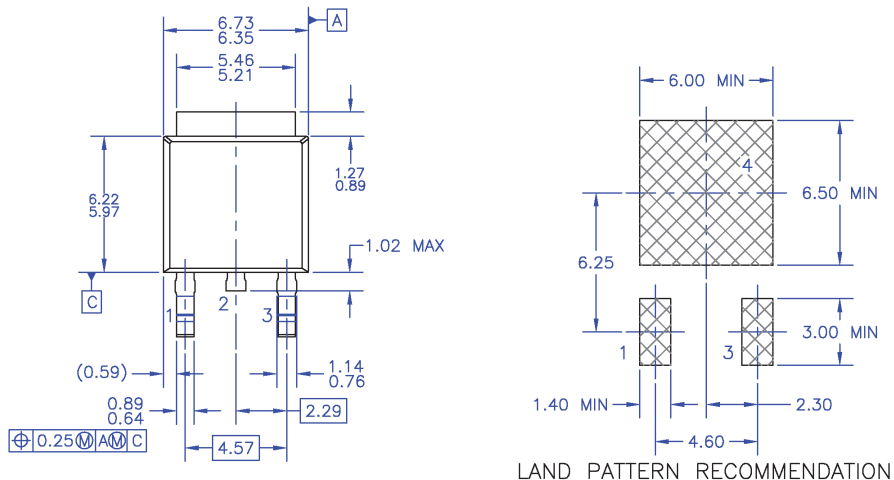
**Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms**



Figure 16. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms



## Mechanical Dimensions



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
  - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
  - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
  - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC351A STD TO220P1003X238-3N.
  - H) DRAWING NUMBER AND REVISION: MKT-T0252A03REV8

**Figure 17. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB**

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| Fairchild Semiconductor® | SPM®                    | SupersOT™-3                                     | UniFET™          |
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| FACT®                    | SPM®                    | SupersOT™-8                                     | VisualMax™       |
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