1 MSPS, Ultralow Power, 12-Bit ADC in 8-Lead LFCSP

Data Sheet **AD7091**

FEATURES

- Fast throughput rate of 1 MSPS
- Specified for V_{DD} of 2.09 V to 5.25 V
- INL of ±1 LSB maximum
- Analog input range of 0 V to V_{DD}
- Ultralow power
  - 367 µA typical at 3 V and 1 MSPS
  - 324 nA typical at 3 V in power-down mode
- Reference provided by V_{DD}
- Flexible power/throughput rate management
- High speed serial interface: SPI®-/QSPI™-/MICROWIRE®-/DSP-compatible
- Busy indicator
- Power-down mode
- 8-lead, 2 mm × 2 mm LFCSP package
- Temperature range: −40°C to +125°C

APPLICATIONS

- Battery-powered systems
  - Handheld meters
  - Medical instruments
  - Mobile communications
- Instrumentation and control systems
- Data acquisition systems
- Optical sensors
- Diagnostic/monitoring functions
- Energy harvesting

FUNCTIONAL BLOCK DIAGRAM

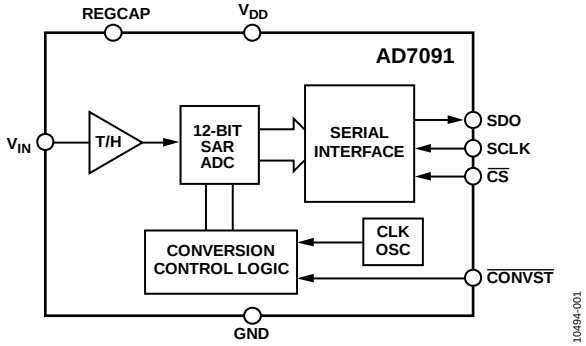

Figure 1.

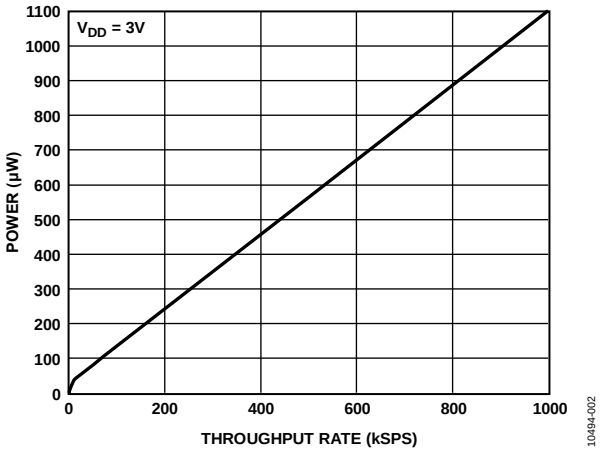

Figure 2. Power Dissipation vs. Throughput Rate

GENERAL DESCRIPTION

The AD7091 is a 12-bit successive approximation register analog-to-digital converter (SAR ADC) that offers ultralow power consumption (typically 367 µA at 3 V and 1 MSPS) while achieving fast throughput rates (1 MSPS with a 50 MHz SCLK). The AD7091 operates from a single 2.09 V to 5.25 V power supply. The AD7091 also features an on-chip conversion clock and a high speed serial interface.

The conversion process and data acquisition are controlled using a $\overline{\text{CONVST}}$ signal and an internal oscillator. The AD7091 has a serial interface that allows data to be read after the conversion while achieving a 1 MSPS throughput rate. The AD7091 uses advanced design and process techniques to achieve very low power dissipation at high throughput rates.

The reference is derived internally from V_{DD}. This design allows the widest dynamic input range to the ADC; that is, the analog input range for the AD7091 is from 0 V to V_{DD}.

PRODUCT HIGHLIGHTS

1. Lowest Power 12-Bit SAR ADC Available.
2. High Throughput Rate with Ultralow Power Consumption.
3. Flexible Power/Throughput Rate Management.
   Average power scales with the throughput rate. Power-down mode allows the average power consumption to be reduced when the device is not performing a conversion.
4. Reference Derived from the Power Supply.
5. Single-Supply Operation.

Rev. B
Document Feedback

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10/12—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.09 V to 5.25 V, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 50 MHz, T_A = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE[1]	f_{IN} = 10 kHz sine wave				
Signal-to-Noise Ratio (SNR)[2]	V_{DD} < 2.7 V		68		dB
	V_{DD} ≥ 2.7 V	67	69		dB
Signal-to-Noise-and-Distortion Ratio (SINAD)[2]		66.3	68		dB
Total Harmonic Distortion (THD)[2]			−86	−74	dB
Spurious-Free Dynamic Range (SFDR)[2]			−85	−75	dB
Aperture Delay[2]			5		ns
Aperture Jitter[2]			40		ps
Full Power Bandwidth[2]	At −3 dB		1.5		MHz
	At −0.1 dB		1.2		MHz
DC ACCURACY					
Resolution		12			Bits
Integral Nonlinearity (INL)[2]			±0.6	±1	LSB
Differential Nonlinearity (DNL)[2]	Guaranteed no missing codes to 12 bits		±0.3	±0.9	LSB
Offset Error[2]		−8.5	±0.7	+5	LSB
Gain Error[2]			±1.2	±4	LSB
Total Unadjusted Error (TUE)[2]			1.1		LSB
ANALOG INPUT					
Input Voltage Range		0		V_{DD}	V
DC Leakage Current				±1	µA
Input Capacitance[3]	During acquisition phase		7		pF
	Outside acquisition phase		1		pF
LOGIC INPUTS					
Input High Voltage (V_{INH})		0.7 × V_{DD}			V
Input Low Voltage (V_{INL})				0.3 × V_{DD}	V
Input Current (I_{IN})	Typically 10 nA, V_{IN} = 0 V or V_{DD}			±1	µA
Input Capacitance (C_{IN})[3]				5	pF
LOGIC OUTPUTS					
Output High Voltage (V_{OH})	I_{SOURCE} = 200 µA	V_{DD} − 0.2			V
Output Low Voltage (V_{OL})	I_{SINK} = 200 µA			0.4	V
Floating State Leakage Current				±1	µA
Floating State Output Capacitance[3]				5	pF
Output Coding			Straight binary		
CONVERSION RATE					
Conversion Time				650	ns
Track-and-Hold Acquisition Time[2, 3]	Full-scale step input			350	ns
Throughput Rate				1	MSPS
POWER REQUIREMENTS					
V_{DD}		2.09		5.25	V
I_{DD}	V_{IN} = 0 V				
Normal Mode—Static[4]	V_{DD} = 5.25 V		9.3	27	µA
	V_{DD} = 3 V		9.1	28	µA
Normal Mode—Operational	V_{DD} = 5.25 V, f_{SAMPLE} = 1 MSPS		450	554	µA
	V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS		367	442	µA
	V_{DD} = 3 V, f_{SAMPLE} = 100 kSPS		45		µA
Power-Down Mode	V_{DD} = 5.25 V		0.374	8.2	µA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	V_{DD} = 3 V		0.324	8	µA
	V_{DD} = 3 V, T_A = −40°C to +85°C		0.324	1.8	µA
Power Dissipation	V_{IN} = 0 V				
Normal Mode—Static[4]	V_{DD} = 5.25 V		50	142	µW
	V_{DD} = 3 V		27	84	µW
Normal Mode—Operational	V_{DD} = 5.25 V, f_{SAMPLE} = 1 MSPS		2.4	3	mW
	V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS		1.1	1.4	mW
Power-Down Mode	V_{DD} = 5.25 V		2	44	µW
	V_{DD} = 3 V		1	24	µW

[1] Dynamic performance is achieved when SCLK operates in burst mode. Operating a free running SCLK during the acquisition phase degrades dynamic performance.
[2] See the Terminology section.
[3] Sample tested during initial release to ensure compliance.
[4] SCLK is operating in burst mode and $\overline{CS}$ is idling high. With a free running SCLK and $\overline{CS}$ pulled low, the I_{DD} static current is increased by 60 µA typical at V_{DD} = 5.25 V.

TIMING SPECIFICATIONS

V_{DD} = 2.09 V to 5.25 V, T_A = −40°C to +125°C, unless otherwise noted. Signals are specified from 10% to 90% of V_{DD} with a load capacitance of 12 pF on the output pin.[1]

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{SCLK}	50	MHz max	Frequency of serial read clock
t_1	8	ns max	Delay from the end of a conversion until SDO exits the three-state condition
t_2	7	ns max	Data access time after SCLK falling edge
t_3	0.4 t_{SCLK}	ns min	SCLK high pulse width
t_4	3	ns min	SCLK to data valid hold time
t_5	0.4 t_{SCLK}	ns min	SCLK low pulse width
t_6	15	ns max	SCLK falling edge to SDO high impedance
t_7	10	ns min	$\overline{CONVST}$ pulse width
t_8	650	ns max	Conversion time
t_9	6	ns min	$\overline{CS}$ low time before the end of a conversion
t_{10}	18	ns max	Delay from $\overline{CS}$ falling edge until SDO exits the three-state condition
t_{11}	8	ns min	$\overline{CS}$ high time before the end of a conversion
t_{12}	8	ns min	Delay from the end of a conversion until the $\overline{CS}$ falling edge
t_{13}	100	µs max	Power-up time
t_{QUIET}	50	ns min	Time between the last SCLK edge and the next $\overline{CONVST}$ pulse

[1] Sample tested during initial release to ensure compliance.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
ESD	
Human Body Model (HBM)	±2.5 kV
Field-Induced Charged Device Model (FICDM)	±1.5 kV

[1] Transient currents of up to 100 mA do not cause silicon controlled rectifier (SCR) latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead LFCSP	36.67	6.67	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

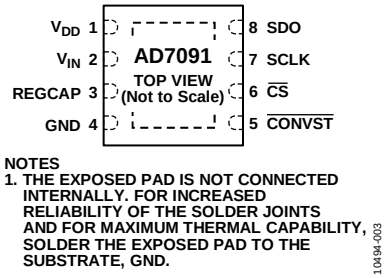

Figure 3.

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Power Supply Input. The V_{DD} range is from 2.09 V to 5.25 V. Decouple this supply pin to GND. Typical recommended capacitor values are 10 µF and 0.1 µF.
2	V_{IN}	Analog Input. The single-ended analog input range is from 0 V to V_{DD}.
3	REGCAP	Decoupling Capacitor Pin for Voltage Output from Internal Low Dropout (LDO) Regulator. Decouple this output pin separately to GND using a 1 µF capacitor. The voltage at this pin is 1.8 V typical.
4	GND	Ground. This pin is the ground reference point for all circuitry on the AD7091. The analog input signal should be referred to this GND voltage.
5	$\overline{\text{CONVST}}$	Conversion Start. Active low, edge triggered logic input. The falling edge of $\overline{\text{CONVST}}$ places the track-and-hold into hold mode and initiates a conversion.
6	$\overline{\text{CS}}$	Chip Select. Active low logic input. The serial bus is enabled when $\overline{\text{CS}}$ is held low; in this mode $\overline{\text{CS}}$ is used to frame the output data on the SPI bus.
7	SCLK	Serial Clock. This pin acts as the serial clock input.
8	SDO	Serial Data Output. The conversion output data is supplied to this pin as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data is provided MSB first.
9	EPAD	Exposed Pad. The exposed pad is not connected internally. For increased reliability of the solder joints and for maximum thermal capability, solder the exposed pad to the substrate, GND.

TYPICAL PERFORMANCE CHARACTERISTICS

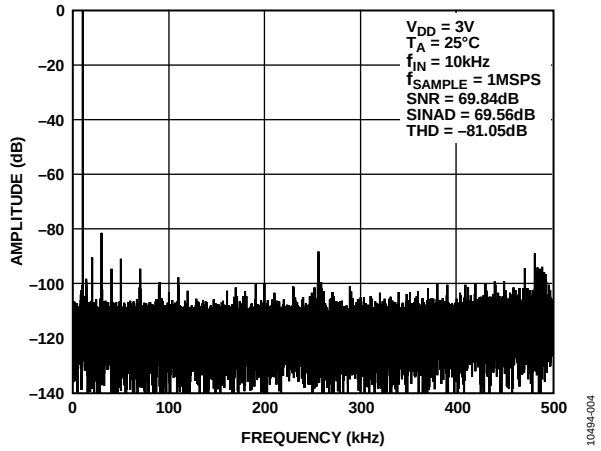

Figure 4. Typical Dynamic Performance

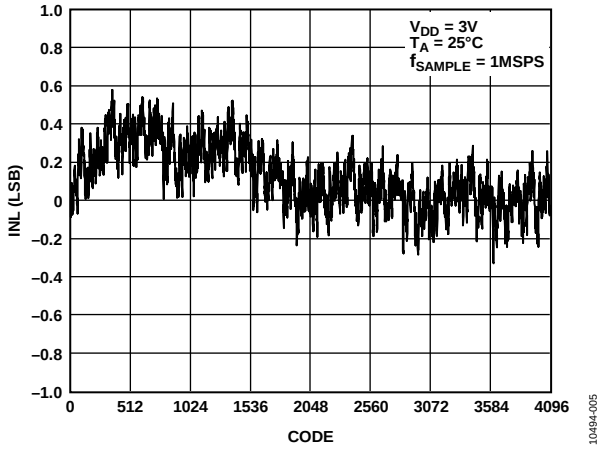

Figure 5. Typical INL Performance

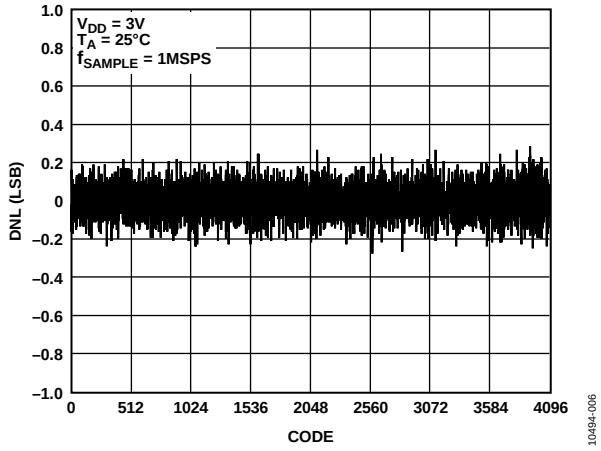

Figure 6. Typical DNL Performance

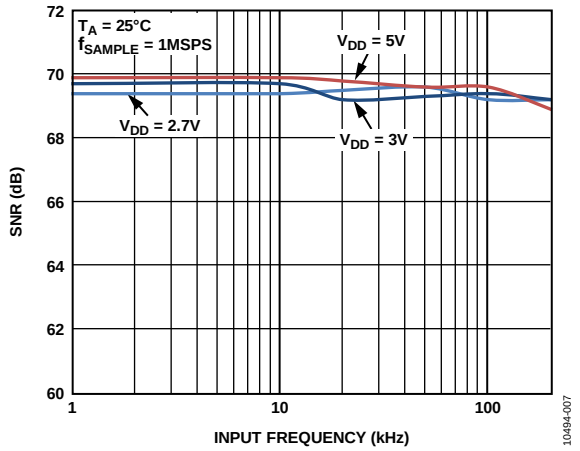

Figure 7. SNR vs. Analog Input Frequency for Various Supply Voltages

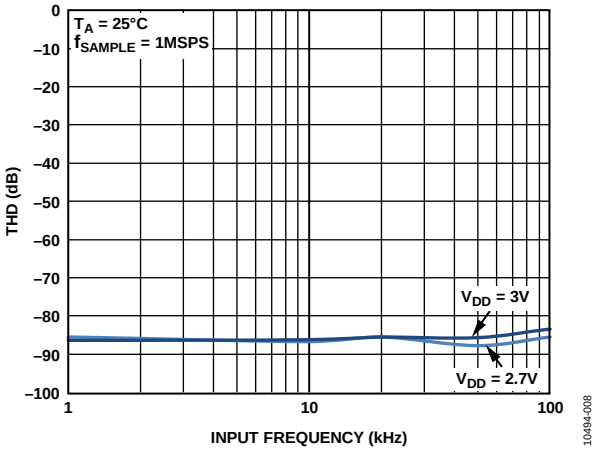

Figure 8. THD vs. Analog Input Frequency for Various Supply Voltages

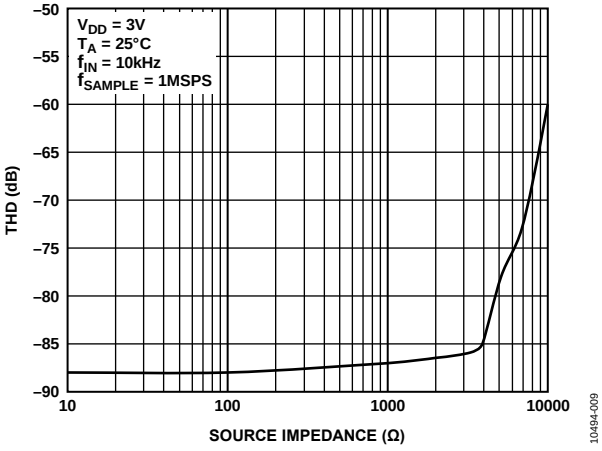

Figure 9. THD vs. Source Impedance

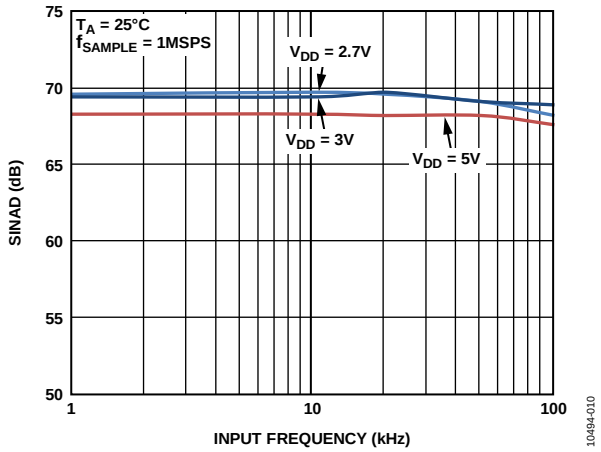

Figure 10. SINAD vs. Analog Input Frequency for Various Supply Voltages

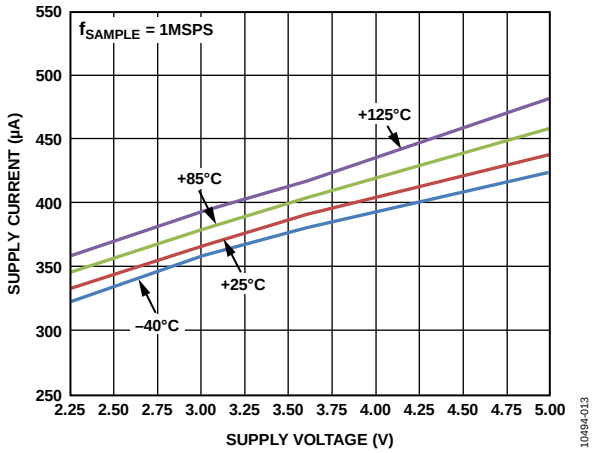

Figure 13. Operational Supply Current vs. Supply Voltage for Various Temperatures

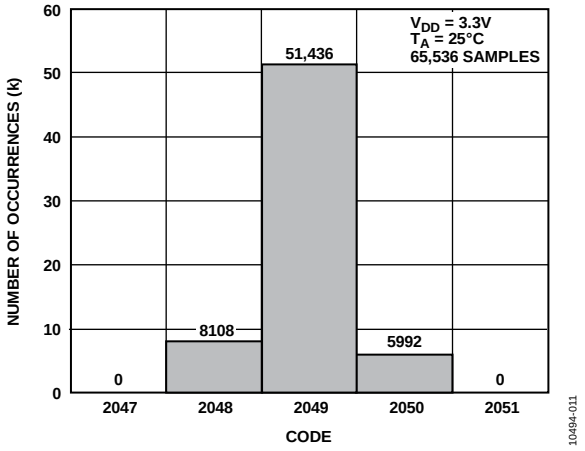

Figure 11. Histogram of Codes at Code Center (V_{DD}/2)

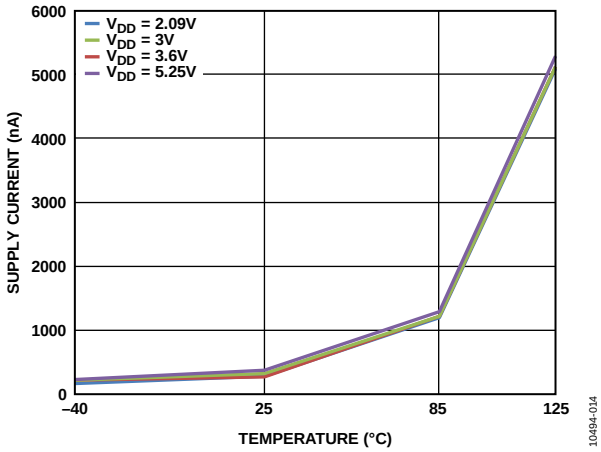

Figure 14. Power-Down Supply Current vs. Temperature for Various Supply Voltages

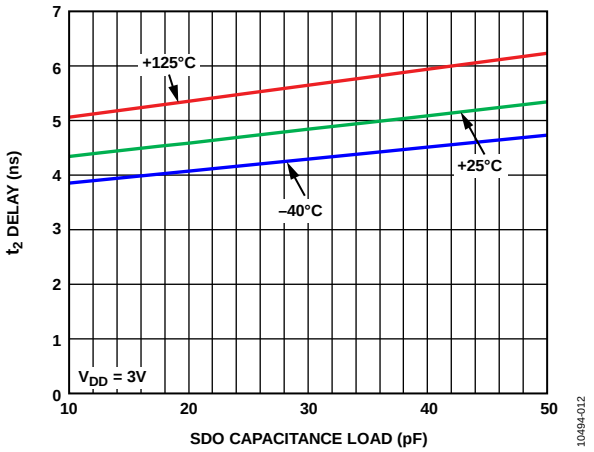

Figure 12. t_2 Delay vs. SDO Capacitance Load, V_{DD} = 3 V

TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. For the AD7091, the endpoints of the transfer function are zero scale (a point 0.5 LSB below the first code transition) and full scale (a point 0.5 LSB above the last code transition).

Differential Nonlinearity (DNL)
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
Offset error is the deviation of the first code transition (00 … 000 to 00 … 001) from the ideal (such as GND + 0.5 LSB).

Gain Error
Gain error is the deviation of the last code transition (111 … 110 to 111 … 111) from the ideal (such as V_{DD} − 1.5 LSB) after the offset error has been adjusted out.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns to track mode after the end of a conversion. The track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±0.5 LSB, after a conversion.

Signal-to-Noise Ratio (SNR)
SNR is the measured ratio of signal to noise at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_{SAMPLE}/2$), excluding dc.

The ratio is dependent on the number of quantization levels in the digitization process: the more levels, the smaller the quantization noise. The theoretical signal-to-noise ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\text{-}to\text{-}Noise\ Ratio = (6.02N + 1.76)\ \text{dB}$$

Therefore, for a 12-bit converter, the SNR is 74 dB.

Signal-to-Noise-and-Distortion Ratio (SINAD)
SINAD is the measured ratio of signal to noise and distortion at the output of the ADC. The signal is the rms value of the sine wave, and noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_{SAMPLE}/2$), including harmonics, but excluding dc.

Total Unadjusted Error (TUE)
TUE is a comprehensive specification that includes the gain, linearity, and offset errors.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7091, THD is defined as

$$THD\ (\text{dB}) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Spurious-Free Dynamic Range (SFDR)
SFDR, also known as peak harmonic or spurious noise, is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_{SAMPLE}/2$ and excluding dc) to the rms value of the fundamental.

Aperture Delay
Aperture delay is the measured interval between the leading edge of the sampling clock and the point at which the ADC samples data.

Aperture Jitter
Aperture jitter is the sample-to-sample variation in the effective point in time at which the data is sampled.

Full Power Bandwidth
Full power bandwidth is the input frequency at which the amplitude of the reconstructed fundamental is reduced by 0.1 dB or 3 dB for a full-scale input.

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7091 is a 12-bit successive approximation register analog-to-digital converter (SAR ADC) that offers ultralow power consumption (typically 367 µA at 3 V and 1 MSPS) while achieving fast throughput rates (1 MSPS with a 50 MHz SCLK). The part operates from a single power supply in the range of 2.09 V to 5.25 V.

The AD7091 provides an on-chip track-and-hold amplifier and an analog-to-digital converter (ADC) with a serial interface housed in a tiny 8-lead LFCSP package. This package offers considerable space-saving advantages compared with alternative solutions. The serial clock input accesses data from the part. The clock for the SAR ADC is generated internally.

The analog input range is 0 V to V_{DD}. An external reference is not required for the ADC, nor is there a reference on chip. The reference voltage for the AD7091 is derived from the power supply and, thus, provides the widest dynamic input range of 0 V to V_{DD}.

The AD7091 also features a power-down option to save power between conversions. The power-down feature is implemented using the standard serial interface, as described in the Modes of Operation section.

CONVERTER OPERATION

The AD7091 is a SAR ADC based around a charge redistribution DAC. Figure 15 and Figure 16 show simplified schematics of the ADC.

Figure 15 shows the ADC during its acquisition phase; SW2 is closed and SW1 is in Position A. The comparator is held in a balanced condition, and the sampling capacitor acquires the signal on V_{IN}.

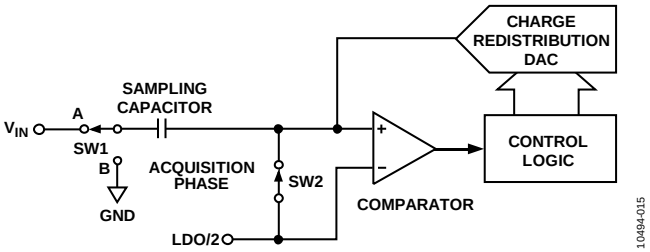

Figure 15. ADC Acquisition Phase

When the ADC starts a conversion, SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced (see Figure 16). The control logic and the charge redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Figure 17 shows the ADC transfer function.

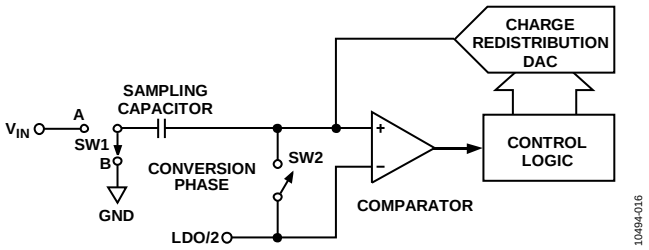

Figure 16. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding of the AD7091 is straight binary. The designed code transitions occur midway between successive integer LSB values, such as 0.5 LSB, 1.5 LSB, and so on. The LSB size for the AD7091 is $V_{DD}/4096$. The ideal transfer characteristic for the AD7091 is shown in Figure 17.

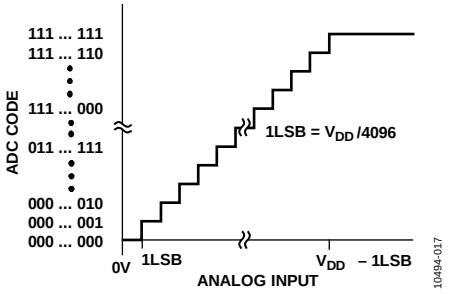

Figure 17. AD7091 Transfer Characteristic

TYPICAL CONNECTION DIAGRAM

Figure 19 shows a typical connection diagram for the AD7091. A positive power supply in the range of 2.09 V to 5.25 V should be connected to the V_{DD} pin. The reference is derived internally from V_{DD} and, for this reason, V_{DD} should be well decoupled to achieve the specified performance; typical values for the decoupling capacitors are 100 nF and 10 µF. The analog input range is 0 V to V_{DD}. The typical value for the regulator bypass decoupling capacitor (REGCAP) is 1 µF. The conversion result is output in a 12-bit word with the MSB first.

Alternatively, because the supply current required by the AD7091 is so low, a precision reference can be used as the supply source to the part. A reference such as the REF195 or ADR4550 can be used where a 5 V supply is desired. The REF193 or ADR4530 are recommended for use when a 3 V supply is required for the ADC. This configuration is especially useful if the power supply is quite noisy, or if the system supply voltages are at some value other than 5 V or 3 V, such as 15 V.

If the busy indicator function is required, connect a pull-up resistor of typically 100 kΩ to V_{DD} to the SDO pin (see Figure 19).

In addition, for applications in which power consumption is a concern, the power-down mode can be used to improve the power performance of the ADC (see the Modes of Operation section for more information).

ANALOG INPUT

Figure 18 shows an equivalent circuit of the AD7091 analog input structure. The D1 and D2 diodes provide ESD protection for the analog input. To prevent the diodes from becoming forward-biased and conducting current, ensure that the analog input signal never exceeds V_{DD} by more than 300 mV. These diodes can conduct a maximum of 10 mA without causing irreversible damage to the part.

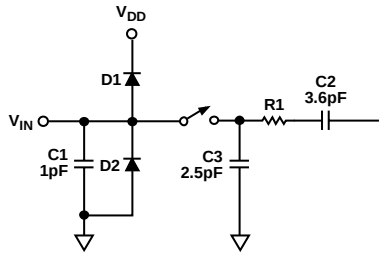

Figure 18. Equivalent Analog Input Circuit

Capacitor C1 in Figure 18 is typically about 1 pF and can primarily be attributed to pin capacitance. Resistor R1 is a lumped component made up of the on resistance of a switch. This resistor is typically about 500 Ω. Capacitor C2 is the ADC sampling capacitor and typically has a capacitance of 3.6 pF.

In applications where harmonic distortion and signal-to-noise ratio (SNR) are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC and may necessitate the use of an input buffer amplifier, as shown in Figure 19. The choice of the op amp is a function of the particular application.

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. The THD increases as the source impedance increases and performance degrades. Figure 9 shows a graph of THD vs. source impedance when using a supply voltage of 3 V and a sampling rate of 1 MSPS.

To achieve the specified performance, use an external filter—such as the one-pole, low-pass RC filter shown in Figure 19—on the analog input connected to the AD7091.

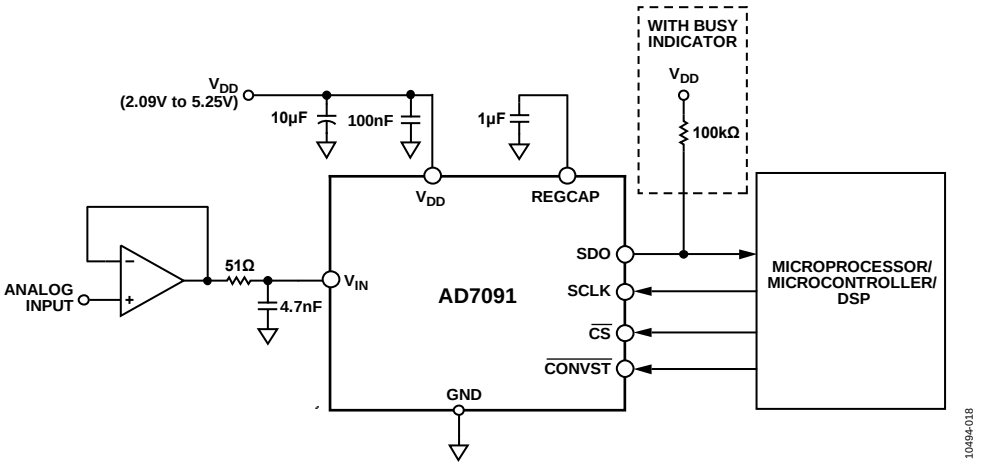

Figure 19. Typical Connection Diagram

MODES OF OPERATION

The mode of operation of the AD7091 is selected by controlling the logic level of the $\overline{\text{CONVST}}$ signal when a conversion is complete. The two modes of operation are normal mode and power-down mode. These modes of operation provide flexible power management options, allowing optimization of the power dissipation to throughput rate ratio for different application requirements.

The logic level of the $\overline{\text{CONVST}}$ pin at the end of a conversion determines whether the AD7091 remains in normal mode or enters power-down mode (see the Normal Mode section and the Power-Down Mode section). Similarly, if the device is in power-down mode, $\overline{\text{CONVST}}$ controls whether the device returns to normal mode or remains in power-down mode.

Normal Mode

The normal mode of operation is intended to achieve the fastest throughput rate performance. In normal mode, the AD7091 remains fully powered at all times, so power-up times are not a concern. Figure 20 shows the general timing diagram of the AD7091 in normal mode.

In normal mode, the conversion is initiated on the falling edge of $\overline{\text{CONVST}}$, as described in the Serial Interface section. To ensure that the part remains fully powered at all times, $\overline{\text{CONVST}}$ must return high after t_7 and remain high until the conversion is complete. At the end of a conversion (denoted as EOC in Figure 20), the logic level of $\overline{\text{CONVST}}$ is tested.

To read back data stored in the conversion result register, wait until the conversion is complete, and then pull $\overline{\text{CS}}$ low. The conversion data is subsequently clocked out on the SDO pin (see Figure 20). Because the output shift register is 12 bits wide, data is shifted out of the device as a 12-bit word under the control of the serial clock input (SCLK). After reading back the data, the user can pull $\overline{\text{CONVST}}$ low again to start another conversion after the t_{QUIET} time has elapsed.

Power-Down Mode

The power-down mode of operation is intended for use in applications where slower throughput rates and lower power consumption are required. In this mode, the ADC can be powered down after each conversion or after a series of conversions performed at a high throughput rate, with the ADC powered down for relatively long durations between these bursts of several conversions. When the AD7091 is in power-down mode, the serial interface remains active even though all analog circuitry is powered down.

To enter power-down mode, pull $\overline{\text{CONVST}}$ low and keep it low prior to the end of a conversion (denoted as EOC in Figure 21). After the conversion is complete, the logic level of the $\overline{\text{CONVST}}$ pin is tested. If the $\overline{\text{CONVST}}$ signal is logic low, the part enters power-down mode.

The serial interface of the AD7091 is functional in power-down mode; therefore, users can read back the conversion result after the part enters power-down mode.

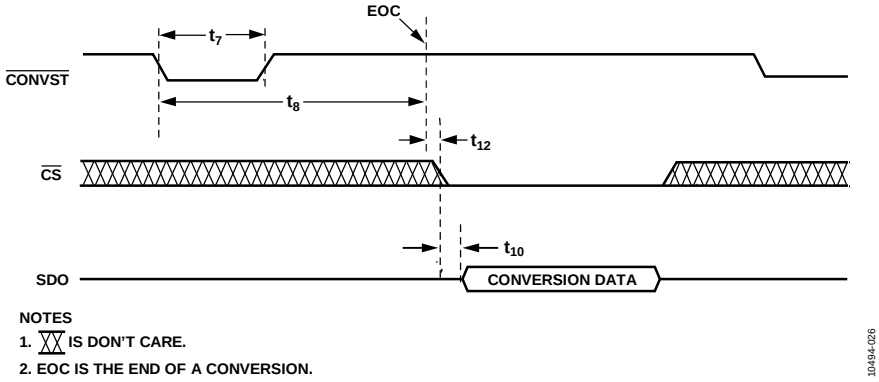

Figure 20. Normal Mode of Operation, Serial Interface Read Timing

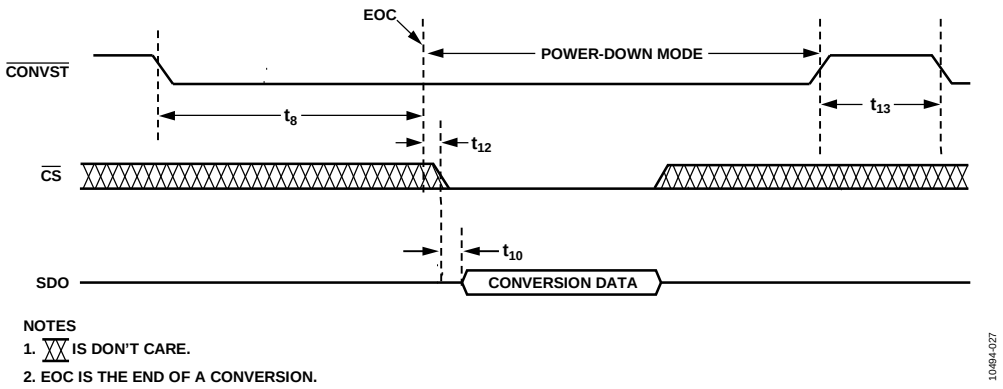

Figure 21. Entering and Exiting Power-Down Mode

To exit power-down mode and power up the AD7091, pull CONVST high at any time. On the rising edge of CONVST, the device begins to power up. The power-up time of the AD7091 is 100 µs. To start the next conversion, operate the interface as described in the Normal Mode section.

POWER CONSUMPTION

The two modes of operation for the AD7091—normal mode and power-down mode (see the Modes of Operation section for more information)—produce different power vs. throughput rate performances. Using a combination of normal mode and power-down mode achieves the optimum power performance.

To achieve optimum static current consumption, SCLK should be in burst mode and CS should idle high. Failure to adhere to these guidelines results in increased static current.

Improved power consumption for the AD7091 can also be achieved by carefully selecting the V_{DD} supply (see Figure 13).

Power Consumption in Normal Mode

With a 3 V V_{DD} supply and a throughput rate of 1 MSPS, the I_{DD} current consumption for the part in normal operational mode is 367 µA (composed of 9.1 µA of static current and 357.9 µA of dynamic current during conversion). The dynamic current consumption is directly proportional to the throughput rate.

The following example calculates the power consumption of the AD7091 when operating in normal mode with a 500 kSPS throughput rate and a 3 V supply.

The dynamic conversion time contributes 537 µW to the overall power dissipation as follows:

((500 kSPS/1 MSPS) × 357.9 µA) × 3 V = 537 µW

The contribution to the total power dissipated by the normal mode static operation is

9.1 µA × 3 V = 27 µW

Therefore, the total power dissipated at 500 kSPS is

537 µW + 27 µW = 564 µW

Power Consumption Using a Combination of Normal Mode and Power-Down Mode

A combination of normal mode and power-down mode achieves the optimum power performance. This operation can be performed at constant sampling rates of <10 kSPS.

Figure 22 shows the AD7091 conversion sequence using a combination of normal mode and power-down mode with a throughput of 5 kSPS. With a V_{DD} supply voltage of 3 V, the static current is 9.1 µA. The dynamic current is 357.9 µA at 1 MSPS. The current consumption during power-down mode is 324 nA. A conversion takes typically 650 ns to complete, and the AD7091 takes 100 µs to power up from power-down mode.

The dynamic conversion time contributes 5 µW to the overall power dissipation as follows:

((5 kSPS/1 MSPS) × 357.9 µA) × 3 V = 5 µW

The contribution to the total power dissipated by the normal mode static operation and the power-down mode is

(((100 µs + 650 ns)/200 µs) × 9.1 µA) × 3 V +
((99.4 µs/200 µs) × 324 nA) × 3 V = 14 µW

Therefore, the total power dissipated at 5 kSPS is

5 µW + 14 µW = 19 µW

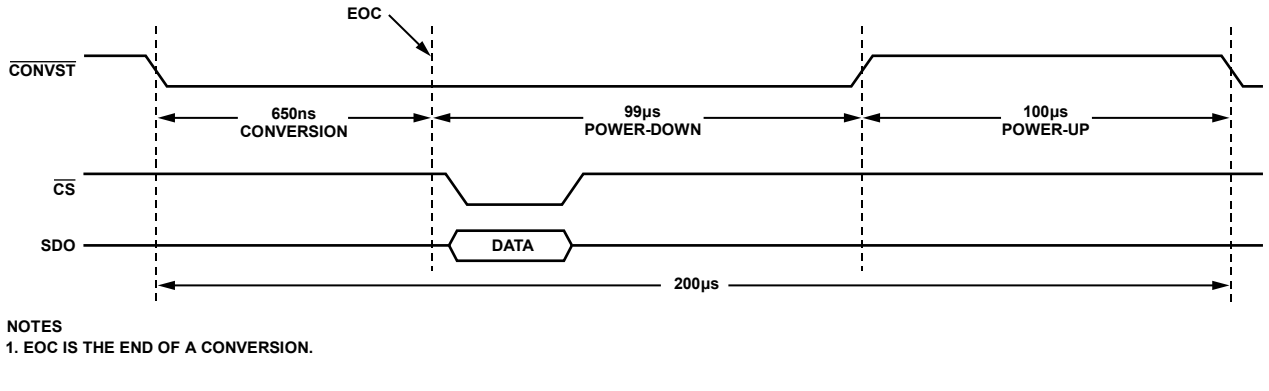

Figure 22. Conversion Sequence with Normal Mode and Power-Down Mode, 5 kSPS Throughput

Figure 23 and Figure 24 show the typical power dissipation vs. throughput rate for the AD7091 at 3 V for the V_{DD} supply. Figure 24 shows the reduction in power consumption that can be achieved when power-down mode is used compared with using only normal mode at lower throughput rates.

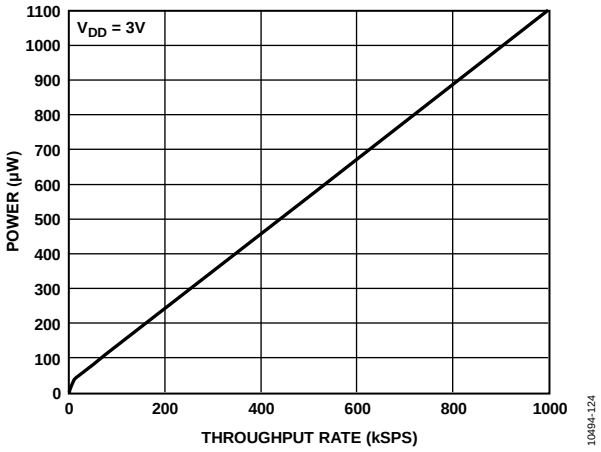

Figure 23. Power Dissipation vs. Throughput Rate (Full Range)

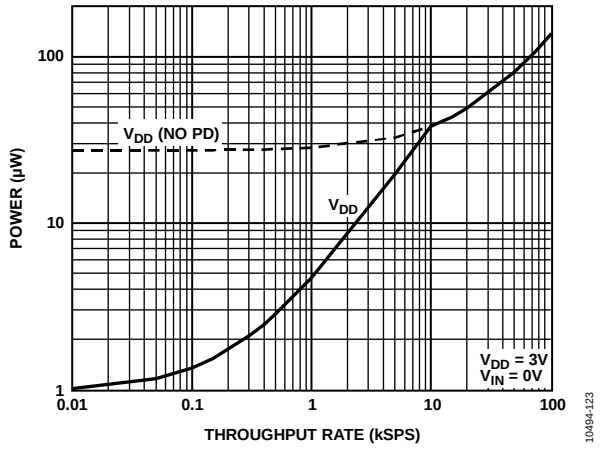

Figure 24. Power Dissipation vs. Throughput Rate (Lower Range)

MULTIPLEXER APPLICATIONS

A multiplexer can be used in the signal chain to switch multiple analog input signals to the AD7091. In such applications, control the multiplexer switch time to ensure accurate analog-to digital-conversion of the input signals. To allow the AD7091 to fully acquire the input signal, the multiplexer should switch in the channel to be converted a minimum of 350 ns before initiating a conversion. The multiplexer should also hold this channel at the AD7091 for a minimum of 200 ns after the $\overline{\text{CONVST}}$ falling edge.

SERIAL INTERFACE

The AD7091 serial interface consists of four signals: SCLK, SDO, $\overline{\text{CONVST}}$, and $\overline{\text{CS}}$. The serial interface is used to access data from the result register and to control the modes of operation of the device.

- The SCLK pin is the serial clock input for the device.
- The SDO pin outputs the conversion result; data transfers take place with respect to SCLK.
- The $\overline{\text{CONVST}}$ pin is used to initiate the conversion process and to select the mode of operation of the AD7091 (see the Modes of Operation section).
- The $\overline{\text{CS}}$ pin is used to frame the data. The falling edge of $\overline{\text{CS}}$ takes the SDO line out of a high impedance state. A rising edge on $\overline{\text{CS}}$ returns the SDO line to a high impedance state.

The logic level of $\overline{\text{CS}}$ at the end of a conversion determines whether the busy indicator is enabled. This feature affects the propagation of the MSB with respect to $\overline{\text{CS}}$ and SCLK.

BUSY INDICATOR ENABLED

When the busy indicator is enabled, the SDO pin can be used as an interrupt signal to indicate that a conversion is complete. The connection diagram for this configuration is shown in Figure 25. Note that a pull-up resistor to V_{DD} is required on the SDO pin.

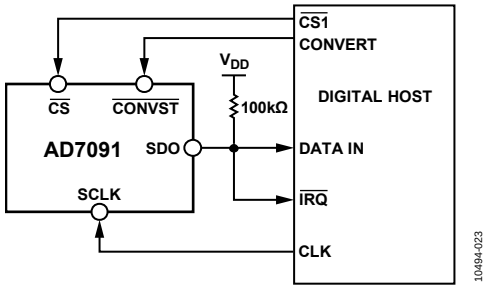

Figure 25. Connection Diagram with Busy Indicator

The busy indicator allows the host to detect when the SDO pin exits the three-state condition after the end of a conversion. When the busy indicator is enabled, 13 SCLK cycles are required: 12 clock cycles to propagate the data and an additional clock cycle to return the SDO pin to the three-state condition.

To enable the busy indicator feature, a conversion must first be started. A high-to-low transition on $\overline{\text{CONVST}}$ initiates a conversion. This transition places the track-and-hold into hold mode and samples the analog input at this point. If the user does not want the AD7091 to enter power-down mode, $\overline{\text{CONVST}}$ should be taken high before the end of the conversion.

A conversion requires 650 ns to complete. When the conversion process is finished, the track-and-hold returns to track mode. Before the end of a conversion, pull $\overline{\text{CS}}$ low to enable the busy indicator (see Figure 26). The busy indicator is not valid for this first conversion, only on subsequent conversions. The user must ensure that $\overline{\text{CS}}$ is pulled low before the end of each conversion to keep the busy indicator enabled.

The conversion result is shifted out of the device as a 12-bit word under the control of SCLK and the logic level of $\overline{\text{CS}}$ at the end of a conversion. At the end of a conversion, SDO is driven low. SDO remains low until the MSB (DB11) of the conversion result is clocked out on the first falling edge of SCLK. DB10 to DB0 are shifted out on the subsequent falling edges of SCLK. The 13th SCLK falling edge returns SDO to a high impedance state. Data is propagated on SCLK falling edges and is valid on both the rising and falling edges of the next SCLK. The timing diagram for this operation is shown in Figure 26.

If another conversion is required, pull $\overline{\text{CONVST}}$ low again and repeat the cycle.

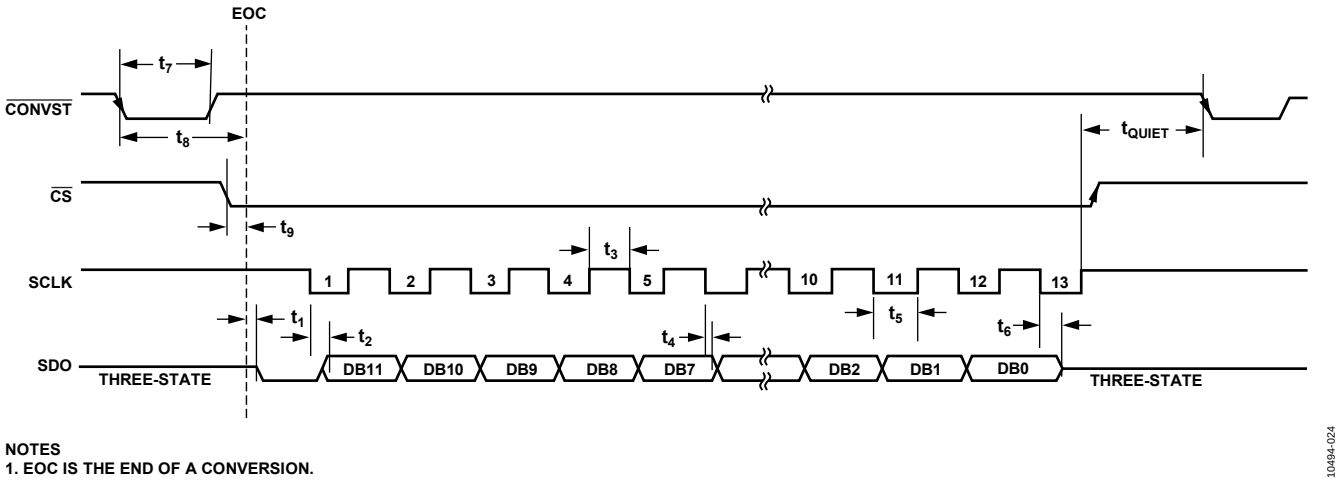

Figure 26. Serial Port Timing with Busy Indicator

BUSY INDICATOR DISABLED

To operate the AD7091 without the busy indicator, a conversion must first be started. A high-to-low transition on $\overline{\text{CONVST}}$ initiates a conversion. This transition places the track-and-hold into hold mode and samples the analog input at this point. If the user does not want the AD7091 to enter power-down mode, $\overline{\text{CONVST}}$ should be taken high before the end of the conversion.

A conversion requires 650 ns to complete. When the conversion process is finished, the track-and-hold returns to track mode. To prevent the busy indicator from becoming enabled, ensure that $\overline{\text{CS}}$ is pulled high before the end of the conversion (see Figure 27).

The conversion result is shifted out of the device as a 12-bit word under the control of SCLK and $\overline{\text{CS}}$. The MSB (Bit DB11) is clocked out on the falling edge of $\overline{\text{CS}}$. DB10 to DB0 are shifted out on the subsequent falling edges of SCLK. The 12th SCLK falling edge returns SDO to a high impedance state. After all the data is clocked out, pull $\overline{\text{CS}}$ high again. Data is propagated on SCLK falling edges and is valid on both the rising and falling edges of the next SCLK. The timing diagram for this operation is shown in Figure 27.

If another conversion is required, pull $\overline{\text{CONVST}}$ low again and repeat the cycle.

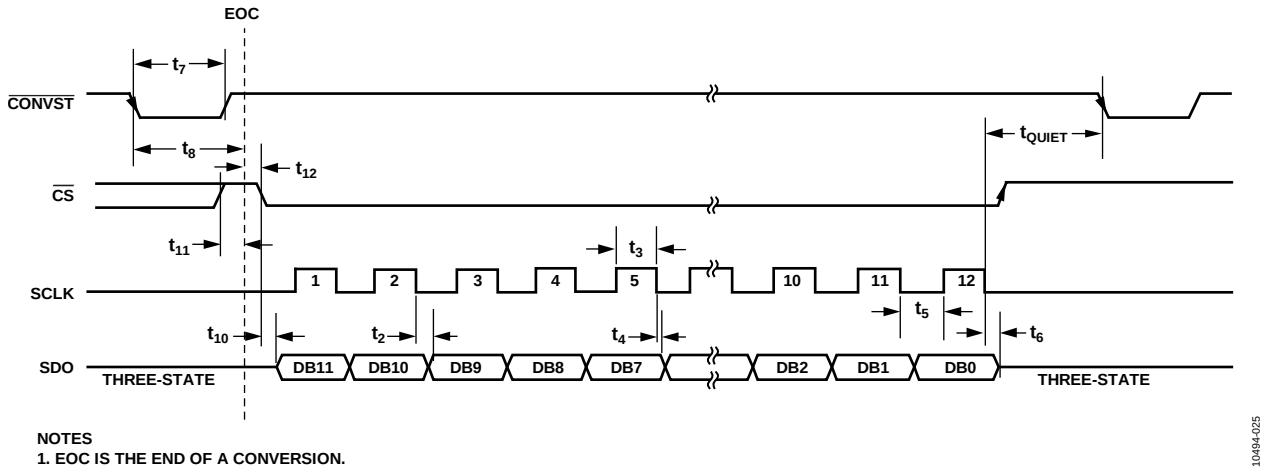

Figure 27. Serial Port Timing Without Busy Indicator

SOFTWARE RESET

The AD7091 requires the user to initiate a software reset upon power-up. Note that failure to apply the correct software reset command may result in a device malfunction. The timing diagram for the software reset operation is shown in Figure 28.

To issue a software reset,

1. Start a conversion by pulling $\overline{\text{CONVST}}$ low.
2. Read back the conversion result by pulling $\overline{\text{CS}}$ low after the conversion is complete.
3. Between the second and eighth SCLK cycles, pull $\overline{\text{CS}}$ high to short cycle the read operation.
4. At the end of the next conversion, the software reset is executed.

As soon as a software reset is issued, the user can start another conversion by pulling $\overline{\text{CONVST}}$ low.

INTERFACING WITH AN 8-/16-BIT SPI BUS

It is also possible to interface the AD7091 with a conventional 8-/16-bit SPI bus.

Performing conversions and reading results can be achieved by configuring the host SPI interface for 16 bits, which results in providing an additional four SCLK cycles to complete a conversion compared with the standard interface methods (see the Busy Indicator Enabled section and the Busy Indicator Disabled section).

After the 13th SCLK falling edge with the busy indicator enabled or after the 12th SCLK falling edge with the busy indicator disabled, SDO returns to a high impedance state. The additional four bits should be treated as don't care bits by the host. All other timings are as shown in Figure 26 and Figure 27, with t_{QUIET} starting after the 16th SCLK cycle.

A software reset can be performed by configuring the SPI bus for eight bits and performing the operation described in the Software Reset section.

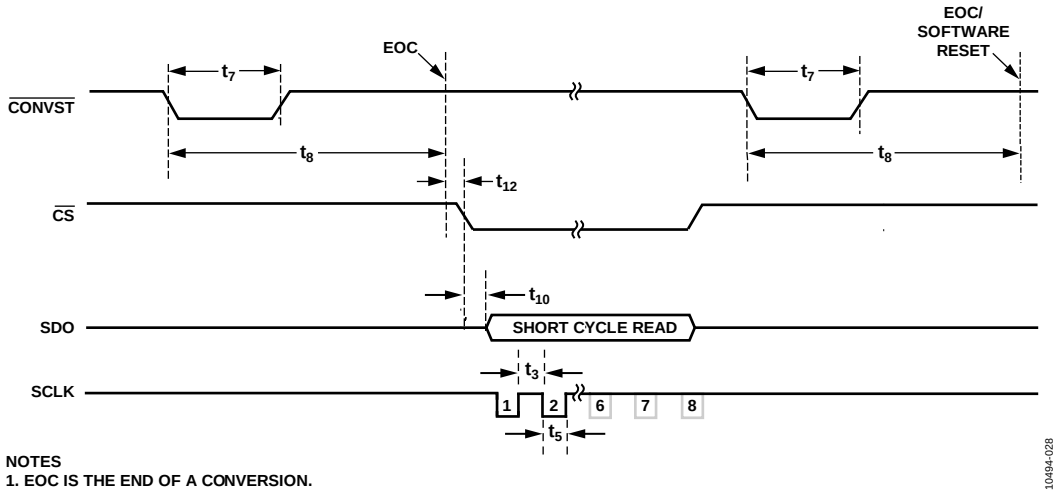

Figure 28. Software Reset Timing

OUTLINE DIMENSIONS

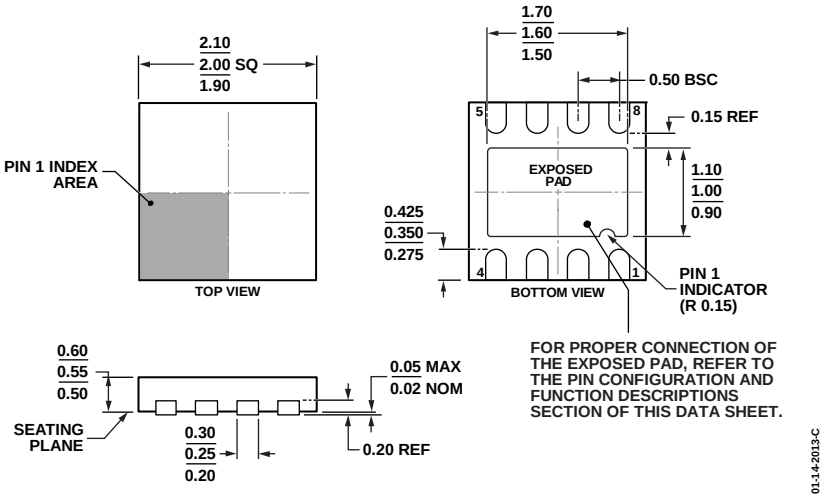

Figure 29. 8-Lead Lead Frame Chip Scale Package [LFCSP_UD]
2.00 mm × 2.00 mm Body, Ultra Thin, Dual Lead
(CP-8-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD7091BCPZ-RL	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP_UD]	CP-8-10	92
AD7091BCPZ-RL7	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP_UD]	CP-8-10	92
EVAL-AD7091SDZ		Evaluation Board		
EVAL-SDP-CB1Z		Evaluation Controller Board		

[1] Z = RoHS Compliant Part.

NOTES

NOTES

D10996-0-3/15(B)

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