10-Bit, 10-Channel, Multiformat SDTV/HDTV Video Decoder and RGB Graphics Digitizer

Data Sheet **ADV7181D**

FEATURES

Four 10-bit ADCs sampling up to 75 MHz
10 analog input channels
SCART fast blank support
Internal antialiasing filters
NTSC, PAL, and SECAM color standards supported
525p/625p component progressive scan supported
720p/1080i component HDTV supported
Digitizes RGB graphics up to 1024 × 768 at 70 Hz (XGA)
3 × 3 color space conversion matrix
Industrial temperature range: −40°C to +85°C
12-bit 4:4:4 DDR, 8-/10-/16-/20-bit SDR pixel output interface
Programmable interrupt request output pin
Small package
Low pin count
Single front end for video and graphics
VBI data slicer (including teletext)
Qualified for automotive applications

APPLICATIONS

Automotive entertainment
HDTVs
LCD/DLP® projectors
HDTV STBs with PVR
DVD recorders with progressive scan input support
AVR receivers

GENERAL DESCRIPTION

The ADV7181D is a high quality, single-chip, multiformat video decoder and graphics digitizer. This multiformat decoder supports the conversion of PAL, NTSC, and SECAM standards in the form of composite or S-Video into a digital ITU-R BT.656 format.

The ADV7181D also supports the decoding of a component RGB/YPrPb video signal into a digital YCrCb or RGB pixel output stream. Support for component video includes standards such as 525i, 625i, 525p, 625p, 720p, 1080i, and many other HD and SMPTE standards.

Graphics digitization is also supported by the ADV7181D; it is capable of digitizing RGB graphics signals from VGA to XGA rates and converting them into a digital DDR RGB or YCrCb pixel output stream. SCART and overlay functionality are enabled by the ability of the ADV7181D to simultaneously process CVBS and standard definition RGB signals. The mixing of these signals is controlled by the fast blank (FB) pin.

The ADV7181D contains two main processing sections. The first section is the standard definition processor (SDP), which processes all PAL, NTSC, and SECAM signal types. The second section is the component processor (CP), which processes YPrPb and RGB component formats, including RGB graphics.

The ADV7181D has unique software and hardware configuration requirements. For more information, see the Typical Connection Diagram section.

Rev. A **Document Feedback**

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Evaluation Kits

- ADV7181D Evaluation Board

Documentation

Application Notes

- AN-1180: Optimizing Video Platforms for Automated Post-Production Self-Tests
- AN-1260: Crystal Design Considerations for Video Decoders, HDMI Receivers, and Transceivers

Data Sheet

- ADV7181D: 10-Bit, 10-Channel, Multiformat SDTV/ HDTV Video Decoder and RGB Graphics Digitizer Data Sheet

User Guides

- ADV7181D Design Support Files

Design Resources

- ADV7181D Material Declaration
- PCN-PDN Information
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12/11—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

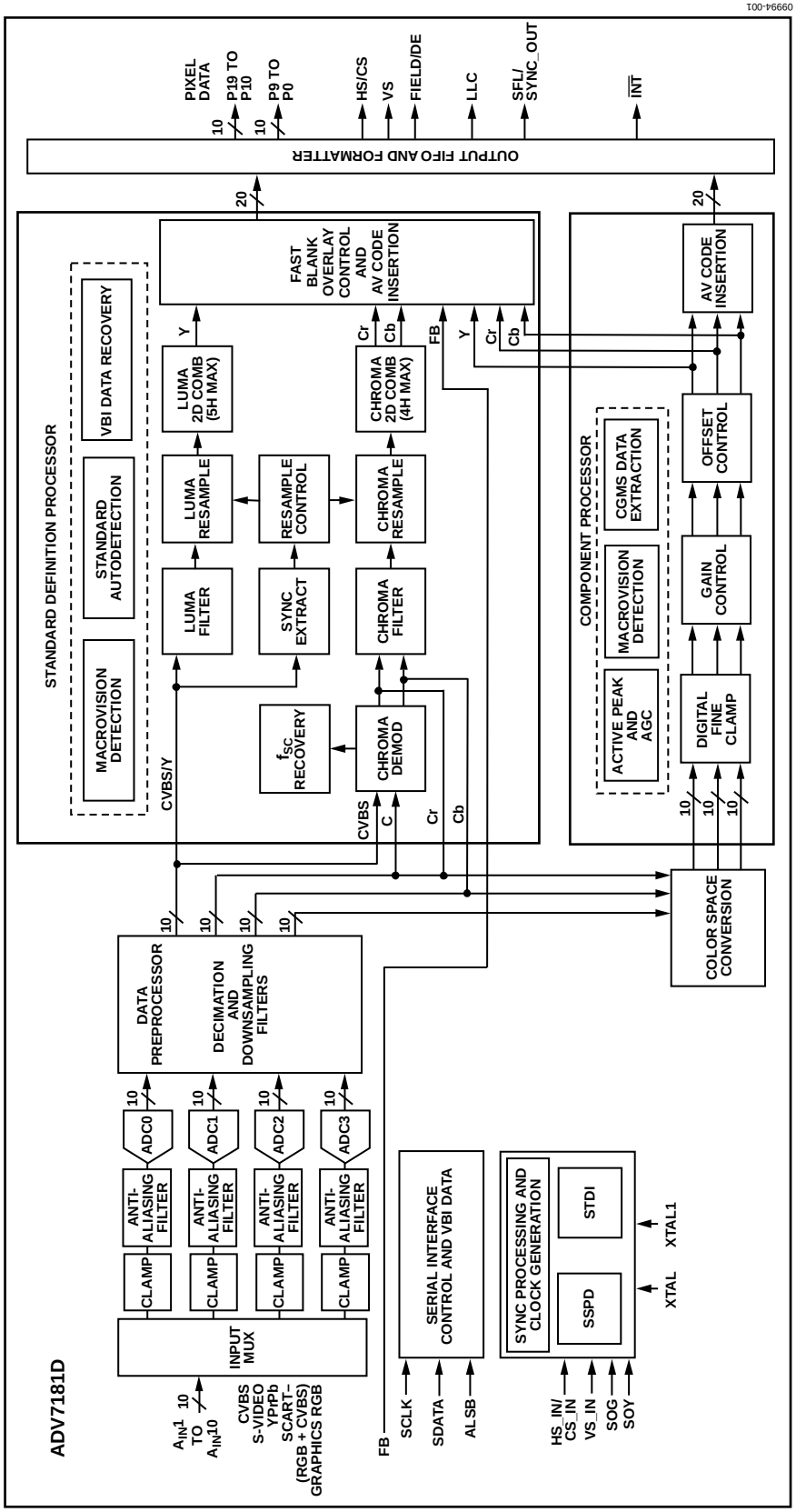


Figure 1.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

AVDD = 3.15 V to 3.45 V, DVDD = 1.65 V to 2.0 V, DVDDIO = 3.0 V to 3.6 V, PVDD = 1.71 V to 1.89 V, nominal input range = 1.6 V. T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted. The minimum and maximum specifications are guaranteed over this temperature range.

Table 1.

Parameter[1]	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
STATIC PERFORMANCE[2, 3]						
Resolution (Each ADC)	N				10	Bits
Integral Nonlinearity	INL	BSL at 27 MHz (10-bit level)		±0.6	±2.5	LSB
		BSL at 54 MHz (10-bit level)		−0.6/+0.7		LSB
		BSL at 74 MHz (10-bit level)		±1.4		LSB
Differential Nonlinearity	DNL	At 27 MHz (10-bit level)		−0.2/+0.25	−0.99/+2.5	LSB
		At 54 MHz (10-bit level)		−0.2/+0.25		LSB
		At 74 MHz (10-bit level)		±0.9		LSB
DIGITAL INPUTS						
Input High Voltage[4]	V_{IH}		2			V
		HS_IN, VS_IN low trigger mode	0.7			V
Input Low Voltage[5]	V_{IL}				0.8	V
		HS_IN, VS_IN low trigger mode			0.3	V
Input Current	I_{IN}		−10		+10	µA
Input Capacitance[6]	C_{IN}				10	pF
DIGITAL OUTPUTS						
Output High Voltage[7]	V_{OH}	I_{SOURCE} = 0.4 mA	2.4			V
Output Low Voltage[7]	V_{OL}	I_{SINK} = 3.2 mA			0.4	V
High Impedance Leakage Current	I_{LEAK}	Pin 1			60	µA
		All other output pins			10	µA
Output Capacitance[6]	C_{OUT}				20	pF
POWER REQUIREMENTS[6]						
Digital Core Power Supply	DVDD		1.65	1.8	2.0	V
Digital I/O Power Supply	DVDDIO		3.0	3.3	3.6	V
PLL Power Supply	PVDD		1.71	1.8	1.89	V
Analog Power Supply	AVDD		3.15	3.3	3.45	V
Digital Core Supply Current	I_{DVDD}	CVBS input sampling at 54 MHz		105		mA
		Graphics RGB sampling at 75 MHz		90		mA
		SCART RGB FB sampling at 54 MHz		106		mA
Digital I/O Supply Current	I_{DVDDIO}	CVBS input sampling at 54 MHz		4		mA
		Graphics RGB sampling at 75 MHz		38		mA
PLL Supply Current	I_{PVDD}	CVBS input sampling at 54 MHz		11		mA
		Graphics RGB sampling at 75 MHz		12		mA
Analog Supply Current[8]	I_{AVDD}	CVBS input sampling at 54 MHz		99		mA
		Graphics RGB sampling at 75 MHz		166		mA
		SCART RGB FB sampling at 54 MHz		200		mA
Power-Down Current	I_{PWRDN}			2.25		mA
Green Mode Power-Down	I_{PWRDNG}	Synchronization bypass function		16		mA
Power-Up Time	t_{PWRUP}			20		ms

[1] All specifications are obtained using the Analog Devices, Inc., recommended programming scripts.
[2] All ADC linearity tests performed at input range of full scale − 12.5% and at zero scale + 12.5%.
[3] Maximum INL and DNL specifications obtained with part configured for component video input.
[4] To obtain specified V_{IH} level on Pin 22, program Register 0x13 (WO) with a value of 0x04. If Register 0x13 is programmed with a value of 0x00, then V_{IH} on Pin 22 is 1.2 V.
[5] To obtain specified V_{IL} level on Pin 22, program Register 0x13 (WO) with a value of 0x04. If Register 0x13 is programmed with a value of 0x00, then V_{IL} on Pin 22 is 0.4 V.
[6] Guaranteed by characterization.
[7] V_{OH} and V_{OL} levels obtained using default drive strength value (0xD5) in Register Subaddress 0xF4.
[8] For CVBS current measurements only, ADC0 is powered up. For RGB current measurements only, ADC0, ADC1, and ADC2 are powered up. For SCART FB current measurements, all four ADCs are powered up.

VIDEO SPECIFICATIONS

AVDD = 3.15 V to 3.45 V, DVDD = 1.65 V to 2.0 V, DVDDIO = 3.0 V to 3.6 V, PVDD = 1.71 V to 1.89 V. T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted. The minimum and maximum specifications are guaranteed over this temperature range.

Table 2.

Parameter[1]	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NONLINEAR SPECIFICATIONS						
Differential Phase	DP	CVBS input, modulated 5 step		0.5		Degrees
Differential Gain	DG	CVBS input, modulated 5 step		0.5		%
Luma Nonlinearity	LNL	CVBS input, 5 step		0.5		%
NOISE SPECIFICATIONS						
Signal-to-Noise Ratio, Unweighted	SNR	Luma ramp	54	56		dB
		Luma flat field	58	60		dB
Analog Front-End Crosstalk				60		dB
LOCK TIME SPECIFICATIONS						
Horizontal Lock Range			−5		+5	%
Vertical Lock Range			40		70	Hz
f_{SC} Subcarrier Lock Range				±1.3		kHz
Color Lock-In Time				60		Lines
Synchronization Depth Range[2]			20		200	%
Color Burst Range			5		200	%
Vertical Lock Time				2		Fields
Horizontal Lock Time				100		Lines
CHROMA SPECIFICATIONS						
Hue Accuracy				1		Degrees
Color Saturation Accuracy	CL_AC			1		%
Color AGC Range			5		400	%
Chroma Amplitude Error				0.5		%
Chroma Phase Error				0.4		Degrees
Chroma Luma Intermodulation				0.2		%
LUMA SPECIFICATIONS						
Luma Brightness Accuracy		CVBS, 1 V input		1		%
Luma Contrast Accuracy		CVBS, 1 V input		1		%

[1] Guaranteed by characterization.
[2] Nominal synchronization depth is 300 mV at 100% synchronization depth range.

ANALOG SPECIFICATIONS

AVDD = 3.15 V to 3.45 V, DVDD = 1.65 V to 2.0 V, DVDDIO = 3.0 V to 3.6 V, PVDD = 1.71 V to 1.89 V. T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted. The minimum and maximum specifications are guaranteed over this temperature range. The recommended analog input video signal range is 0.5 V to 1.6 V, typically 1 V p-p.

Table 3.

Parameter[1]	Test Conditions/Comments	Min	Typ	Max	Unit
CLAMP CIRCUITRY					
External Clamp Capacitor			0.1		µF
Input Impedance					
All Pins Except for Pin 32 (FB)	Clamps switched off		10		MΩ
Pin 32 (FB)			20		kΩ
Common-Mode Level (CML)			1.86		V
ADC Full-Scale Level			CML + 0.8		V
ADC Zero-Scale Level			CML − 0.8		V
ADC Dynamic Range			1.6		V
Clamp Level (When Locked)	CVBS input		CML − 0.292		V
	SCART RGB input (R, G, B signals)		CML − 0.4		V
	S-Video input (Y signal)		CML − 0.292		V
	S-Video input (C signal)		CML		V
	Component input (Y, Pr, Pb signals)		CML − 0.3		V
	PC RGB input (R, G, B signals)		CML − 0.3		V
Large Clamp Source Current	SDP only		0.75		mA
Large Clamp Sink Current	SDP only		0.9		mA
Fine Clamp Source Current	SDP only		17		µA
Fine Clamp Sink Current	SDP only		17		µA

[1] Guaranteed by characterization.

TIMING CHARACTERISTICS

AVDD = 3.15 V to 3.45 V, DVDD = 1.65 V to 2.0 V, DVDDIO = 3.0 V to 3.6 V, PVDD = 1.71 V to 1.89 V. T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted. The minimum and maximum specifications are guaranteed over this temperature range.

Table 4.

Parameter[1]	Symbol	Description	Min	Typ	Max	Unit
SYSTEM CLOCK AND CRYSTAL						
Crystal Nominal Frequency				28.63636		MHz
Crystal Frequency Stability					±50	ppm
Horizontal Sync Input Frequency			14.8		110	kHz
LLC Frequency Range			12.825		75	MHz
I²C PORT[2]						
SCLK Frequency					400	kHz
SCLK Minimum Pulse Width High	t_1		0.6			µs
SCLK Minimum Pulse Width Low	t_2		1.3			µs
Hold Time (Start Condition)	t_3		0.6			µs
Setup Time (Start Condition)	t_4		0.6			µs
SDATA Setup Time	t_5		100			ns
SCLK and SDATA Rise Time	t_6				300	ns
SCLK and SDATA Fall Time	t_7				300	ns
Setup Time (Stop Condition)	t_8			0.6		µs
RESET FEATURE						
Reset Pulse Width			5			ms
CLOCK OUTPUTS						
LLC Mark-Space Ratio	t_9:t_{10}		45:55		55:45	% duty cycle
DATA AND CONTROL OUTPUTS						
Data Output Transition Time						
SDR (SDP)[3]	t_{11}	Negative clock edge to start of valid data			3.6	ns
	t_{12}	End of valid data to negative clock edge			2.4	ns
SDR (CP)[4]	t_{13}	End of valid data to negative clock edge			2.8	ns
	t_{14}	Negative clock edge to start of valid data			0.1	ns
DDR (CP)[4, 5]	t_{15}	Positive clock edge to end of valid data	$-4 + T_{LLC}/4$			ns
	t_{16}	Positive clock edge to start of valid data	$0.25 + T_{LLC}/4$			ns
	t_{17}	Negative clock edge to end of valid data	$-2.95 + T_{LLC}/4$			ns
	t_{18}	Negative clock edge to start of valid data	$-0.5 + T_{LLC}/4$			ns

[1] Guaranteed by characterization.
[2] TTL input values are 0 V to 3 V, with rise/fall times of ≤3 ns, measured between the 10% and 90% points.
[3] SDP timing figures obtained using default drive strength value (0xD5) in Register Subaddress 0xF4.
[4] CP timing figures obtained using maximum drive strength value (0xFF) in Register Subaddress 0xF4.
[5] DDR timing specifications dependent on LLC output pixel clock; $T_{LLC}/4$ = 9.25 ns at LLC = 27 MHz.

Timing Diagrams

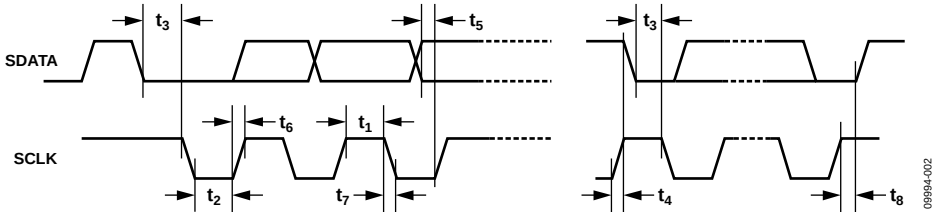


Figure 2. I²C Timing

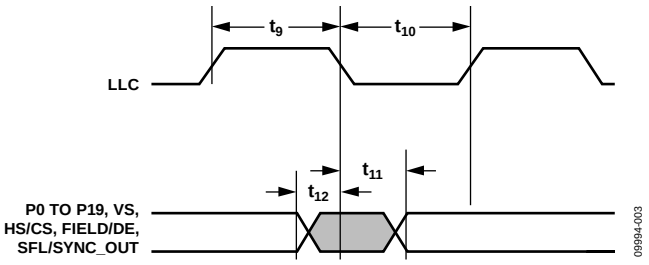


Figure 3. Pixel Port and Control SDR Output Timing (SDP Core)

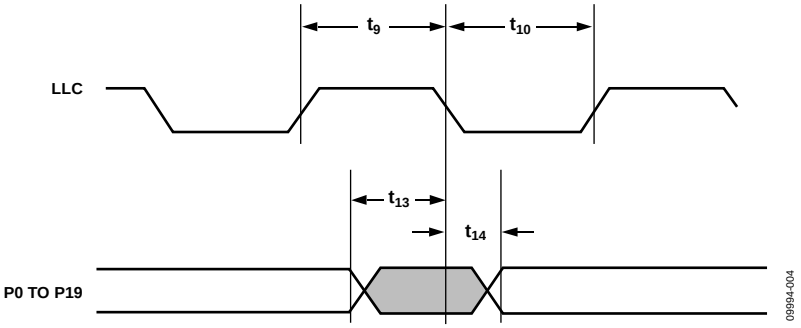


Figure 4. Pixel Port and Control SDR Output Timing (CP Core)

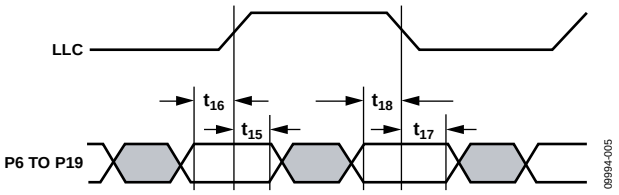


Figure 5. Pixel Port and Control DDR Output Timing (CP Core)

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
AVDD to GND	4 V
DVDD to GND	2.2 V
PVDD to GND	2.2 V
DVDDIO to GND	4 V
DVDDIO to AVDD	−0.3 V to +0.3 V
PVDD to DVDD	−0.3 V to +0.3 V
DVDDIO to PVDD	−0.3 V to +2 V
DVDDIO to DVDD	−0.3 V to +2 V
AVDD to PVDD	−0.3 V to +2 V
AVDD to DVDD	−0.3 V to +2 V
Digital Inputs to GND	GND − 0.3 V to DVDDIO + 0.3 V
Digital Outputs to GND	GND − 0.3 V to DVDDIO + 0.3 V
Analog Inputs to GND	GND − 0.3 V to AVDD + 0.3 V
Operating Temperature Range	−40°C to +85°C
Maximum Junction Temperature ($T_{J\,MAX}$)	125°C
Storage Temperature Range	−65°C to +150°C
Infrared Reflow, Soldering (20 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

REFLOW SOLDER

The ADV7181D is a Pb-free, environmentally friendly product. It is manufactured using the most up-to-date materials and processes. The coating on the leads of each device is 100% pure Sn electroplate. The device is suitable for Pb-free applications and can withstand surface-mount soldering at up to 255°C ± 5°C.

In addition, the ADV7181D is backward-compatible with conventional SnPb soldering processes. This means that the electroplated Sn coating can be soldered with Sn/Pb solder pastes at conventional reflow temperatures of 220°C to 235°C.

PACKAGE THERMAL PERFORMANCE

To reduce power consumption when using the part, turn off any unused ADCs.

It is imperative that the recommended scripts be used for the following high current modes: SCART, 720p, 1080i, and all RGB graphic standards. Using the recommended scripts ensures correct thermal performance. These scripts are available from a local field applications engineer (FAE).

The junction temperature must always stay below the maximum junction temperature ($T_{J\,MAX}$) of 125°C. The junction temperature can be calculated by

$$T_J = T_{A\,MAX} + (\theta_{JA} \times W_{MAX})$$

where:
$T_{A\,MAX}$ = 85°C.
θ_{JA} = 20.3°C/W.
$W_{MAX} = ((AVDD \times I_{AVDD}) + (DVDD \times I_{DVDD}) + (DVDDIO \times I_{DVDDIO}) + (PVDD \times I_{PVDD}))$

THERMAL RESISTANCE

Table 6 specifies the typical values for the junction-to-ambient thermal resistance (θ_{JA}) and the junction-to-case thermal resistance (θ_{JC}) for an ADV7181D soldered on a 4-layer PCB with solid ground plane.

Table 6. Thermal Resistance

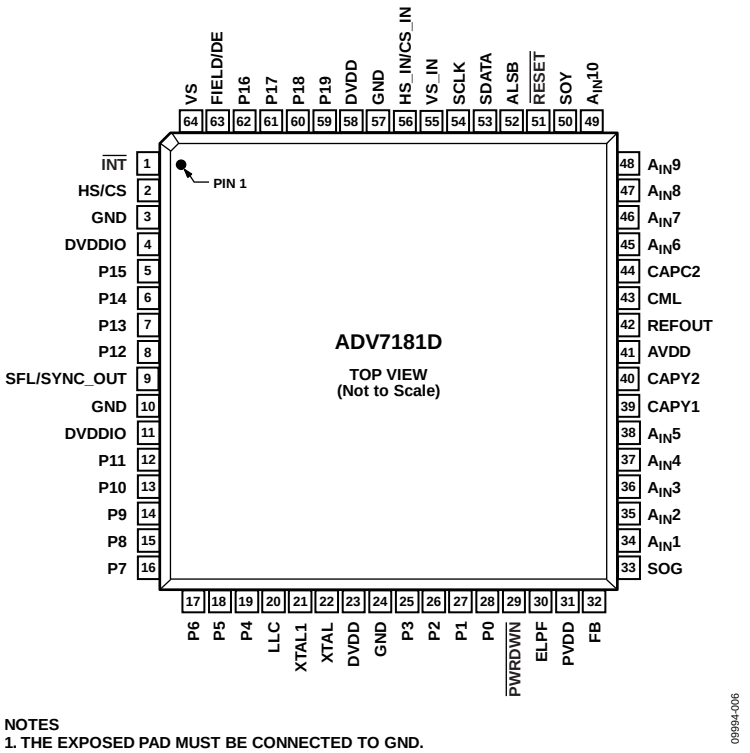
Package Type	θ_{JA}[1]	θ_{JC}	Unit
64-Lead LFCSP (CP-64-3)	20.3	1.2	°C/W

[1] In still air.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD MUST BE CONNECTED TO GND.

Figure 6. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	$\overline{\text{INT}}$	Output	Interrupt. This pin can be active low or active high. When SDP/CP status bits change, this pin is triggered. The set of events that triggers an interrupt is under user control.
2	HS/CS	Output	Horizontal Synchronization Output Signal (HS). Available in SDP and CP modes. Digital Composite Synchronization Signal (CS). Available in CP mode only.
3, 10, 24, 57	GND	Ground	Ground.
4, 11	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
28 to 25, 19 to 12, 8 to 5, 62 to 59	P0 to P19	Output	Video Pixel Output Port. See Table 10 and Table 11 for output configuration modes.
9	SFL/SYNC_OUT	Output	Subcarrier Frequency Lock (SFL). This pin contains a serial output stream that can be used to lock the subcarrier frequency when this decoder is connected to any Analog Devices digital video encoder. Sliced Synchronization Output Signal (SYNC_OUT). Available in CP mode only.
20	LLC	Output	Line-Locked Clock Output for Pixel Data. The range is 12.825 MHz to 75 MHz.
21	XTAL1	Output	This pin should be connected to the 28.63636 MHz crystal or left unconnected if an external 3.3 V, 28.63636 MHz clock oscillator source is used to clock the ADV7181D. In crystal mode, the crystal must be a fundamental crystal.
22	XTAL	Input	Input Pin for the 28.63636 MHz Crystal. This input can be overdriven by an external 3.3 V, 28.63636 MHz clock oscillator source to clock the ADV7181D.
23, 58	DVDD	Power	Digital Core Supply Voltage (1.8 V).
29	$\overline{\text{PWRDWN}}$	Input	Power-Down Input. A Logic 0 on this pin places the ADV7181D in power-down mode.
30	ELPF	Output	External Loop Filter Output. The recommended external loop filter must be connected to this pin (see the Recommended External Loop Filter Components section).
31	PVDD	Power	PLL Supply Voltage (1.8 V).
32	FB	Input	Fast Blank Input. Fast switch between CVBS and RGB analog signals.
33	SOG	Input	Sync on Green Input. Used in embedded synchronization mode.

Pin No.	Mnemonic	Type	Description
34 to 38, 45 to 49	$A_{IN}1$ to $A_{IN}10$	Input	Analog Video Input Channels.
39, 40	CAPY1, CAPY2	Input	ADC Capacitor Network. See Figure 9 for a recommended capacitor network for these pins.
41	AVDD	Power	Analog Supply Voltage (3.3 V).
42	REFOUT	Output	Internal Voltage Reference Output. See Figure 9 for a recommended capacitor network for this pin.
43	CML	Output	Common-Mode Level Pin for the Internal ADCs. See Figure 9 for a recommended capacitor network for this pin.
44	CAPC2	Input	ADC Capacitor Network. See Figure 9 for a recommended capacitor network for this pin.
50	SOY	Input	Sync on Luma Input. Used in embedded synchronization mode.
51	$\overline{\text{RESET}}$	Input	System Reset Input, Active Low. A minimum low reset pulse width of 5 ms is required to reset the ADV7181D circuitry.
52	ALSB	Input	This pin selects the I^2C address for the ADV7181D control and VBI readback ports. When set to Logic 0, this pin sets the address for a write to Control Port 0x40 and the readback address for VBI Port 0x21. When set to Logic 1, this pin sets the address for a write to Control Port 0x42 and the readback address for VBI Port 0x23.
53	SDATA	Input/ Output	I^2C Port Serial Data Input/Output Pin.
54	SCLK	Input	I^2C Port Serial Clock Input. Maximum clock rate of 400 kHz.
55	VS_IN	Input	Vertical Synchronization Input Signal. This pin can be configured in CP mode to extract timing in a 5-wire mode.
56	HS_IN/CS_IN	Input	Horizontal Synchronization Input Signal (HS_IN). This pin can be configured in CP mode to extract timing in a 5-wire mode. Composite Synchronization Input Signal (CS_IN). This pin can be configured in CP mode to extract timing in a 4-wire mode.
63	FIELD/DE	Output	Field Synchronization Output Signal (FIELD). Used in all interlaced video modes. Data Enable Signal (DE). This pin can also be used as a data enable (DE) signal in CP mode to allow direct connection to an HDMI/DVI transmitter IC.
64	VS	Output	Vertical Synchronization Output Signal (SDP and CP Modes).
EP	Exposed Pad		The exposed pad must be connected to GND.

FUNCTIONAL OVERVIEW

This section provides a brief description of the functionality of the ADV7181D. For more information, see the Detailed Descriptions section.

ANALOG FRONT END

The analog front end of the ADV7181D contains four high quality, 10-bit ADCs and a multiplexer (mux) with 10 analog input channels to enable multisource connection without the requirement of an external multiplexer. The analog front end also provides the following:

- Four current and voltage clamp control loops to ensure that dc offsets are removed from the video signal
- SCART functionality and standard definition (SD) RGB overlay on CVBS controlled by the fast blank (FB) input
- Four internal antialiasing filters to remove out-of-band noise on standard definition input video signals

STANDARD DEFINITION PROCESSOR (SDP) PIXEL DATA OUTPUT MODES

The ADV7181D features the following SDP pixel data output modes:

- 8-/10-bit ITU-R BT.656 4:2:2 YCrCb with embedded time codes and/or HS, VS, and FIELD
- 16-/20-bit 4:2:2 YCrCb with embedded time codes and/or HS, VS, and FIELD

COMPONENT PROCESSOR (CP) PIXEL DATA OUTPUT MODES

The ADV7181D features the following CP pixel data output modes for single data rate (SDR) and double data rate (DDR):

- SDR 8-/10-bit 4:2:2 YCrCb for 525i and 625i
- SDR 16-/20-bit 4:2:2 YCrCb for all standards
- DDR 8-/10-bit 4:2:2 YCrCb for all standards
- DDR 12-bit 4:4:4 RGB for graphics inputs

COMPOSITE AND S-VIDEO PROCESSING

Composite and S-Video processing features offer support for NTSC M/J, NTSC 4.43, PAL B/D/I/G/H, PAL60, PAL M, PAL N, and SECAM (B, D, G, K, and L) standards in the form of CVBS and S-Video. Superadaptive, 2D, five-line comb filters for NTSC and PAL provide superior chrominance and luminance separation for composite video.

Composite and S-Video processing features also include full automatic detection and autoswitching of all worldwide standards (PAL, NTSC, and SECAM) and automatic gain control (AGC) with white peak mode to ensure that the video is always processed without loss of the video processing range. Other features include

- Adaptive Digital Line Length Tracking (ADLLT™), a proprietary architecture for locking to weak, noisy, and unstable sources from VCRs and tuners
- IF filter block to compensate for high frequency luma attenuation due to tuner SAW filter
- Chroma transient improvement (CTI)
- Luminance digital noise reduction (DNR)
- Color controls including hue, brightness, saturation, contrast, and Cr and Cb offset controls
- Certified Macrovision® copy protection detection on composite and S-Video for all worldwide formats (PAL/NTSC/SECAM)
- 4× oversampling (54 MHz) for CVBS, S-Video, and YUV modes
- Line-locked clock (LLC) output
- Letterbox detection support
- Free-run output mode to provide stable timing when no video input is present
- Vertical blanking interval (VBI) data processor, including teletext, video programming system (VPS), vertical interval time codes (VITC), closed captioning (CC), extended data service (XDS), wide screen signaling (WSS), copy generation management system (CGMS), and compatibility with GemStar® 1×/2× electronic program guide
- Clocked from a single 28.63636 MHz crystal
- Subcarrier frequency lock (SFL) output for downstream video encoder
- Differential gain, typically 0.5%
- Differential phase, typically 0.5°

COMPONENT VIDEO PROCESSING

Component video processing supports formats including 525i, 625i, 525p, 625p, 720p, 1080i, and many other HD formats, as well as automatic adjustments that include gain (contrast) and offset (brightness), and manual adjustment controls. Other features supported by component video processing include

- Analog component YPrPb/RGB video formats with embedded synchronization or with separate HS, VS, or CS
- Color space conversion matrix to support YCrCb-to-DDR RGB and RGB-to-YCrCb conversions
- Standard identification (STDI) to enable system level component format detection
- Synchronization source polarity detector (SSPD) to determine the source and polarity of the synchronization signals that accompany the input video
- Certified Macrovision copy protection detection on component formats (525i, 625i, 525p, and 625p)
- Free-run output mode to provide stable timing when no video input is present
- Arbitrary pixel sampling support for nonstandard video sources

RGB GRAPHICS PROCESSING

RGB graphics processing offers a 75 MSPS conversion rate that supports RGB input resolutions up to 1024 × 768 at 70 Hz (XGA), automatic or manual clamp and gain controls for graphics modes, and contrast and brightness controls. Other features include

- 32-phase DLL to allow optimum pixel clock sampling
- Automatic detection of synchronization source and polarity by SSPD block
- Standard identification enabled by the STDI block
- RGB that can be color space converted to YCrCb and decimated to a 4:2:2 format for videocentric back-end IC interfacing
- Data enable (DE) output signal supplied for direct connection to HDMI®/DVI transmitter IC
- Arbitrary pixel sampling support for nonstandard video sources
- RGB graphics supported on 12-bit DDR format

GENERAL FEATURES

The ADV7181D features HS/CS, VS, and FIELD/DE output signals with programmable position, polarity, and width, as well as a programmable interrupt request output pin, $\overline{\text{INT}}$, that signals SDP/CP status changes. Other features include

- Low power consumption: 1.8 V digital core, 3.3 V analog and digital I/O, low power, power-down mode, and green PC mode
- Industrial temperature range of −40°C to +85°C
- 64-lead, 9 mm × 9 mm, Pb-free LFCSP
- 3.3 V ADCs giving enhanced dynamic range and performance

DETAILED DESCRIPTIONS

ANALOG FRONT END

The ADV7181D analog front end comprises four 10-bit ADCs that digitize the analog video signal before applying it to the SDP or CP. The analog front end uses differential channels to each ADC to ensure high performance in a mixed-signal application.

The front end also includes a 10-channel input mux that enables multiple video signals to be applied to the ADV7181D. Current and voltage clamps are positioned in front of each ADC to ensure that the video signal remains within the range of the converter. Fine clamping of the video signals is performed downstream by digital fine clamping in either the CP or SDP.

Optional antialiasing filters are positioned in front of each ADC. These filters can be used to band-limit standard definition video signals, removing spurious out-of-band noise.

The ADCs are configured to run in 4× oversampling mode when decoding composite and S-Video inputs; 2× oversampling is performed for component 525i, 625i, 525p, and 625p sources. All other video standards are 1× oversampled. Oversampling the video signals reduces the cost and complexity of external antialiasing filters with the benefit of an increased signal-to-noise ratio (SNR).

The ADV7181D can support simultaneous processing of CVBS and RGB standard definition signals to enable SCART compatibility and overlay functionality. A combination of CVBS and RGB inputs can be mixed and output under the control of the I^2C registers and the fast blank (FB) pin.

STANDARD DEFINITION PROCESSOR (SDP)

The SDP section is capable of decoding a large selection of baseband video signals in composite, S-Video, and YUV formats. The video standards supported by the SDP include PAL B/D/I/G/H, PAL60, PAL M, PAL N, NTSC M/J, NTSC 4.43, and SECAM B/D/G/K/L. The ADV7181D automatically detects the video standard and processes it accordingly.

The SDP has a five-line, superadaptive, 2D comb filter that provides superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts its processing mode according to video standards and signal quality with no user intervention required. The SDP has an IF filter block that compensates for attenuation in the high frequency luma spectrum due to the tuner SAW filter.

The SDP has specific luminance and chrominance parameter control for brightness, contrast, saturation, and hue.

The ADV7181D implements a patented ADLLT algorithm to track varying video line lengths from sources such as a VCR. ADLLT enables the ADV7181D to track and decode poor quality video sources such as VCRs, noisy sources from tuner outputs, VCD players, and camcorders.

The SDP also contains a chroma transient improvement (CTI) processor. This processor increases the edge rate on chroma transitions, resulting in a sharper video image.

The SDP can process a variety of VBI data services, such as teletext, closed captioning (CC), wide screen signaling (WSS), video programming system (VPS), vertical interval time codes (VITC), copy generation management system (CGMS), GemStar 1×/2×, and extended data service (XDS). The ADV7181D SDP section has a Macrovision 7.1 detection circuit that allows it to detect Type I, Type II, and Type III protection levels. The decoder is also fully robust to all Macrovision signal inputs.

COMPONENT PROCESSOR (CP)

The CP section is capable of decoding and digitizing a wide range of component video formats in any color space. Component video standards supported by the CP are 525i, 625i, 525p, 625p, 720p, 1080i, graphics up to XGA at 70 Hz, and many other standards.

The CP section of the ADV7181D contains an AGC block. When no embedded synchronization is present, the video gain can be set manually. The AGC section is followed by a digital clamp circuit, which ensures that the video signal is clamped to the correct blanking level. Automatic adjustments within the CP include gain (contrast) and offset (brightness); manual adjustment controls are also supported.

A fixed mode graphics RGB to component output is available.

A color space conversion matrix is placed between the analog front end and the CP section. This enables YCrCb-to-DDR RGB and RGB-to-YCrCb conversions. Many other standards of color space can be implemented using the color space converter.

The output section of the CP is highly flexible. It can be configured in SDR mode with one data packet per clock cycle or in DDR mode where data is presented on the rising and falling edges of the clock. In SDR and DDR modes, HS/CS, VS, and FIELD/DE (where applicable) timing reference signals are provided. In SDR mode, a 20-bit 4:2:2 is possible. In DDR mode, the ADV7181D can be configured in an 8-bit or 10-bit 4:2:2 YCrCb or in a 12-bit 4:4:4 RGB pixel output interface with corresponding timing signals.

The CP section contains circuitry to enable the detection of Macrovision encoded YPrPb signals for 525i, 625i, 525p, and 625p. It is designed to be fully robust when decoding these types of signals.

VBI extraction of component data is performed by the CP section of the ADV7181D for interlaced, progressive, and high definition scanning rates. The data extracted can be read back over the I^2C interface.

ANALOG INPUT MUXING

The ADV7181D has an integrated analog muxing section, which allows more than one source of video signal to be connected to the decoder. Figure 7 outlines the overall structure of the input muxing provided in the ADV7181D.

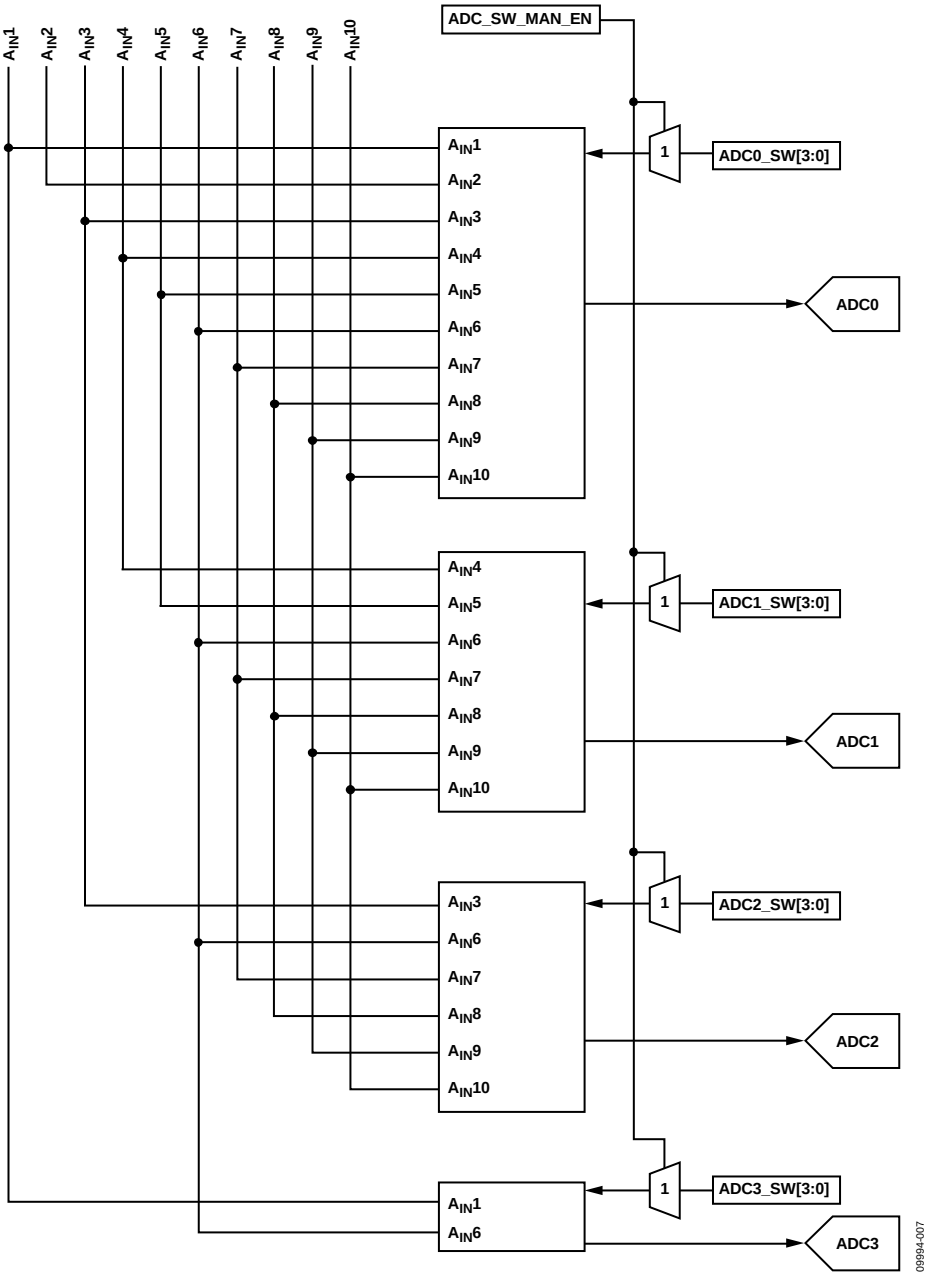


Figure 7. Internal Pin Connections

Table 8 provides the recommended ADC mapping for the ADV7181D.

Table 8. Recommended ADC Mapping

Mode	Required ADC Mapping	Analog Input Channel	Core	Configuration[1]
CVBS	ADC0	CVBS = $A_{IN}1$	SDP	INSEL[3:0] = 0000 SDM_SEL[1:0] = 00 PRIM_MODE[3:0] = 0000 VID_STD[3:0] = 0010
YC/YC Auto	Y = ADC0 C = ADC1	Y = $A_{IN}7$ C = $A_{IN}9$	SDP	INSEL[3:0] = 0000 SDM_SEL[1:0] = 11 PRIM_MODE[3:0] = 0000 VID_STD[3:0] = 0010
Component YUV	Y = ADC0 U = ADC2 V = ADC1	Y = $A_{IN}10$ U = $A_{IN}8$ V = $A_{IN}6$	SDP	INSEL[3:0] = 1001 SDM_SEL[1:0] = 00 PRIM_MODE[3:0] = 0000 VID_STD[3:0] = 0010
Component YUV	Y = ADC0 U = ADC2 V = ADC1	Y = $A_{IN}10$ U = $A_{IN}8$ V = $A_{IN}6$	CP	INSEL[3:0] = 0000 SDM_SEL[1:0] = 00 PRIM_MODE[3:0] = 0000 VID_STD[3:0] = 1010
SCART RGB	CBVS = ADC0 G = ADC1 B = ADC3 R = ADC2	CVBS = $A_{IN}4$ G = $A_{IN}10$ B = $A_{IN}6$ R = $A_{IN}8$	SDP	INSEL[3:0] = 0000 SDM_SEL[1:0] = 00 PRIM_MODE[3:0] = 0000 VID_STD[3:0] = 0010
Graphics RGB Mode	G = ADC0 B = ADC2 R = ADC1	G = $A_{IN}2$ B = $A_{IN}3$ R = $A_{IN}5$	CP	INSEL[3:0] = 0000 SDM_SEL[1:0] = 00 PRIM_MODE[3:0] = 0010 VID_STD[3:0] = 1100

[1] Configuration to format follow-on blocks in correct frame.

The analog input muxes of the ADV7181D must be controlled directly. This is referred to as manual input muxing. The manual muxing is activated by setting the ADC_SW_MAN_EN bit (see Table 9). It affects only the analog switches in front of the ADCs. The INSEL, SDM_SEL, PRIM_MODE, and VID_STD bits must still be set so that the follow-on blocks process the video data in the correct format.

Not every input pin can be routed to any ADC. The analog signal routing inside the IC imposes restrictions on the channel routing. See Table 9 for an overview of the routing capabilities inside the chip. The four mux sections can be controlled by the reserved control signal buses ADC0_SW[3:0], ADC1_SW[3:0], ADC2_SW[3:0], and ADC3_SW[3:0].

Table 9 explains the ADC mapping configuration for the following:

- ADC_SW_MAN_EN, manual input muxing enable, IO map, Address C4[7]
- ADC0_SW[3:0], ADC0 mux configuration, IO map, Address C3[3:0]
- ADC1_SW[3:0], ADC1 mux configuration, IO map, Address C3[7:4]
- ADC2_SW[3:0], ADC2 mux configuration, IO map, Address C4[3:0]
- ADC3_SW[3:0], ADC3 mux configuration, IO map, Address F3[7:4]

Table 9. Manual MUX Settings for All ADCs

ADC_SW_MAN_EN = 1							
ADC0_SW[3:0]	**ADC0 Connection**	**ADC1_SW[3:0]**	**ADC1 Connection**	**ADC2_SW[3:0]**	**ADC2 Connection**	**ADC3_SW[3:0]**	**ADC3 Connection**
0000	N/A	0000	N/A	0000	N/A	0000	N/A
0001	$A_{IN}2$	0001	N/A	0001	N/A	0001	N/A
0010	$A_{IN}3$	0010	N/A	0010	$A_{IN}3$	0010	N/A
0011	$A_{IN}5$	0011	$A_{IN}5$	0011	N/A	0011	N/A
0100	$A_{IN}6$	0100	$A_{IN}6$	0100	$A_{IN}6$	0100	$A_{IN}6$
0101	$A_{IN}8$	0101	$A_{IN}8$	0101	$A_{IN}8$	0101	N/A
0110	$A_{IN}10$	0110	$A_{IN}10$	0110	$A_{IN}10$	0110	N/A
0111	N/A	0111	N/A	0111	N/A	0111	N/A
1000	N/A	1000	N/A	1000	N/A	1000	N/A
1001	$A_{IN}1$	1001	N/A	1001	N/A	1001	$A_{IN}1$
1010	N/A	1010	N/A	1010	N/A	1010	N/A
1011	$A_{IN}4$	1011	$A_{IN}4$	1011	N/A	1011	N/A
1100	N/A	1100	N/A	1100	N/A	1100	N/A
1101	$A_{IN}7$	1101	$A_{IN}7$	1101	$A_{IN}7$	1101	N/A
1110	$A_{IN}9$	1110	$A_{IN}9$	1110	$A_{IN}9$	1110	N/A
1111	N/A	1111	N/A	1111	N/A	1111	N/A

PIXEL OUTPUT FORMATTING

Table 10. SDP Output Formats—SDR 4:2:2 (8-/10-/16-/20-Bit)

Pixel Output Pin	8-Bit SDR ITU-R BT.656	10-Bit SDR ITU-R BT.656	16-Bit SDR	20-Bit SDR
P19	Y7, Cb7, Cr7	Y9, Cb9, Cr9	Y7	Y9
P18	Y6, Cb6, Cr6	Y8, Cb8, Cr8	Y6	Y8
P17	Y5, Cb5, Cr5	Y7, Cb7, Cr7	Y5	Y7
P16	Y4, Cb4, Cr4	Y6, Cb6, Cr6	Y4	Y6
P15	Y3, Cb3, Cr3	Y5, Cb5, Cr5	Y3	Y5
P14	Y2, Cb2, Cr2	Y4, Cb4, Cr4	Y2	Y4
P13	Y1, Cb1, Cr1	Y3, Cb3, Cr3	Y1	Y3
P12	Y0, Cb0, Cr0	Y2, Cb2, Cr2	Y0	Y2
P11	High-Z	Y1, Cb1, Cr1	High-Z	Y1
P10	High-Z	Y0, Cb0, Cr0	High-Z	Y0
P9	High-Z	High-Z	Cb7, Cr7	Cb9, Cr9
P8	High-Z	High-Z	Cb6, Cr6	Cb8, Cr8
P7	High-Z	High-Z	Cb5, Cr5	Cb7, Cr7
P6	High-Z	High-Z	Cb4, Cr4	Cb6, Cr6
P5	High-Z	High-Z	Cb3, Cr3	Cb5, Cr5
P4	High-Z	High-Z	Cb2, Cr2	Cb4, Cr4
P3	High-Z	High-Z	Cb1, Cr1	Cb3, Cr3
P2	High-Z	High-Z	Cb0, Cr0	Cb2, Cr2
P1	High-Z	High-Z	High-Z	Cb1, Cr1
P0	High-Z	High-Z	High-Z	Cb0, Cr0

Table 11. CP Output Formats—SDR 4:2:2 (16-/20-Bit) and DDR 4:4:4 (12-Bit)

	SDR 4:2:2		12-Bit DDR 4:4:4[1]	
Pixel Output	16-Bit SDR	20-Bit SDR	Clock Rise	Clock Fall
P19	Y7	Y9	B7-0	R3-1
P18	Y6	Y8	B6-0	R2-1
P17	Y5	Y7	B5-0	R1-1
P16	Y4	Y6	B4-0	R0-1
P15	Y3	Y5	B3-0	G7-1
P14	Y2	Y4	B2-0	G6-1
P13	Y1	Y3	B1-0	G5-1
P12	Y0	Y2	B0-0	G4-1
P11	High-Z	Y1	High-Z	High-Z
P10	High-Z	Y0	High-Z	High-Z
P9	Cb7, Cr7	Cb9, Cr9	G3-0	R7-1
P8	Cb6, Cr6	Cb8, Cr8	G2-0	R6-1
P7	Cb5, Cr5	Cb7, Cr7	G1-0	R5-1
P6	Cb4, Cr4	Cb6, Cr6	G0-0	R4-1
P5	Cb3, Cr3	Cb5, Cr5	High-Z	High-Z
P4	Cb2, Cr2	Cb4, Cr4	High-Z	High-Z
P3	Cb1, Cr1	Cb3, Cr3	High-Z	High-Z
P2	Cb0, Cr0	Cb2, Cr2	High-Z	High-Z
P1	High-Z	Cb1, Cr1	High-Z	High-Z
P0	High-Z	Cb0, Cr0	High-Z	High-Z

[1] xx-0 corresponds to data clocked at the rising edge; xx-1 corresponds to data clocked at the falling edge.

RECOMMENDED EXTERNAL LOOP FILTER COMPONENTS

The external loop filter components for the ELPF pin should be placed as close to the pin as possible. Figure 8 shows the recommended component values.

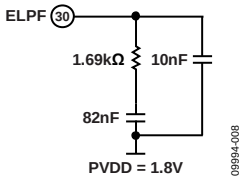


Figure 8. ELPF Components

TYPICAL CONNECTION DIAGRAM

For the latest software configuration files, visit the ADV7181D design support files Web page on the EngineerZone video forum.

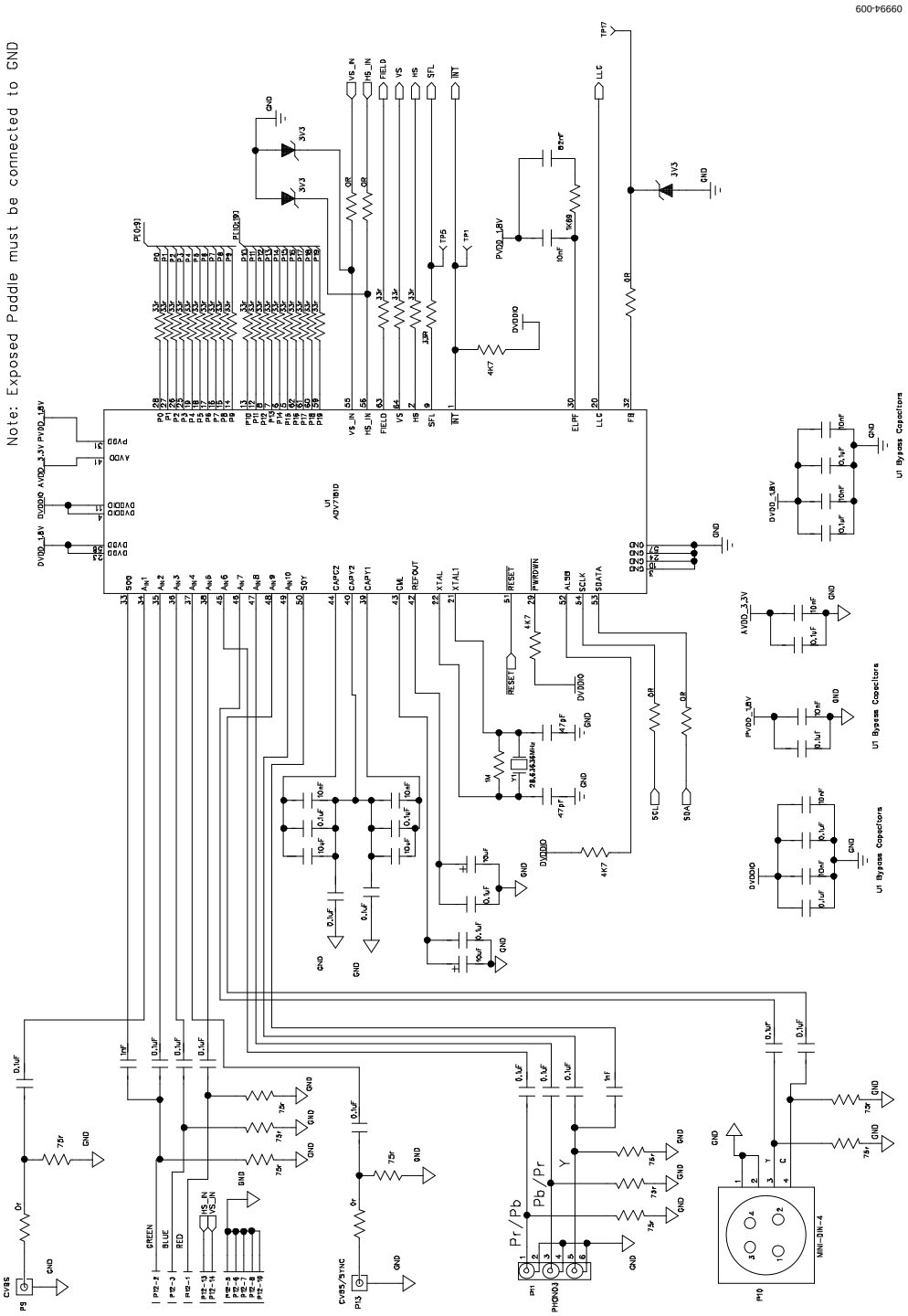


Figure 9. Typical Connection

OUTLINE DIMENSIONS

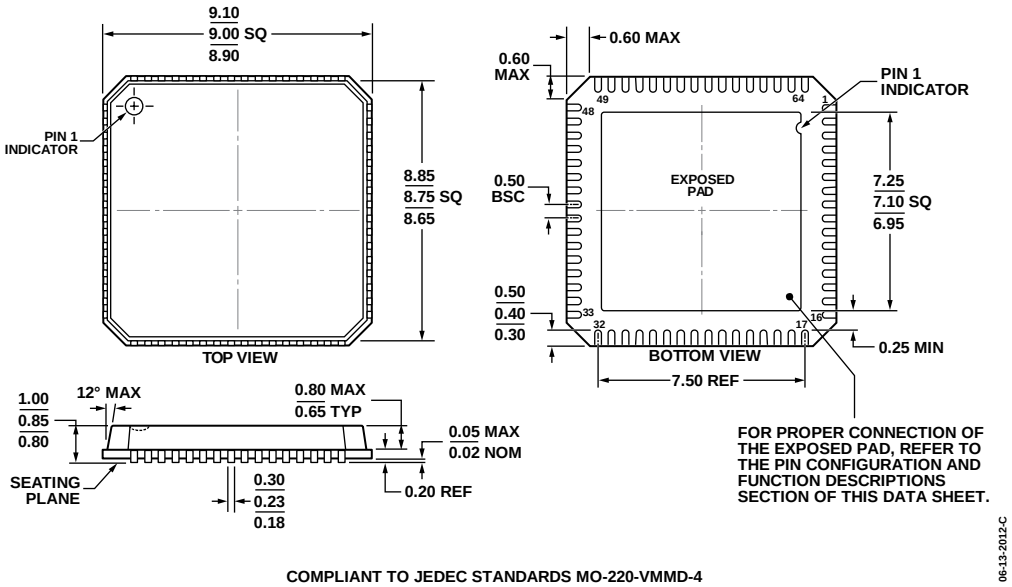


Figure 10. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
(CP-64-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADV7181DBCPZ	−40°C to +85°C	64-Lead LFCSP	CP-64-3
ADV7181DBCPZ-RL	−40°C to +85°C	64-Lead LFCSP	CP-64-3
ADV7181DWBCPZ	−40°C to +85°C	64-Lead LFCSP	CP-64-3
ADV7181DWBCPZ-RL	−40°C to +85°C	64-Lead LFCSP	CP-64-3
EVAL-ADV7181DEBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADV7181DW models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

NOTES

NOTES

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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