## Features

- Very high speed: 45 ns
  - Industrial: –40 °C to +85 °C
  - Automotive-E: –40 °C to +125 °C
- Wide voltage range: 4.5 V–5.5 V
- Ultra low standby power
  - Typical standby current: 2 μA
  - Maximum standby current: 8 μA (Industrial)
- Ultra low active power
  - Typical active current: 1.8 mA at f = 1 MHz
- Ultra low standby power
- Easy memory expansion with $\overline{CE}_1$, $CE_2$ and $\overline{OE}$ features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Available in Pb-free 44-pin TSOP II and 48-ball VFBGA package

## Functional Description

The CY62157E is a high performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Place the device into standby mode when deselected ($\overline{CE}_1$ HIGH or $CE_2$ LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input or output pins ($I/O_0$ through $I/O_{15}$) are placed in a high impedance state when:

- Deselected ($\overline{CE}_1$ HIGH or $CE_2$ LOW)
- Outputs are disabled ($\overline{OE}$ HIGH)
- Both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH)
- Write operation is active ($\overline{CE}_1$ LOW, $CE_2$ HIGH and $\overline{WE}$ LOW)
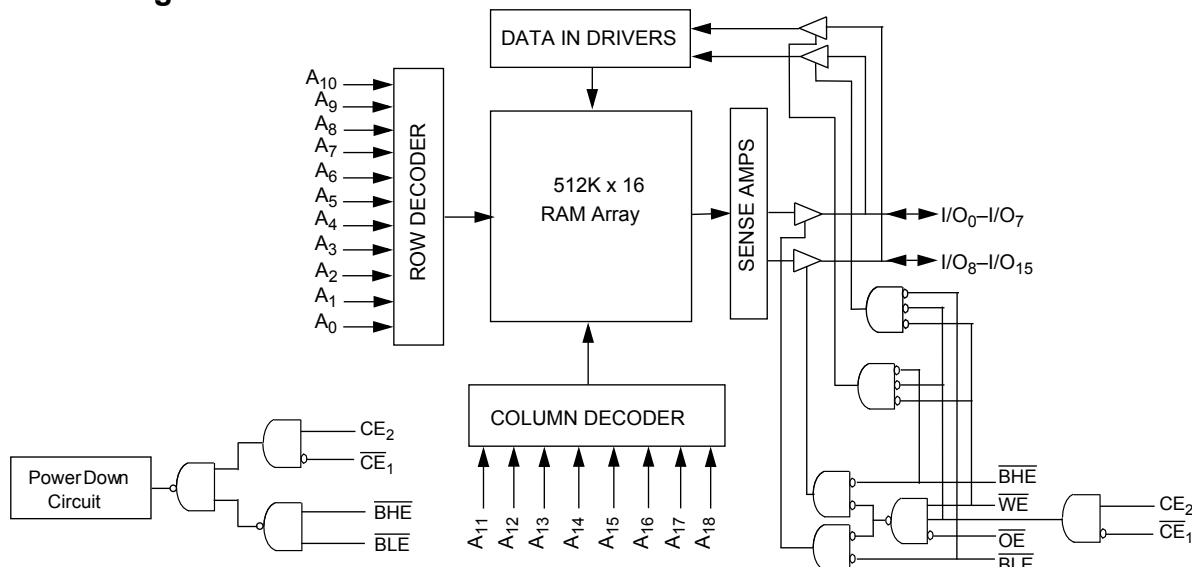
To write to the device, take Chip Enable ($\overline{CE}_1$ LOW and $CE_2$ HIGH) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins ($I/O_0$ through $I/O_7$), is written into the location specified on the address pins ($A_0$ through $A_{18}$). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins ($I/O_8$ through $I/O_{15}$) is written into the location specified on the address pins ($A_0$ through $A_{18}$).

To read from the device, take Chip Enable ($\overline{CE}_1$ LOW and $CE_2$ HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on $I/O_0$ to $I/O_7$. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on $I/O_8$ to $I/O_{15}$. See Truth Table on page 12 for a complete description of read and write modes.

The CY62157E device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see Electrical Characteristics on page 4 for more details and suggested alternatives.

For a complete list of related documentation, click here.

## Logic Block Diagram

# Contents

## Product Portfolio

| Product | Range | $V_{CC}$ Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Operating $I_{CC}$, (mA) | | | | Standby, $I_{SB2}$ ($\mu$A) | |
| | | | | | | f = 1 MHz | | f = $f_{max}$ | | | |
| | | Min | Typ[1] | Max | | Typ[1] | Max | Typ[1] | Max | Typ[1] | Max |
| CY62157ELL | Industrial | 4.5 | 5.0 | 5.5 | 45 | 1.8 | 3 | 18 | 25 | 2 | 8 |
| CY62157ELL | Automotive | 4.5 | 5.0 | 5.5 | 55 | 1.8 | 4 | 18 | 35 | 2 | 30 |

## Pin Configurations

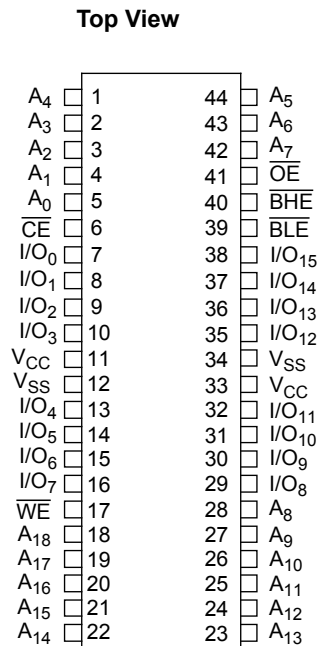### Figure 1.  44-pin TSOP II pinout [2, 3]
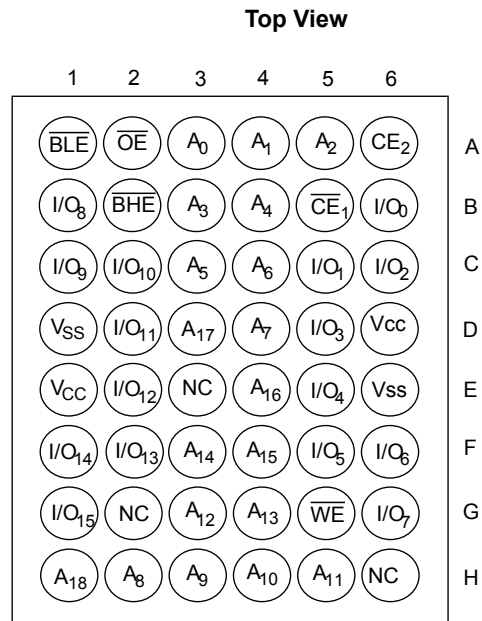
**Top View**



### Figure 2.  48-ball VFBGA pinout [2]

**Top View**



**Notes**
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = $V_{CC(typ)}$, $T_A$ = 25 °C.
2. NC pins are not connected on the die.
3. The 44-pin TSOP II package has only one chip enable ($\overline{CE}$) pin.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ............................. –65 °C to + 150 °C

Ambient Temperature with
Power Applied ........................................ –55 °C to + 125 °C

Supply Voltage to Ground
Potential ........................................................ –0.5 V to 6.0 V

DC Voltage Applied to Outputs
in High Z State [4, 5] ....................................... –0.5 V to 6.0 V

DC Input Voltage [4, 5] ..................................... –0.5 V to 6.0 V

Output Current into Outputs (LOW) ........................... 20 mA

Static Discharge Voltage
(MIL-STD-883, Method 3015) ................................. > 2001 V

Latch up Current .................................................. > 200 mA

## Operating Range

| Device | Range | Ambient Temperature | $V_{CC}$[6] |
|---|---|---|---|
| CY62157ELL | Industrial | –40 °C to +85 °C | 4.5 V to 5.5 V |
| | Automotive | –40 °C to +125 °C | |

## Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | | 45 ns (Industrial) | | | 55 ns (Automotive) | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[7] | Max | Min | Typ[7] | Max | |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = 4.5 V | $I_{OH}$ = –1 mA | 2.4 | – | – | 2.4 | – | – | V |
| | | $V_{CC}$ = 5.5 V | $I_{OH}$ = –0.1 mA | – | – | 3.4 [8] | – | – | 3.4 [8] | |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 2.1 mA | | – | – | 0.4 | – | – | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | $V_{CC}$ = 4.5 V to 5.5 V | | 2.2 | – | $V_{CC}$ + 0.5 | 2.2 | – | $V_{CC}$ + 0.5 | V |
| $V_{IL}$ | Input LOW Voltage | $V_{CC}$ = 4.5 V to 5.5 V | | –0.5 | – | 0.8 | –0.5 | – | 0.8 | V |
| $I_{IX}$ | Input Leakage Current | GND $\leq V_I \leq V_{CC}$ | | –1 | – | +1 | –4 | – | +4 | μA |
| $I_{OZ}$ | Output Leakage Current | GND $\leq V_O \leq V_{CC}$, Output Disabled | | –1 | – | +1 | –4 | – | +4 | μA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | f = $f_{max}$ = 1/$t_{RC}$ | $V_{CC}$ = $V_{CC(max)}$ $I_{OUT}$ = 0 mA CMOS levels | – | 18 | 25 | – | 18 | 35 | mA |
| | | f = 1 MHz | | – | 1.8 | 3 | – | 1.8 | 4 | |
| $I_{SB1}$ [9] | Automatic CE Power Down Current – CMOS Inputs | $\overline{CE}_1 \geq V_{CC}$ – 0.2 V or $CE_2 \leq$ 0.2 V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V, $V_{IN} \leq$ 0.2 V, f = $f_{max}$ (Address and Data Only), f = 0 ($\overline{OE}$ and $\overline{WE}$), $V_{CC}$ = $V_{CC(max)}$ | | – | 2 | 8 | – | 2 | 30 | μA |
| $I_{SB2}$ [9] | Automatic CE Power Down Current – CMOS Inputs | $\overline{CE}_1 \geq V_{CC}$ – 0.2 V or $CE_2 \leq$ 0.2 V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC}$ – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = 0, $V_{CC}$ = $V_{CC(max)}$ | | – | 2 | 8 | – | 2 | 30 | μA |

**Notes**
4. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns for I < 30 mA.
5. $V_{IH(max)}$ = $V_{CC}$ + 0.75 V for pulse durations less than 20 ns.
6. Full device AC operation assumes a 100 μs ramp time from 0 to $V_{CC}$(min) and 200 μs wait time after $V_{CC}$ stabilization.
7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = $V_{CC(typ)}$, $T_A$ = 25 °C.
8. Please note that the maximum $V_{OH}$ limit doesnot exceed minimum CMOS $V_{IH}$ of 3.5 V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum $V_{IH}$ of 3.5V, please refer to Application Note AN6081 for technical details and options you may consider.
9. Chip enables ($\overline{CE}_1$ and $CE_2$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the $I_{SB1}$ / $I_{SB2}$ / $I_{CCDR}$ spec. Other inputs can be left floating.

## Capacitance

| Parameter [10] | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{CC}$ = $V_{CC(typ)}$ | 10 | pF |
| $C_{OUT}$ | Output capacitance | | 10 | pF |

## Thermal Resistance

| Parameter [10] | Description | Test Conditions | 44-pin TSOP II | 48-ball VFBGA | Unit |
|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance (junction to ambient) | Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board | 77 | 72 | °C/W |
| $\Theta_{JC}$ | Thermal resistance (junction to case) | | 13 | 8.86 | °C/W |

## AC Test Loads and Waveforms

**Figure 3. AC Test Loads and Waveforms**
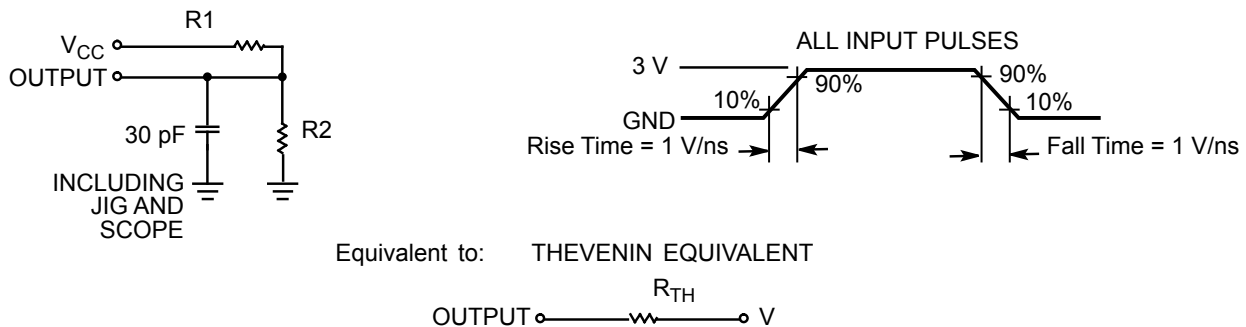


| Parameters | Values | Unit |
|---|---|---|
| R1 | 1800 | Ω |
| R2 | 990 | Ω |
| $R_{TH}$ | 639 | Ω |
| $V_{TH}$ | 1.77 | V |

**Note**
10. Tested initially and after any design or process changes that may affect these parameters.

## Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | | Min | Typ [11] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | | | 2 | – | – | V |
| $I_{CCDR}$[12] | Data Retention Current | $V_{CC}$ = 2 V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V | Industrial | – | – | 8 | μA |
| | | | Automotive | – | – | 30 | |
| $t_{CDR}$[13] | Chip Deselect to Data Retention Time | | | 0 | – | – | ns |
| $t_R$[14] | Operation Recovery Time | | CY62157ELL-45 | 45 | – | – | ns |
| | | | CY62157ELL-55 | 55 | – | – | |

## Data Retention Waveform

**Figure 4. Data Retention Waveform** [15]
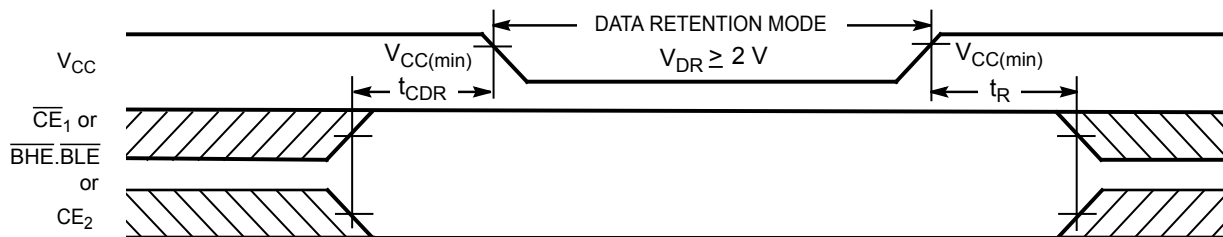


**Notes**
11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = $V_{CC(typ)}$, $T_A$ = 25 °C.
12. Chip enables ($\overline{CE}_1$ and $CE_2$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the $I_{SB1}$ / $I_{SB2}$ / $I_{CCDR}$ spec. Other inputs can be left floating.
13. Tested initially and after any design or process changes that may affect these parameters.
14. Full device operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min)} \geq 100$ μs or stable at $V_{CC(min)} \geq 100$ μs.
15. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

## Switching Characteristics

Over the Operating Range

| Parameter [16, 17] | Description | 45 ns (Industrial) | | 55 ns (Automotive) | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| **Read Cycle** | | | | | | |
| $t_{RC}$ | Read Cycle Time | 45 | – | 55 | – | ns |
| $t_{AA}$ | Address to Data Valid | – | 45 | – | 55 | ns |
| $t_{OHA}$ | Data Hold from Address Change | 10 | – | 10 | – | ns |
| $t_{ACE}$ | $\overline{CE}_1$ LOW and $CE_2$ HIGH to Data Valid | – | 45 | – | 55 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | – | 22 | – | 25 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low Z[18] | 5 | – | 5 | – | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z[18, 19] | – | 18 | – | 20 | ns |
| $t_{LZCE}$ | $\overline{CE}_1$ LOW and $CE_2$ HIGH to Low Z[18] | 10 | – | 10 | – | ns |
| $t_{HZCE}$ | $\overline{CE}_1$ HIGH and $CE_2$ LOW to High Z[18, 19] | – | 18 | – | 20 | ns |
| $t_{PU}$ | $\overline{CE}_1$ LOW and $CE_2$ HIGH to Power Up | 0 | – | 0 | – | ns |
| $t_{PD}$ | $\overline{CE}_1$ HIGH and $CE_2$ LOW to Power Down | – | 45 | – | 55 | ns |
| $t_{DBE}$ | $\overline{BLE}/\overline{BHE}$ LOW to Data Valid | – | 45 | – | 55 | ns |
| $t_{LZBE}$ | $\overline{BLE}/\overline{BHE}$ LOW to Low Z[18] | 10 | – | 10 | – | ns |
| $t_{HZBE}$ | $\overline{BLE}/\overline{BHE}$ HIGH to High Z[18, 19] | – | 18 | – | 20 | ns |
| **Write Cycle** [20, 21] | | | | | | |
| $t_{WC}$ | Write Cycle Time | 45 | – | 55 | – | ns |
| $t_{SCE}$ | $\overline{CE}_1$ LOW and $CE_2$ HIGH to Write End | 35 | – | 40 | – | ns |
| $t_{AW}$ | Address Setup to Write End | 35 | – | 40 | – | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | – | 0 | – | ns |
| $t_{SA}$ | Address Setup to Write Start | 0 | – | 0 | – | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 35 | – | 40 | – | ns |
| $t_{BW}$ | $\overline{BLE}/\overline{BHE}$ LOW to Write End | 35 | – | 40 | – | ns |
| $t_{SD}$ | Data Setup to Write End | 25 | – | 25 | – | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | – | 0 | – | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High Z[18, 19] | – | 18 | – | 20 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low Z[18] | 10 | – | 10 | – | ns |

### Notes
16. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified $I_{OL}/I_{OH}$ as shown in the AC Test Loads and Waveforms on page 5.
17. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes AN13842 and AN66311. However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
18. At any temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZBE}$ is less than $t_{LZBE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any device.
19. $t_{HZOE}$, $t_{HZCE}$, $t_{HZBE}$, and $t_{HZWE}$ transitions are measured when the outputs enter a high impedance state.
20. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$, $\overline{BLE}$, or both = $V_{IL}$, and $CE_2 = V_{IH}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
21. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to sum of $t_{SD}$ and $t_{HZWE}$.

## Switching Waveforms

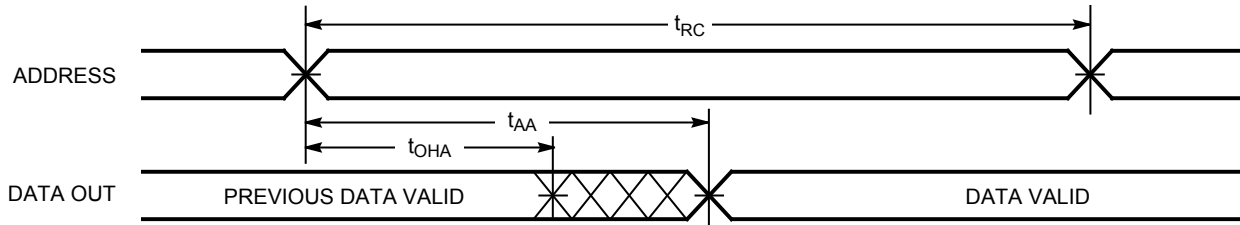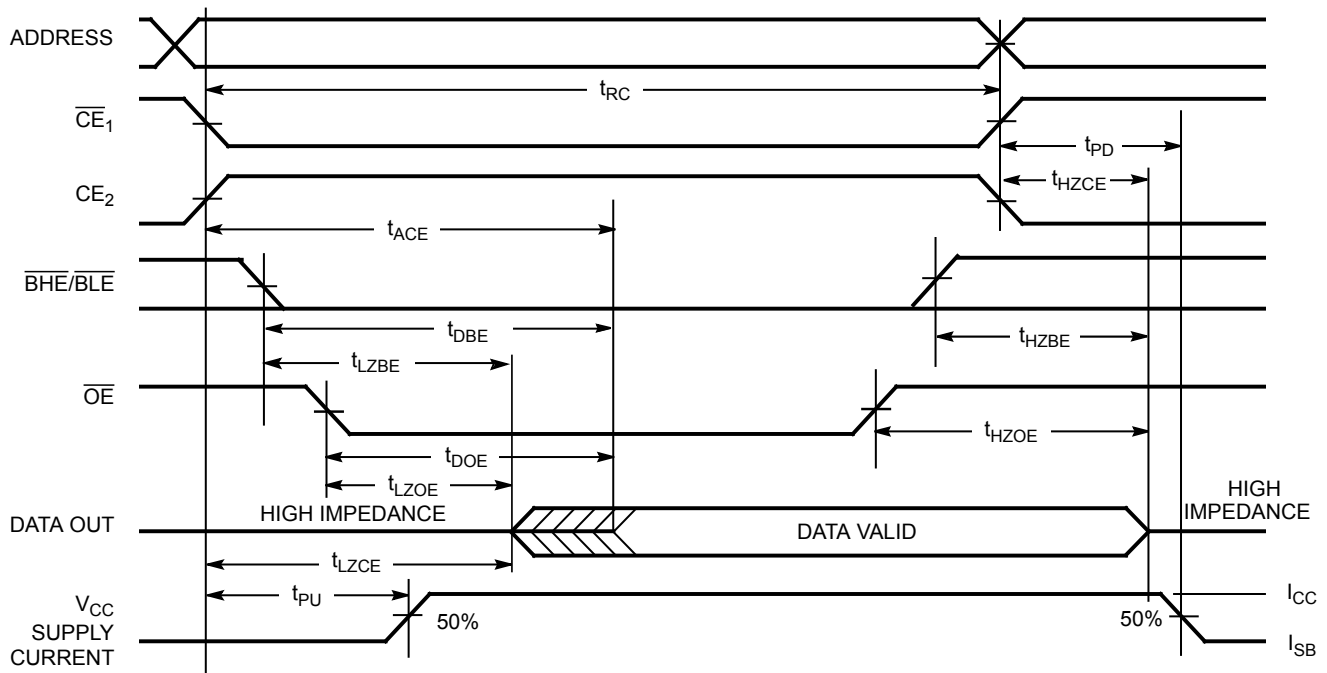**Figure 5. Read Cycle No. 1 (Address Transition Controlled)** [22, 23]



**Figure 6. Read Cycle No. 2 ($\overline{OE}$ Controlled)** [23, 24]
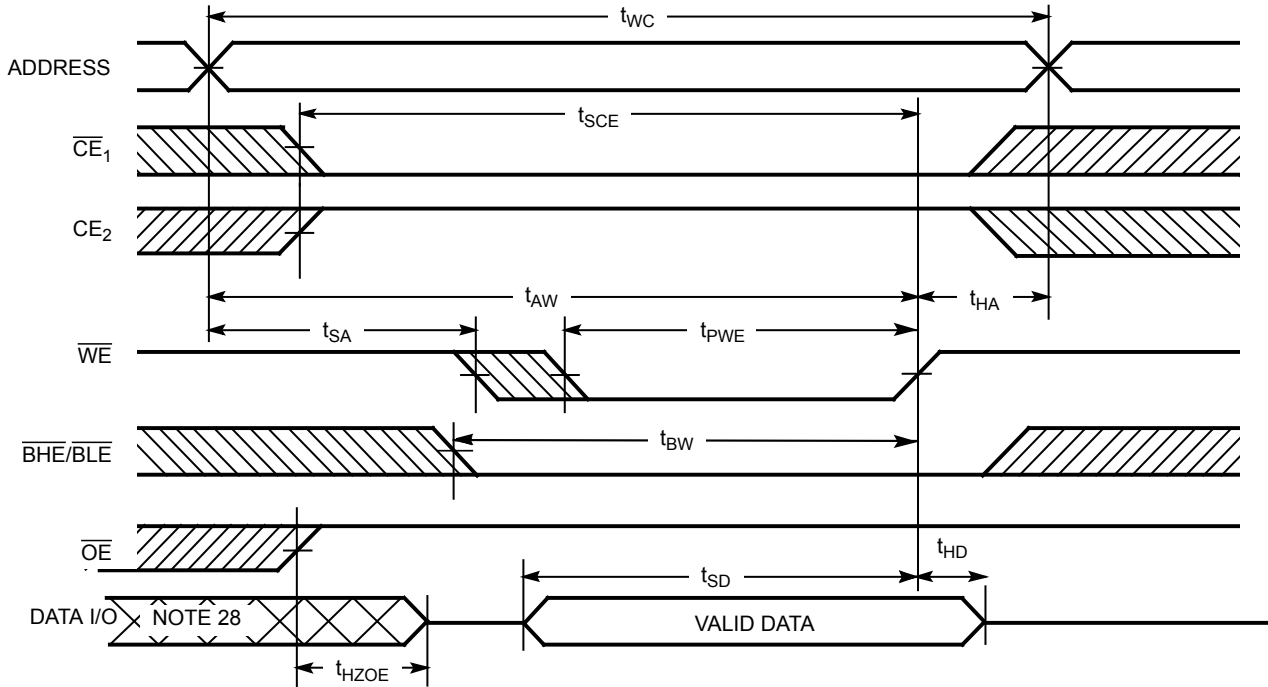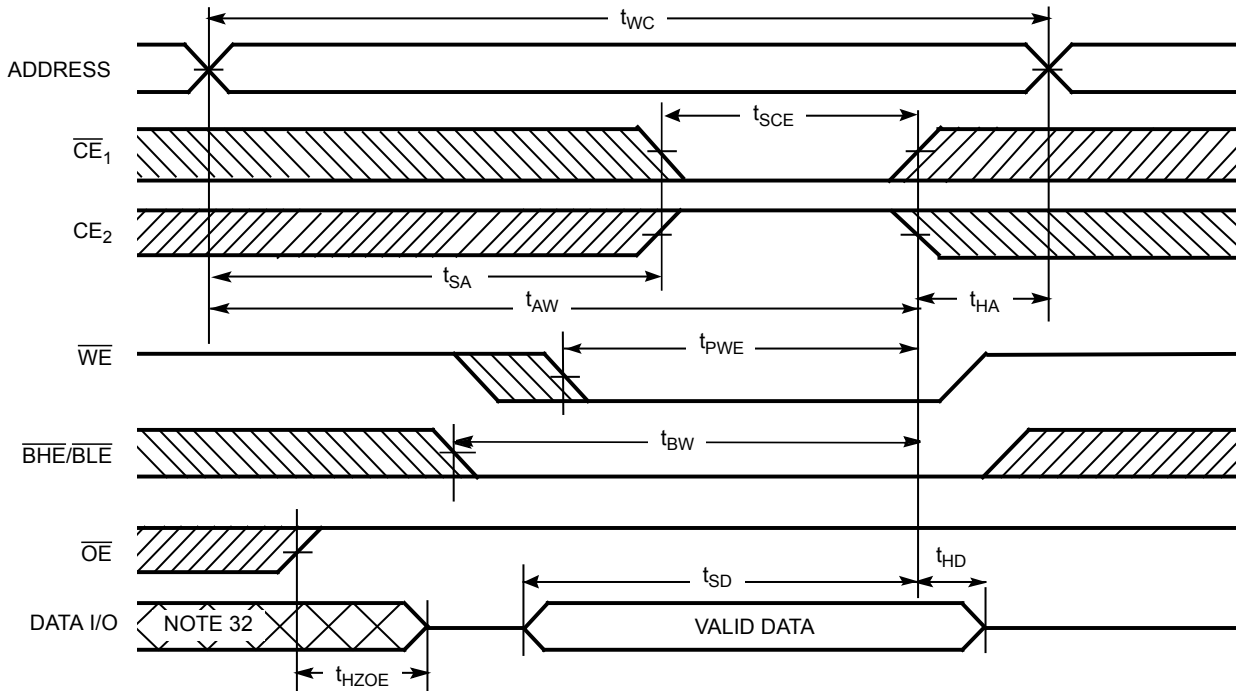


**Notes**
22. The device is continuously selected. $\overline{OE}$, $\overline{CE}_1$ = $V_{IL}$, $\overline{BHE}$, $\overline{BLE}$ or both = $V_{IL}$, and $CE_2$ = $V_{IH}$.
23. $\overline{WE}$ is HIGH for read cycle.
24. Address valid before or similar to $\overline{CE}_1$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and $CE_2$ transition HIGH.

## Switching Waveforms (continued)

### Figure 7. Write Cycle No. 1 ($\overline{WE}$ Controlled) [25, 26, 27]

**Notes**
25. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$, $\overline{BLE}$, or both = $V_{IL}$, and $CE_2 = V_{IH}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
26. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
27. If $\overline{CE}_1$ goes HIGH and $CE_2$ goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
28. During this period, the I/Os are in output state. Do not apply input signals.

## Switching Waveforms (continued)

### Figure 8. Write Cycle No. 2 ($\overline{CE}_1$ or CE$_2$ Controlled) [29, 30, 31]



**Notes**
29. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$, $\overline{BLE}$, or both = $V_{IL}$, and CE$_2 = V_{IH}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
30. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
31. If $\overline{CE}_1$ goes HIGH and CE$_2$ goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
32. During this period, the I/Os are in output state. Do not apply input signals.

## Switching Waveforms (continued)

**Figure 9. Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)** [33, 34]
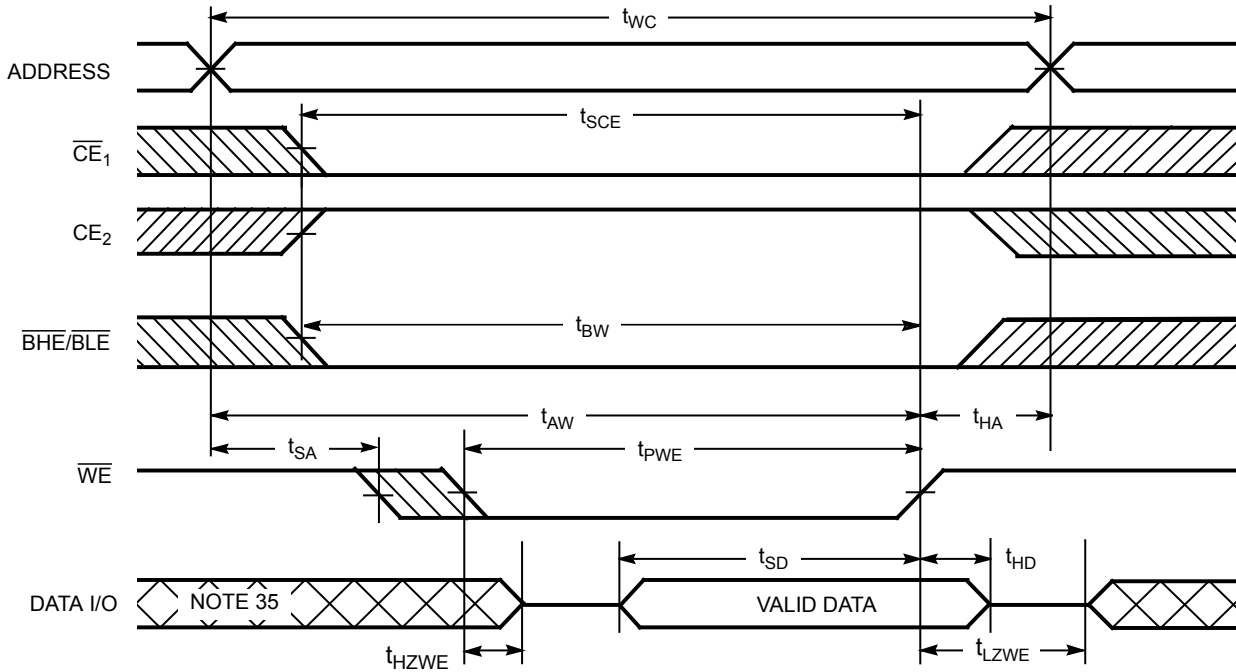


**Figure 10. Write Cycle No. 4 ($\overline{\text{BHE}}/\overline{\text{BLE}}$ Controlled, $\overline{\text{OE}}$ LOW)** [33]
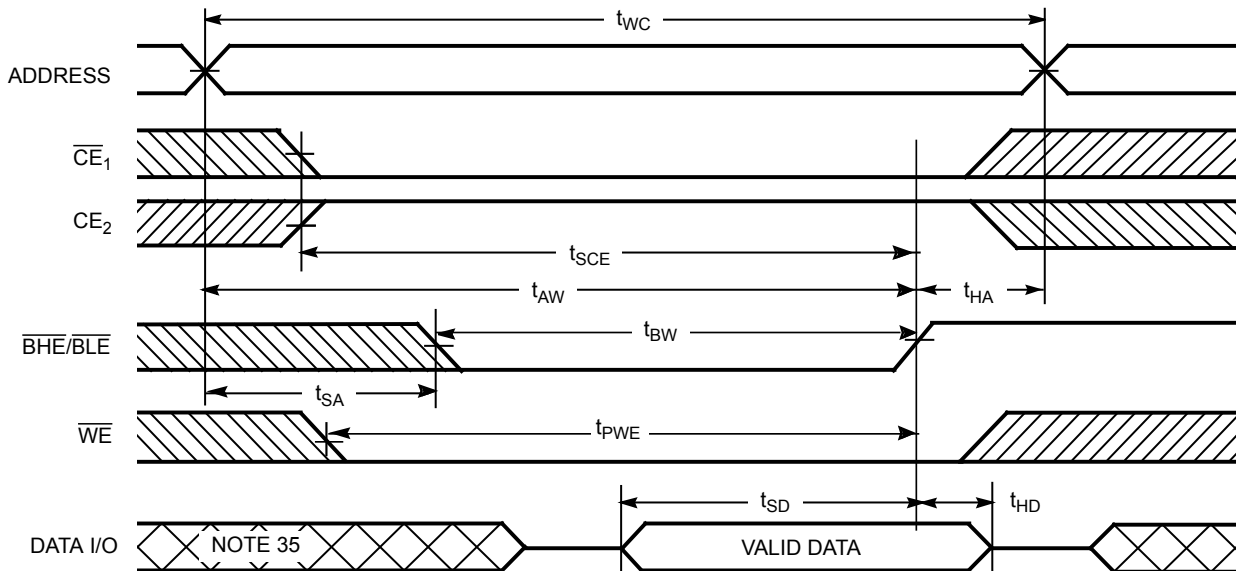


**Notes**
33. If $\overline{\text{CE}}_1$ goes HIGH and $\text{CE}_2$ goes LOW simultaneously with $\overline{\text{WE}}$ = $V_{IH}$, the output remains in a high impedance state.
34. The minimum write cycle pulse width should be equal to sum of $t_{SD}$ and $t_{HZWE}$.
35. During this period, the I/Os are in output state. Do not apply input signals.

## Truth Table

| $\overline{CE}_1$ | $CE_2$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | Inputs/Outputs | Mode | Power |
|---|---|---|---|---|---|---|---|---|
| H | X[36] | X | X | X | X | High Z | Deselect/Power Down | Standby ($I_{SB}$) |
| X[36] | L | X | X | X | X | High Z | Deselect/Power Down | Standby ($I_{SB}$) |
| X[36] | X[36] | X | X | H | H | High Z | Deselect/Power Down | Standby ($I_{SB}$) |
| L | H | H | L | L | L | Data Out ($I/O_0$–$I/O_{15}$) | Read | Active ($I_{CC}$) |
| L | H | H | L | H | L | Data Out ($I/O_0$–$I/O_7$); High Z ($I/O_8$–$I/O_{15}$) | Read | Active ($I_{CC}$) |
| L | H | H | L | L | H | High Z ($I/O_0$–$I/O_7$); Data Out ($I/O_8$–$I/O_{15}$) | Read | Active ($I_{CC}$) |
| L | H | H | H | L | H | High Z | Output Disabled | Active ($I_{CC}$) |
| L | H | H | H | H | L | High Z | Output Disabled | Active ($I_{CC}$) |
| L | H | H | H | L | L | High Z | Output Disabled | Active ($I_{CC}$) |
| L | H | L | X | L | L | Data In ($I/O_0$–$I/O_{15}$) | Write | Active ($I_{CC}$) |
| L | H | L | X | H | L | Data In ($I/O_0$–$I/O_7$); High Z ($I/O_8$–$I/O_{15}$) | Write | Active ($I_{CC}$) |
| L | H | L | X | L | H | High Z ($I/O_0$–$I/O_7$); Data In ($I/O_8$–$I/O_{15}$) | Write | Active ($I_{CC}$) |

**Note**

36. The 'X' (Don't care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

## Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 45 | CY62157ELL-45ZSXI | 51-85087 | 44-pin TSOP Type II (Pb-free) | Industrial |
| 55 | CY62157ELL-55ZSXE | 51-85087 | 44-pin TSOP Type II (Pb-free) | Automotive |
| | CY62157ELL-55BVXE | 51-85150 | 48-ball VFBGA (Pb-free) | |

Contact your local Cypress sales representative for availability of these parts.

## Ordering Code Definitions

CY  621  5  7  E  LL -  XX  XX  X  X

- Temperature Range: X = I or E
  I = Industrial; E = Automotive-E
- Pb-free
- Package Type: XX = ZS or BV
  ZS = 44-pin TSOP II
  BV = 48-ball VFBGA
- Speed Grade: XX = 45 ns or 55 ns
- Low Power
- Process Technology: E = 90 nm
- Bus Width: 7 = × 16
- Density: 5 = 8-Mbit
- Family Code: 621= MoBL SRAM family
- Company ID: CY = Cypress
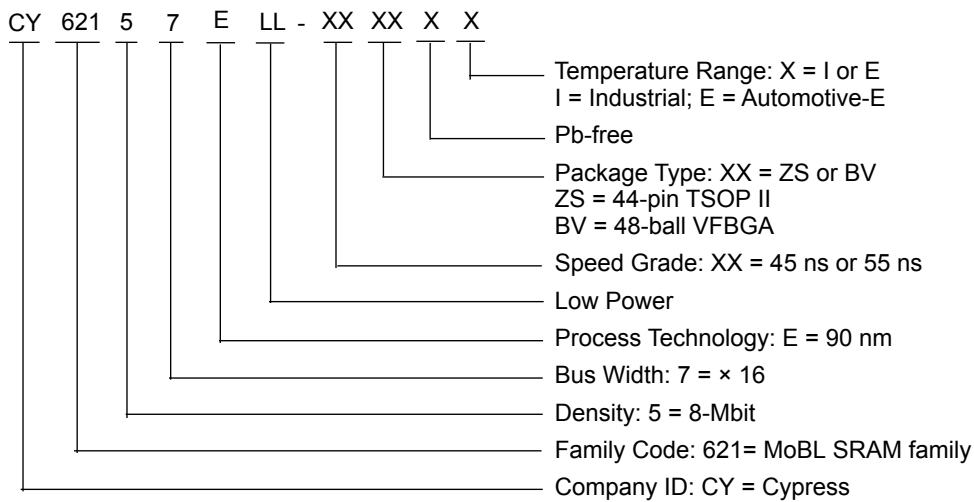
## Package Diagrams

### Figure 11.  48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150
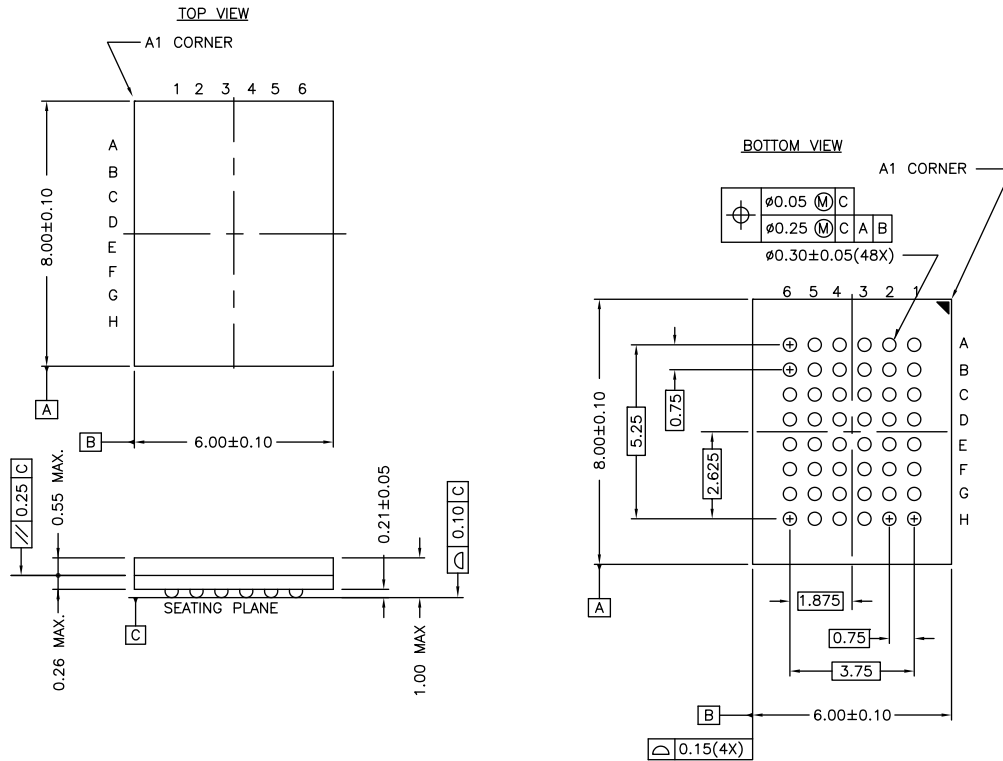


NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

## Package Diagrams (continued)

### Figure 12. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 *E
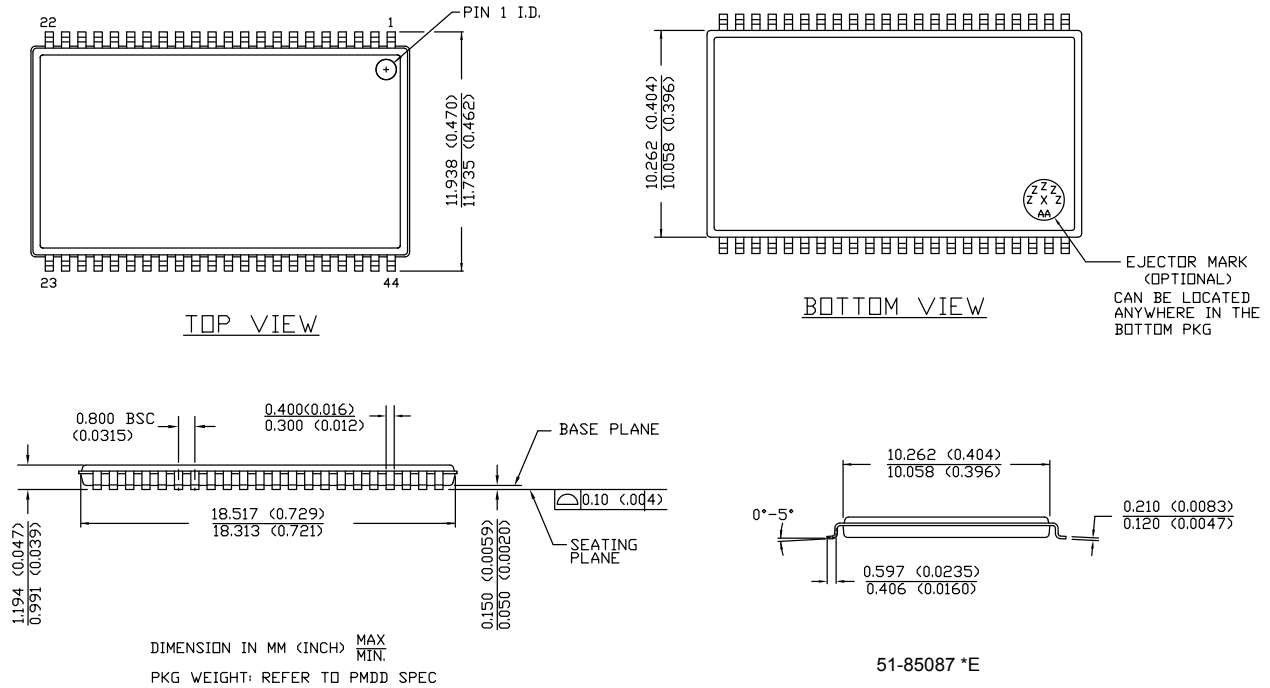
## Acronyms

| Acronym | Description |
|---------|-------------|
| $\overline{CE}$ | Chip Enable |
| CMOS | Complementary Metal Oxide Semiconductor |
| I/O | Input/Output |
| $\overline{OE}$ | Output Enable |
| RAM | Random Access Memory |
| SRAM | Static Random Access Memory |
| TTL | Transistor-Transistor Logic |
| TSOP | Thin Small Outline Package |
| VFBGA | Very Fine-Pitch Ball Grid Array |
| $\overline{WE}$ | Write Enable |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celsius |
| MHz | megahertz |
| µA | microampere |
| µs | microsecond |
| mA | milliampere |
| mm | millimeter |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

## Document History Page

| Document Title: CY62157E MoBL®, 8-Mbit (512 K × 16) Static RAM |
| --- |
| Document Number: 38-05695 |

| Rev. | ECN No. | Issue Date | Orig. of Change | Description of Change |
| --- | --- | --- | --- | --- |
| ** | 291273 | See ECN | PCI | New data sheet. |
| *A | 457689 | See ECN | NXR | Added Automotive Product<br>Removed Industrial Product<br>Removed 35 ns and 45 ns speed bins<br>Removed "L" bin<br>Updated AC Test Loads table<br>Corrected $t_R$ in Data Retention Characteristics from 100 $\mu$s to $t_{RC}$ ns<br>Updated the Ordering Information and replaced the Package Name column with Package Diagram |
| *B | 467033 | See ECN | NXR | Added Industrial Product (Final Information)<br>Removed 48 ball VFBGA package and its relevant information<br>Changed the $I_{CC(typ)}$ value of Automotive from 2 mA to 1.8 mA for f = 1MHz<br>Changed the $I_{SB2(typ)}$ value of Automotive from 5 $\mu$A to 1.8 $\mu$A<br>Modified footnote #4 to include current limit<br>Updated the Ordering Information table |
| *C | 569114 | See ECN | VKN | Added 48 ball VFBGA package<br>Updated Logic Block Diagram<br>Added footnote #3<br>Updated the Ordering Information table |
| *D | 925501 | See ECN | VKN | Added footnote #9 related to $I_{SB2}$ and $I_{CCDR}$<br>Added footnote #14 related AC timing parameters |
| *E | 1045801 | See ECN | VKN | Converted Automotive specs from preliminary to final |
| *F | 2934396 | 06/03/10 | VKN | Added footnote #23 related to chip enable<br>Updated package diagrams<br>Updated template. |
| *G | 3110053 | 12/14/2010 | PRAS | Changed Table Footnotes to Footnotes.<br>Added Ordering Code Definitions. |
| *H | 3269641 | 05/30/2011 | RAME | Removed the note "For best practice recommendations, please refer to the Cypress application note AN1064, SRAM System Guidelines." and its reference in Functional Description.<br>Updated Electrical Characteristics.<br>Updated Data Retention Characteristics.<br>Added Acronyms and Units of Measure.<br>Updated in new template. |
| *I | 4013958 | 06/05/2013 | MEMJ | Updated Functional Description.<br>Updated Electrical Characteristics:<br>Added one more Test Condition "$V_{CC}$ = 5.5 V, $I_{OH}$ = –0.1 mA" for $V_{OH}$ parameter and added maximum value corresponding to that Test Condition.<br>Added Note 8 and referred the same note in maximum value for $V_{OH}$ parameter corresponding to Test Condition "$V_{CC}$ = 5.5 V, $I_{OH}$ = –0.1 mA".<br>Updated Package Diagrams:<br>spec 51-85150 – Changed revision from *F to *H.<br>spec 51-85087 – Changed revision from *C to *E. |
| *J | 4102449 | 08/22/2013 | VINI | Updated Switching Characteristics:<br>Updated Note 17.<br>Updated in new template. |

## Document History Page (continued)

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|---|---|---|---|---|
| Rev. | ECN No. | Issue Date | Orig. of Change | Description of Change |
| *K | 4410589 | 06/17/2014 | VINI | Updated Switching Characteristics: Added Note 21 and referred the same note in "Write Cycle". Updated Switching Waveforms: Added Note 34 and referred the same note in Figure 9. Completing Sunset Review. |
| *L | 4576475 | 11/21/2014 | VINI | Added related documentation hyperlink in page 1. |

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