

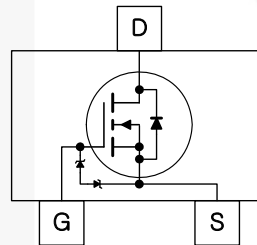
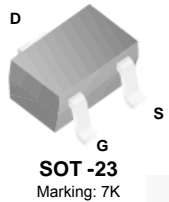


September 2014

# 2N7002K N-Channel Enhancement Mode Field Effect Transistor

## Features

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input / Output Leakage
- Ultra-Small Surface Mount Package
- Pb Free / RoHS Compliant
- ESD HBM = 2000 V (Typical: 3000 V) as per JESD22 A114 and ESD CDM = 2000 V as per JESD22 C101



## Ordering Information

Part Number	Top Mark	Package	Packing Method
2N7002K	7K	SOT-23 3L	Tape and Reel

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain-Source Voltage	60	V
$V_{DGR}$	Drain-Gate Voltage ( $R_{GS} \leq 1.0 \text{ M}\Omega$ )	60	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current	Continuous	300
		Pulsed	800
$T_J$	Operating Junction Temperature Range	-55 to +150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-55 to +150	$^\circ\text{C}$

2N7002K — N-Channel Enhancement Mode Field Effect Transistor

## Thermal Characteristics

Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Value	Unit
$P_D$	Total Power Dissipation	350	mW
	Derate Above $T_A = 25^\circ\text{C}$	2.8	mW/ $^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient <sup>(1)</sup>	350	$^\circ\text{C}/\text{W}$

### Note:

1. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. Minimum land pad size.

## Electrical Characteristics

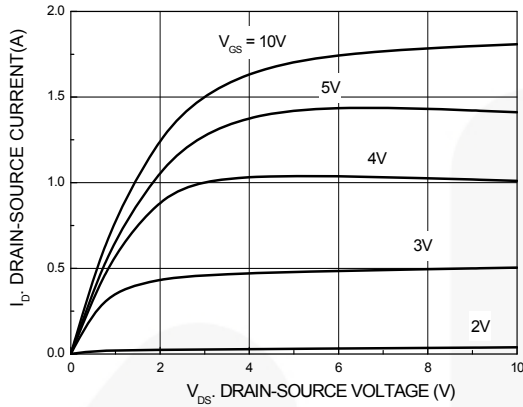
Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Max.	Unit
<b>Off Characteristics<sup>(2)</sup></b>					
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 10\ \mu\text{A}$	60		V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$		1.0	$\mu\text{A}$
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$		500	
$I_{GSS}$	Gate-Body Leakage	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$		$\pm 10$	$\mu\text{A}$
<b>On Characteristics<sup>(2)</sup></b>					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.0	2.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 0.5\text{ A}$		2	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 200\text{ mA}$		4	
$I_{D(ON)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 7.5\text{ V}$	1.5		A
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 0.2\text{ A}$	200		mS
<b>Dynamic Characteristics</b>					
$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$		50	pF
$C_{oss}$	Output Capacitance			15	pF
$C_{rss}$	Reverse Transfer Capacitance			6	pF
<b>Switching Characteristics</b>					
$t_{D(ON)}$	Turn-On Delay Time	$V_{DD} = 30\text{ V}, I_{DSS} = 200\text{ mA}, R_G = 10\ \Omega, V_{GS} = 10\text{ V}$		5	ns
$t_{D(OFF)}$	Turn-Off Delay Time			30	ns

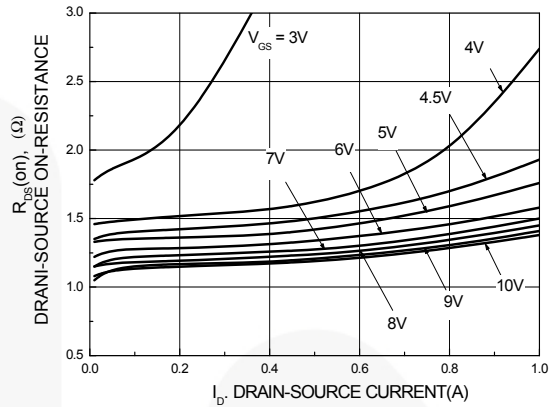
### Note:

2. Short duration test pulse used to minimize self-heating effect.

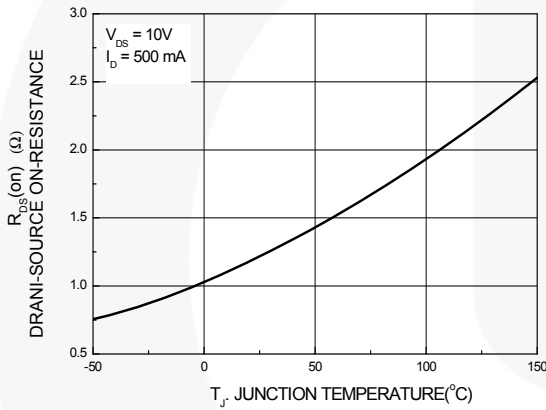
## Typical Performance Characteristics



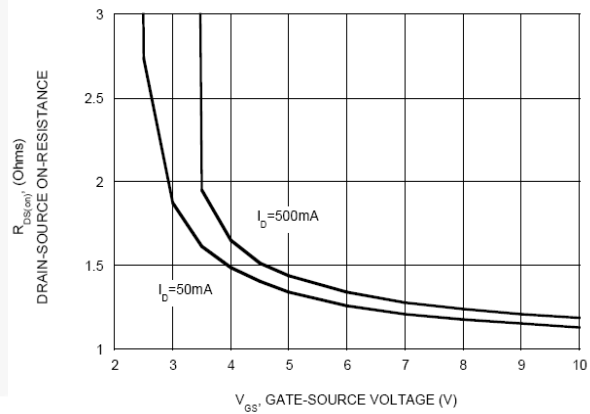
**Figure 1. On-Region Characteristics**



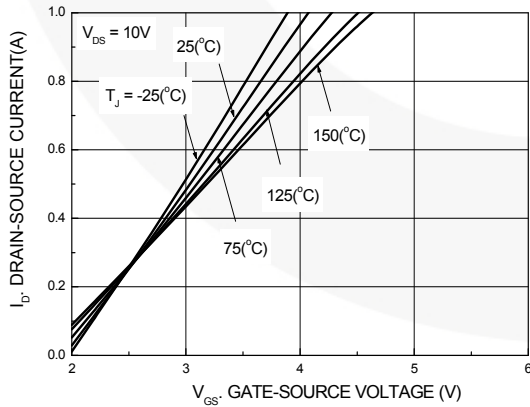
**Figure 2. On-Resistance Variation with Gate Voltage and Drain Current**



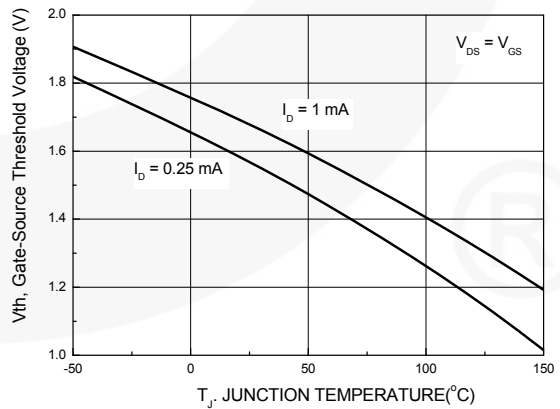
**Figure 3. On-Resistance Variation with Temperature**



**Figure 4. On-Resistance Variation with Gate-Source Voltage**



**Figure 5. Transfer Characteristics**



**Figure 6. Gate Threshold Variation with Temperature**

Typical Performance Characteristics (Continued)

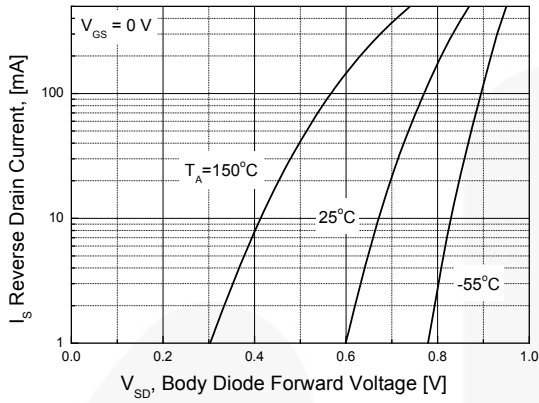


Figure 7. Reverse Drain Current Variation with Diode Forward Voltage and Temperature

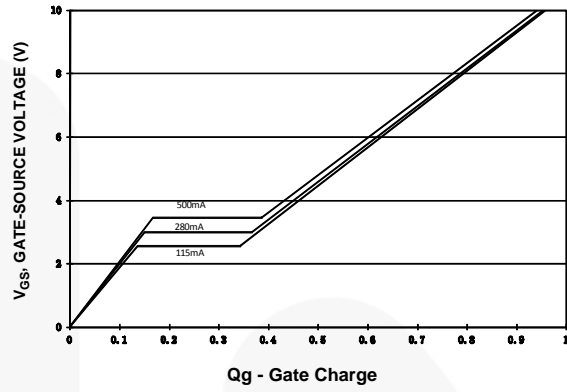


Figure 8. Gate Charge Characteristics

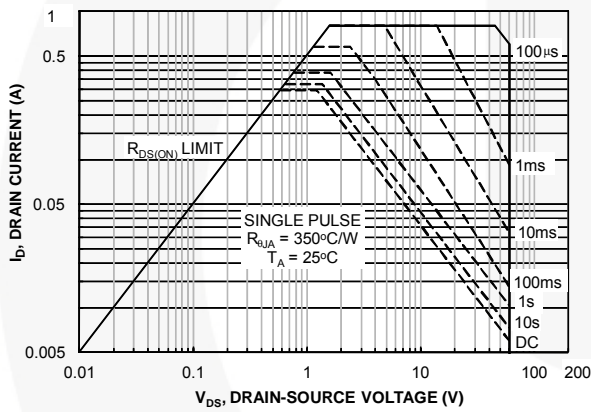


Figure 9. Maximum Safe Operating Area

Physical Dimensions

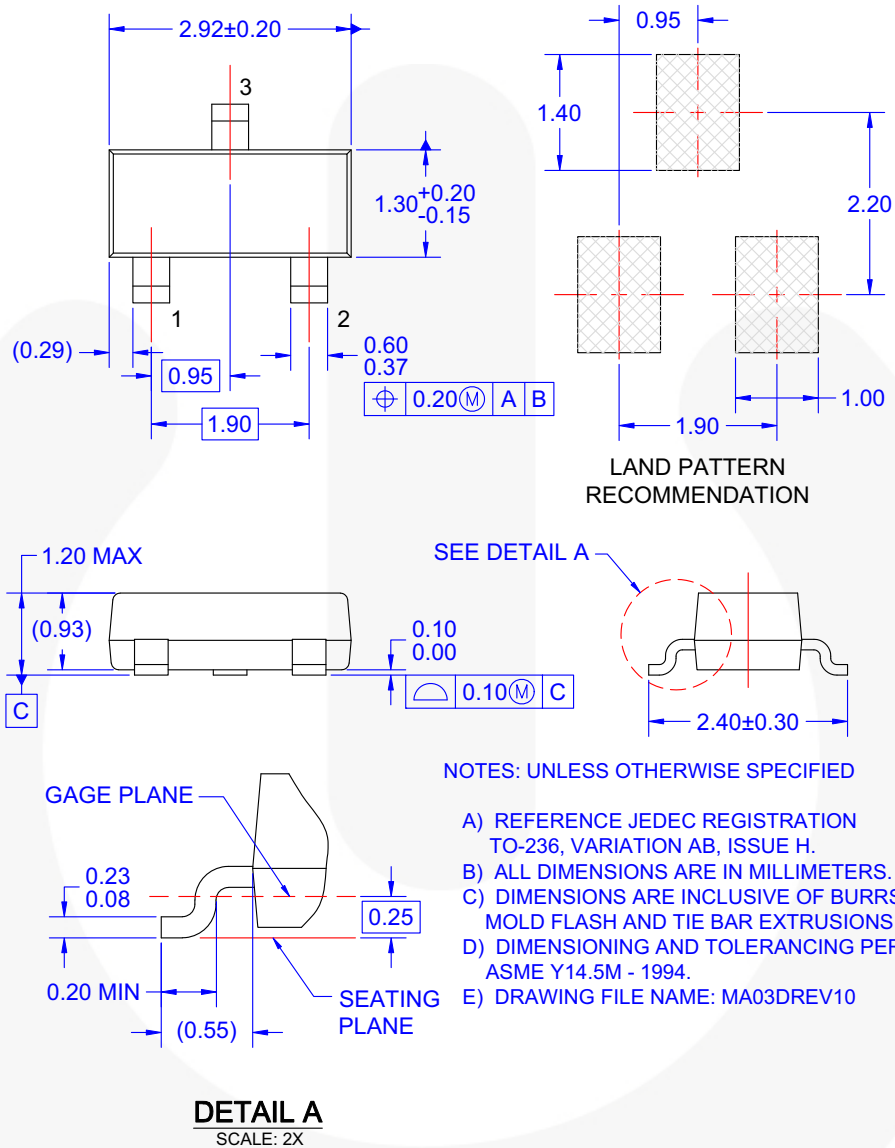


Figure 10. 3-LEAD, SOT23, JEDEC TO-236, LOW PROFILE





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