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October 2014

FAN6208
Secondary-Side Synchronous Rectifier Controller for LLC Topology

Features

- Specialized SR Controller for LLC or LC Resonant Converters
- Secondary-Side Timing Detection with Timing Estimator
- Gate-Shrink Function to Prevent Shoot-Through During Load and Line Transient
- Green-Mode Function for Higher Efficiency at Light-Load Condition
- Programmable Dead Time between Primary-Side Gate Drive Signal and SR Drive Signal
- Advanced Output-Short / Overload Protection Based on the Feedback Information
- Internal Over-Temperature Protection (OTP)
- V_{DD} Pin Over-Voltage Protection (OVP)

Applications

- LCD TV
- PC Power
- Open-Frame SMPS

Description

FAN6208 is a synchronous rectification (SR) controller for isolated LLC or LC resonant converters that can drive two individual SR MOSFETs emulating the behavior of rectifier diodes. FAN6208 measures the SR conduction time of each switching cycle by monitoring the drain-to-source voltage of each SR and determines the optimal timing of the SR gate drive. FAN6208 uses the change of opto-coupler diode current to adaptively shrink the duration of SR gate drive signals during load transients to prevent shoot-through. To improve light-load efficiency, Green-Mode operation is employed, which disables the SR drive signals, minimizing gate drive power consumption at light-load condition.

Optimal timing circuits and protection functions are integrated in an 8-pin SOP package, which allows high-efficiency power supply design with fewer components.

Related Resources

- *FAN6208 Product Folder*

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN6208MY	-40°C to +105°C	8-Pin Small Outline Package (SOP)	Tape & Reel

Application Diagram

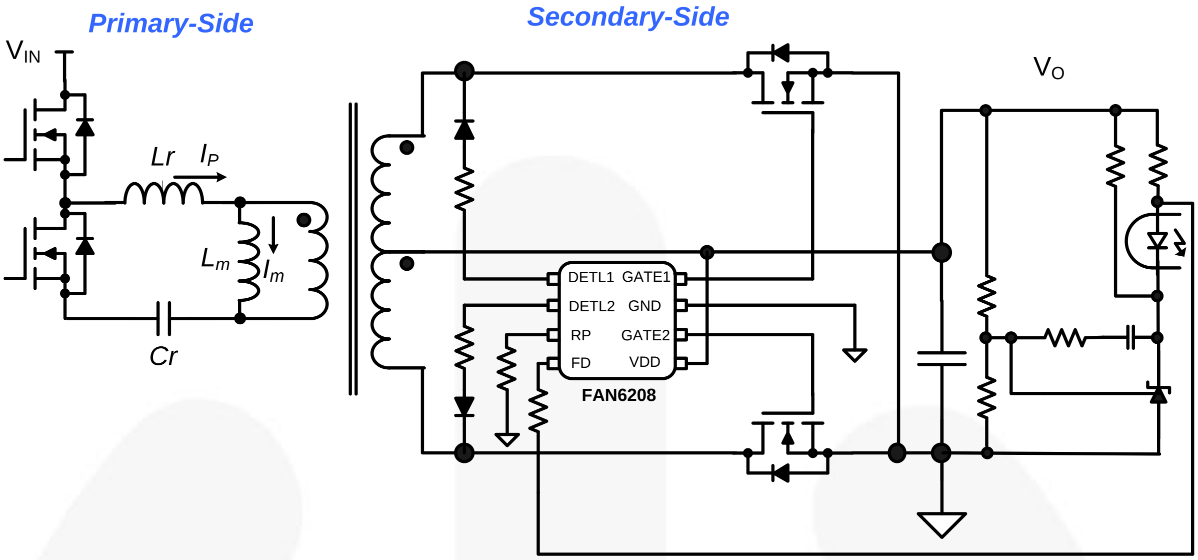

Primary-Side
Secondary-Side
V_IN
Lr
I_P
Lm
Im
Cr
V_O
DETL1
GATE1
DETL2
GND
RP
GATE2
FD
VDD
FAN6208

Figure 1. Typical Application

Block Diagram

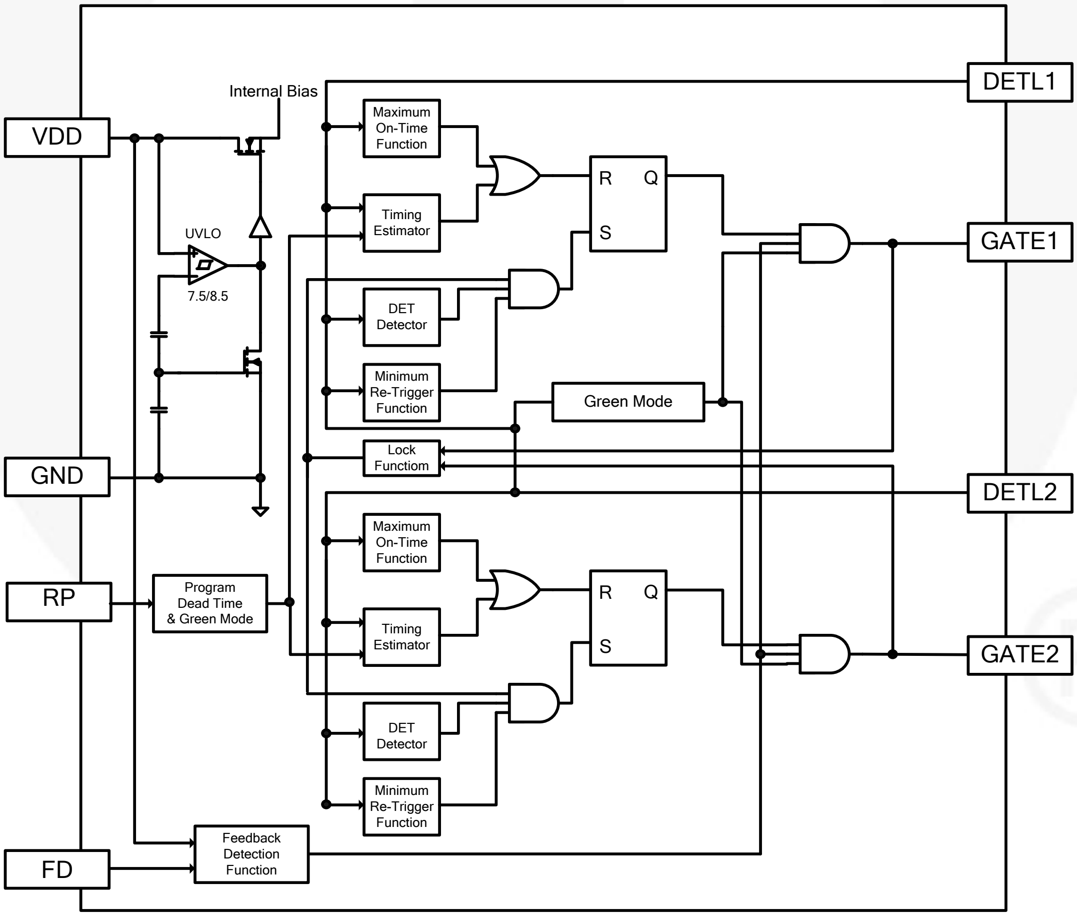
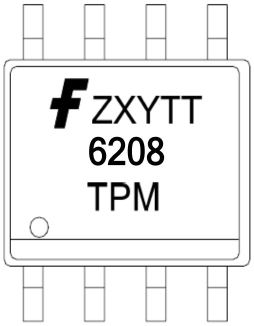

VDD
GND
RP
FD
DETL1
GATE1
DETL2
GATE2
Internal Bias
UVLO
7.5/8.5
Maximum On-Time Function
Timing Estimator
DET Detector
Minimum Re-Trigger Function
Green Mode
Lock Functiom
R
Q
S
Program Dead Time & Green Mode
Feedback Detection Function

Figure 2. Block Diagram

Marking Information



F- Fairchild Logo
Z- Plant Code
X- Year Code
Y- Week Code
TT: Die Run Code
T - Package Type (M = SOP)
P - Y: Green Package
M - Manufacture Flow Code

Figure 3. Top Mark

Pin Configuration

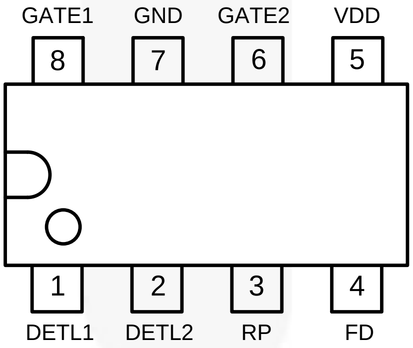


Figure 4. Pin Assignments

Pin Definitions

Pin #	Name	Description
1	DETL1	**Low Detect** provides low-voltage detection of V_{DS} of SR MOSFET1.
2	DETL2	**Low Detect** provides low-voltage detection of V_{DS} of SR MOSFET2.
3	RP	**Dead Time Programming Resistor** programs H/L frequency version and dead time.
4	FD	**Feedback Detection** is used for short-circuit protection and gate shrink.
5	VDD	**Power Supply**
6	GATE2	**Driver Output**. The totem-pole output driver for driving the SR MOSFET2.
7	GND	**Ground**
8	GATE1	**Driver Output**. The totem-pole output driver for driving the SR MOSFET1.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage		30	V
V_{FD}	Voltage on FD Pin		30	V
V_{LV}	Voltage on DETL1, DETL2, RP Pins	-0.3	7.0	V
P_D	Power Dissipation	350 mW at T_A=90°C	1000 mW at T_A=25°C	
Θ_{JA}	Junction–to-Ambient Thermal Resistance		130	°C/W
Ψ_{JT}	Junction-to-Top Thermal Characteristics		45	°C/W
T_J	Operating Junction Temperature	Internally Limited		°C
T_{STG}	Storage Temperature Range	-55	+150	°C
T_L	Lead Temperature (Wave Soldering or IR, 10 Seconds)		+260	°C
ESD	Human Body Model, JESD22-A114		6	kV
	Charged Device Model, JESD22-C101		2	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Operating Ambient Temperature	-40	+105	°C

Electrical Characteristics

V_{DD}=20 V, T_A=25°C, unless otherwise specified. All voltages are with respect to GND unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD Section						
V_{DD}	DC Supply Voltage		$V_{TH\text{-}OFF}$		28	V
$I_{DD\text{-}OP1}$	Operating Current	V_{DD}=12 V, DETL=50 KHz, C_L=6 nF, R_{RP}=24 KΩ	7.0	8.5	10.0	mA
$I_{DD\text{-}OP2}$	Operating Current	V_{DD}=12 V, DETL=100 KHz	2.4	3.2	4.0	mA
$I_{DD\text{-}ST}$	Startup Current	V_{DD}=8 V	180	300	500	μA
$V_{TH\text{-}ON1}$ $V_{TH\text{-}ON2}$	On Threshold Voltage		9.3	9.7	10.1	V
$V_{TH\text{-}OFF1}$ $V_{TH\text{-}OFF2}$	Off Threshold Voltage		8.3	8.8	9.3	V
$V_{DD\text{-}OVP1}$ $V_{DD\text{-}OVP2}$	V_{CC} Over-Voltage Protection		26	27	28	V
$V_{DD\text{-}OVP\text{-}HYS1}$ $V_{DD\text{-}OVP\text{-}HYS2}$	V_{CC} Over-Voltage Protection Hysteresis		1.3	1.8	2.3	V
t_{OVP1},t_{OVP2}	V_{CC} Over-Voltage-Protection Debounce		30	60	100	μs
DETL Section						
V_{DETL1} V_{DETL2}	Threshold Voltage for LOW Detection of DETL	V_{DD}=12 V, DETL=50 KHz, C_L=6 nF, R_{RP}=24 KΩ	1.7	2.0	2.3	V
$t_{SR\text{-}ON\text{-}DETL1}$ $t_{SR\text{-}ON\text{-}DETL2}$	Delay from DETL LOW to SR Gate Turn-On	t_{DB}+ t_{PD}+ t_R	300	350	400	ns
$V_{DETL\text{-}FLOATING1}$ $V_{DETL\text{-}FLOATING2}$	DETL Floating Voltage	V_{DD}=12 V, DETL Pin Floating	4.5			V
$I_{DETL\text{-}SOURCE1}$ $I_{DETL\text{-}SOURCE2}$	DETL Source Current	V_{DETL1}=0 V	40	50	60	μA
$t_{DETL\_Green\_LF1}$ $t_{DETL\_Green\_LF2}$	DETL LOW Time Threshold for Green Mode at Low-Frequency Operation	V_{RP} < 1.5 V	3.50	3.75	4.00	μs
$t_{DET(L)\_Green\_HF1}$ $t_{DET(L)\_Green\_HF2}$	DETL LOW Time Threshold for Green Mode at High-Frequency Operation	V_{RP} > 1.5 V	1.75	1.90	2.05	μs
Thermal Shutdown						
$T_{SHUTDOWN}$	Shutdown Temperature	Temperature Rising, V_{DD}=15 V		140		˚C
	Hysteresis			20		
$T_{STARTUP}$	Startup Temperature	Before Startup		120		

Continued on the following page…

Electrical Characteristics

V_{DD}=20 V, T_A=25°C, unless otherwise specified. All voltages are with respect to GND unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Gate Section						
V_{Z1} V_{Z2}	Gate Output Voltage Maximum (Clamping)	V_{DD}=20 V	10	12	14	V
V_{OL1} V_{OL2}	Gate Output Voltage LOW	V_{DD}=12 V; I_O=100 mA			0.5	V
$V_{OH1}V_{OH2}$	Gate Output Voltage HIGH	V_{DD}=12 V; I_O=100 mA	9			V
t_{R1} t_{R2}	Rising Time	V_{DD}=12 V; C_L=6 nF; V_{GATE}=2 V to 9 V	30	70	120	ns
t_{F1} t_{F2}	Falling Time	V_{DD}=12 V; C_L=6 nF; V_{GATE}=9 V to 2 V	30	50	70	ns
$t_{PD\_HIGH\_DETL1}$ $t_{PD\_HIGH\_DETL2}$	Propagation Delay to Gate Output HIGH (DETL Trigger)	t_R: 0 V~2 V, V_{DD}=12 V (DET Floating)		120		ns
$t_{PD\_LOW\_ DETL1}$ $t_{PD\_LOW\_ DETL2}$	Propagation Delay to Gate Output LOW (DETL Trigger)	t_F: 100%~90%, V_{DD}=12 V (DET Floating)		120		ns
t_{ON_MAX1} t_{ON_MAX2}	Maximum On-Time	Trim Maximum On-Time	9.0	10.5	12.0	μs
$t_{INHIBIT\_LF1}$ $t_{INHIBIT\_LF2}$	Gate Inhibit Time (from Turn-Off to Next Turn-On)	V_{RP} < 1.5 V	1.8	2.1	2.5	μs
$t_{INHIBIT\_HF1}$ $t_{INHIBIT\_HF2}$	Gate Inhibit Time (from Turn-Off to Next Turn-On)	V_{RP} > 1.5 V	1.25	1.45	1.70	μs
$t_{BLANKING1}$ $t_{BLANKING2}$	Blanking Time for SR Turn-Off Triggered by DETL High (Minimum On-Time)			300		ns
K_R	Gate ON-Time Increase Rate Between Two Consecutive Cycles	t_{ON}(n) / t_{ON}(n-1) %		140		%
Timing Estimator Section						
t_{DW}	Detection Window for Insufficient Dead Time (from Gate Turn-Off to DETL HIGH)		80	125	150	ns
$t_{SHRINK-DT}$	Gate Shrink Time by Insufficienct Dead Time	R_{RP}=20 KΩ, t_{DETL}=5 μs	1.00	1.25	1.50	μs
t_{DEAD}	Dead Time by Timing Estimator (70 kHz ~ 140 kHz, V_{RP} < 1.5 V)	t_{DETL}=4 μs, R_{RP}=20 KΩ	210	300	390	ns
		t_{DETL}=6 μs, R_{RP}=20 KΩ	570	720	870	
	Dead Time by Timing Estimator (160kHz ~ 240 kHz, V_{RP} > 1.5V)	t_{DETL}=2.5 μs, R_{RP}=43 KΩ	220	320	420	
		t_{DETL}=3.8 μs, R_{RP}=43 KΩ	560	670	780	
t_{DB}	DETL HIGH-to-LOW Debounce Time for Gate Turn-on Trigger			150		ns
$t_{SHRINK-RNG}$	Gate Shrink by DETL Ringing around Zero			1.2		μs
t_{Green_DH}	DETL Pull-HIGH Time Threshold for Green Mode		18	24	30	μs

Continued on the following page…

Electrical Characteristics

V_{DD}=20 V, T_A=25°C, unless otherwise specified. All voltages are with respect to GND unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Feedback Detection (FD) Section						
ΔV1% ΔV2%	Feedback Increase Threshold for Gate Shrink	$[(V_{DD}-V_{FD})_{n+1}/(V_{DD}-V_{FD})_n]$		120		%
$t_{SHRINK-FD}$	Gate Shrink by Feedback Detection			1.4		µs
$t_{D-SHRINK-FD}$	Gate-Shrink Duration by Feedback Detection		60	90	120	µs
$V_{DD}-V_{FD.SCP}$	Short-Circuit Protection (SCP) Threshold by Feedback Detection		200	270	340	mV
t_{DB-SCP}	Debounce Time for Short-Circuit Protection (SCP)		12	16	20	µs
RP Section						
I_{RP}	RP Source Current		38.5	41.5	44.5	µA
V_{RPO}	RP Open Protect		3.40	3.65	3.90	V
V_{RPS}	RP Short Protect		0.25	0.30	0.35	V
t_{RPOS}	RP Open/Short Debounce		1.6	2.0	2.4	µs
V_{RPHL}	H/L Frequency Threshold		1.40	1.46	1.52	V

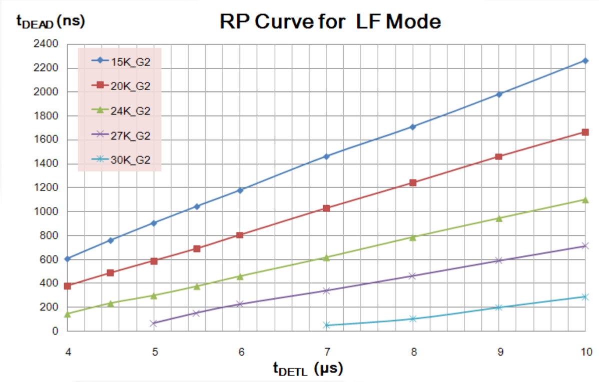


Figure 5. t_{DEAD} vs. t_{DETL} RP Curve for LF Mode

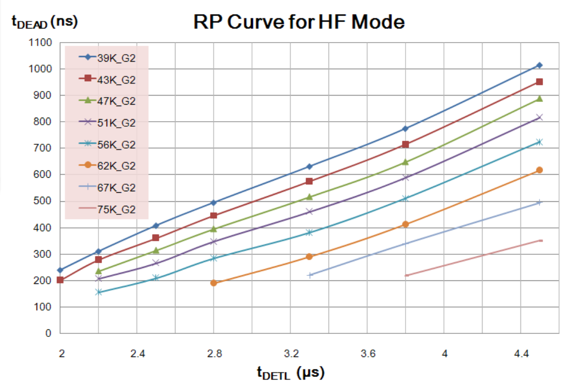


Figure 6. t_{DEAD} vs. t_{DETL} RP Curve for HF Mode

Function Description

Operation Principle

FAN6208 is a secondary-side synchronous rectifier controller for LLC or LC resonant converters that drive two synchronous rectifier MOSFETs. Figure 7 is the simplified circuit diagram of an LLC converter. The FAN6208 determines SR MOSFET turn-on/off timing by detecting the drain-to-source voltage of each SR MOSFET. The key waveforms for LLC resonant converter for below resonance and above resonance are shown in Figure 8 and Figure 9, respectively.

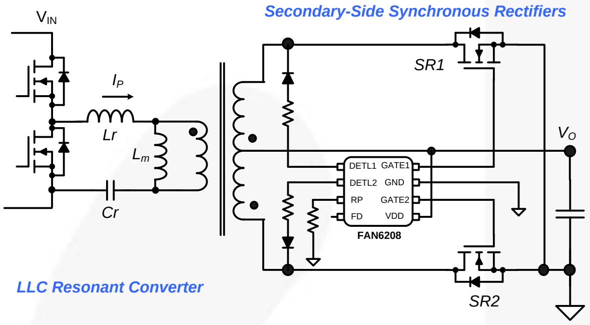


Figure 7. Simplified Schematic of LLC Converter

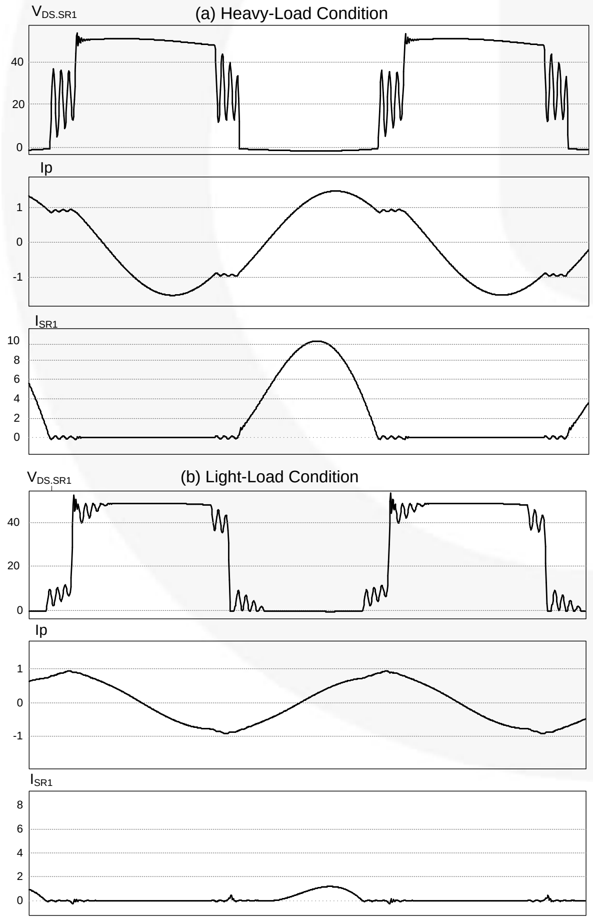


Figure 8. Key Waveforms of LLC Resonant Converter for Below Resonance Operation

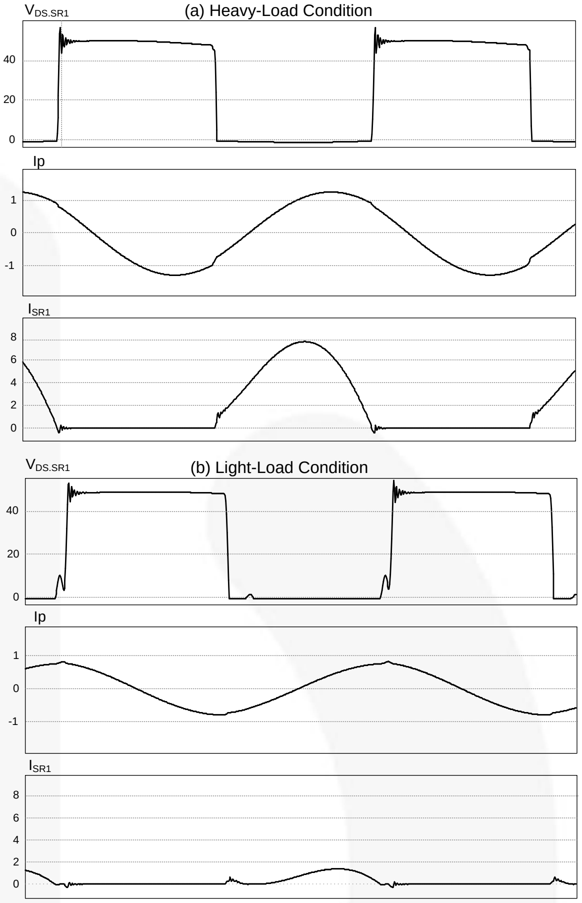


Figure 9. Key Waveforms of LLC Resonant Converter for Above Resonance Operation

Timing Estimator

Figure 10 shows the timing diagram for FAN6208. Once the body diode of SR begins conducting, the drain-to-source voltage drops to zero, which causes DETL pin voltage to drop to zero. FAN6208 turns on the MOSFET after $t_{ON\text{-}ON\text{-}DETL}$ (about 350 ns), when voltage on DETL drops below 2 V. As depicted in Figure 11, the turn-on delay (after $t_{SR\text{-}ON\text{-}DETL}$) is the sum of debounce time (150 ns) and propagation delay (200 ns).

FAN6208 measures the SR conduction duration (t_{DETL}), during which DETL stays lower than 2 V, and uses this information to determine the turn-off instant of SR gates of the next switching cycle. The turn-off timing is obtained by subtracting a dead time (t_{DEAD}) from the measured SR conduction duration of the previous switching cycle. The dead time can be programmed using a resistor on the RP pin and the relationship between the dead time and SR conduction duration (t_{DETL}) for different resistor values on RP pin is given in Figure 5.

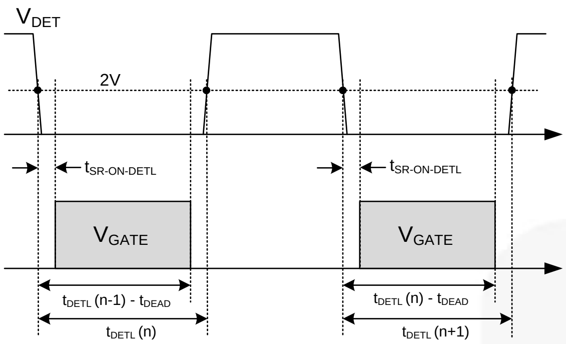

V_{DET}
2V
$t_{SR\text{-}ON\text{-}DETL}$
$t_{SR\text{-}ON\text{-}DETL}$
V_{GATE}
V_{GATE}
t_{DETL} (n-1) - t_{DEAD}
t_{DETL} (n)
t_{DETL} (n) - t_{DEAD}
t_{DETL} (n+1)

Figure 10.SR Gate Timing Diagram

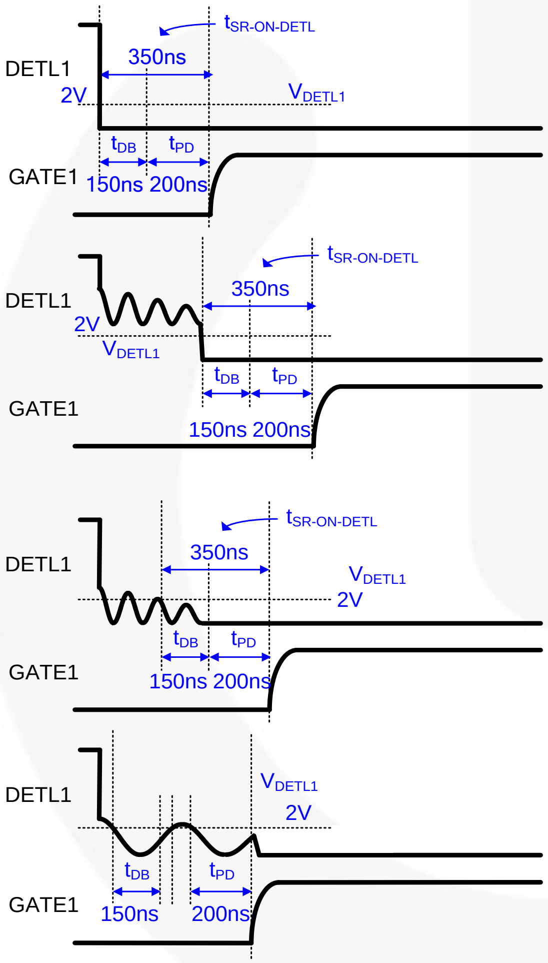

DETL1
GATE1
$t_{SR\text{-}ON\text{-}DETL}$
350ns
2V
V_{DETL1}
t_{DB}
t_{PD}
150ns
200ns

Figure 11.DETL Debounce (Blanking) Time

Gate-Shrink Functions

In normal operation, the turn-off instant is determined by subtracting a dead time (t_{DEAD}) from the measured SR conduction duration of the previous switching cycle, as shown in Figure 10. This allows proper driving timing for SR MOSFETS when the converter is in steady state and the switching frequency does not change much. However, this control method may cause shoot-through of SR MOSFETs when the switching frequency increases fast and switching transition of the primary-side MOSFETs takes place before the turn-off command of SR is given. To prevent the shoot-through, FAN6208 has gate-shrink functions. Gate shrink occurs under three conditions:

(a) When insufficient dead time is detected in the previous switching cycle. When the DETL goes HIGH within 125 ns of detection window after SR gate is turned off, the SR gate drive signal in the next switching cycle is reduced by $t_{SHRINK\text{-}DT}$ (about 1.25 µs) to increase the dead time, as shown in Figure 12.

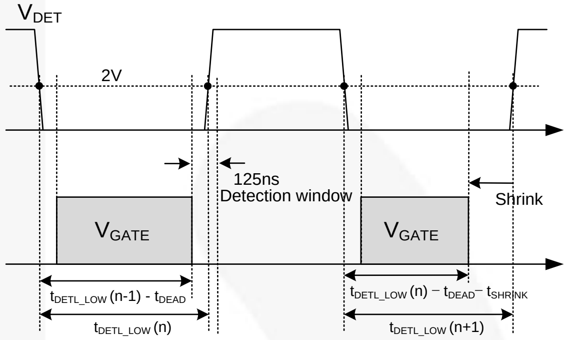

V_{DET}
2V
125ns
Detection window
Shrink
V_{GATE}
V_{GATE}
t_{DETL_LOW} (n-1) - t_{DEAD}
t_{DETL_LOW} (n)
t_{DETL_LOW} (n) − t_{DEAD}− t_{SHRINK}
t_{DETL_LOW} (n+1)

Figure 12.Gate Shrink by Minimum Dead Time Detection Window

(b) When the feedback information changes fast. FAN6208 monitors the current through the opto-coupler diode by measuring the voltage across the resistor in series with the opto-coupler diode, as depicted in Figure 13. If the feedback current through the opto-coupler diode increases by more than 20% of the feedback current of the previous switching cycle, the SR gate signal is shrunk by $t_{SHRINK\text{-}FD}$ (about 1.4 µs) for $t_{D\text{-}SHRINK\text{-}FD}$ (about 90 µs), as shown in Figure 14.

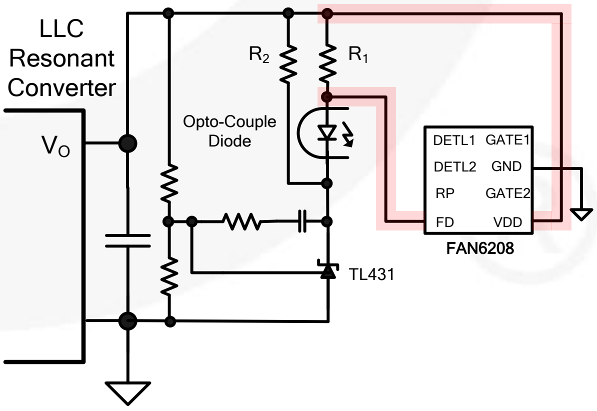

LLC
Resonant
Converter
V_O
R_2
R_1
Opto-Couple
Diode
TL431
DETL1
GATE1
DETL2
GND
RP
GATE2
FD
VDD
FAN6208

Figure 13.Typical Application Circuit

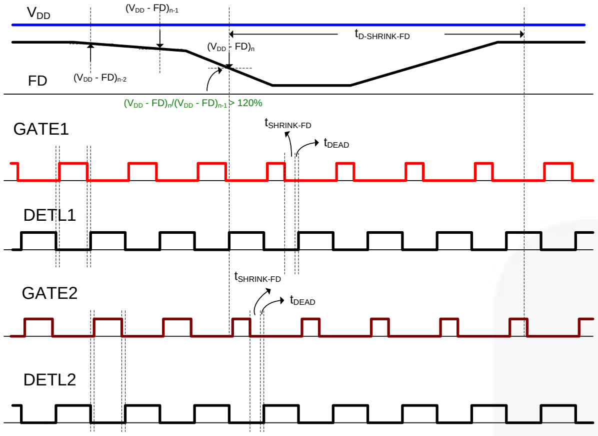

VDD
(VDD - FD)n-1
tD-SHRINK-FD
(VDD - FD)n
FD
(VDD - FD)n-2
(VDD - FD)n/(VDD - FD)n-1 > 120%
GATE1
tSHRINK-FD
tDEAD
DETL1
GATE2
tSHRINK-FD
tDEAD
DETL2

Figure 14. Gate Shrink by Feedback Detection

(c) When the DETL voltage has ringing around zero. As depicted in Figure 8, the drain voltage of SR has ringing around zero at light-load condition after the switching transition of the primary-side switches. When DETL voltage rises above 2 V within 350 ns after DETL voltage drops to zero and stays above 2 V longer than 150 ns, the gate is shrunk by 1.2 µs ($t_{SHRINK-RNG}$), as shown in Figure 15.

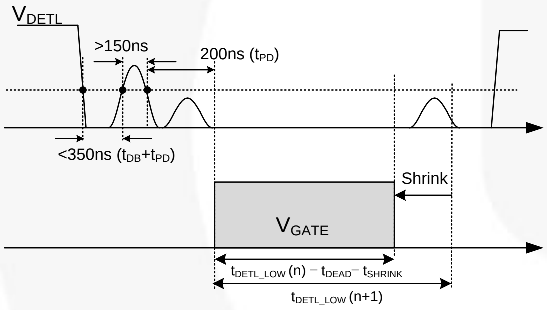

VDETL
>150ns
200ns (tPD)
<350ns (tDB+tPD)
Shrink
VGATE
tDETL_LOW (n) – tDEAD– tSHRINK
tDETL_LOW (n+1)

Figure 15. Gate Shrink by DETL Voltage Ringing Around Zero

RP Pin Function

The RP pin programs the level of green mode and t_{DEAD}. Figure 16 shows how the mode is selected by the voltage on the RP pin (open protection, short protection, and HF/LF mode). When R_{RP} is less than 36 KΩ, FAN6208 operates in low-frequency mode. Green mode is enabled when t_{DETL} is smaller than 3.75 µs. When R_{RP} is larger than 36 KΩ, high-frequency mode is selected and green mode is enabled for t_{DETL} < 1.90 µs. t_{DEAD} can be also adjusted by a resistor on the RP pin. Figure 5 shows the relationship between t_{DEAD} and t_{DETL} for different RP resistors.

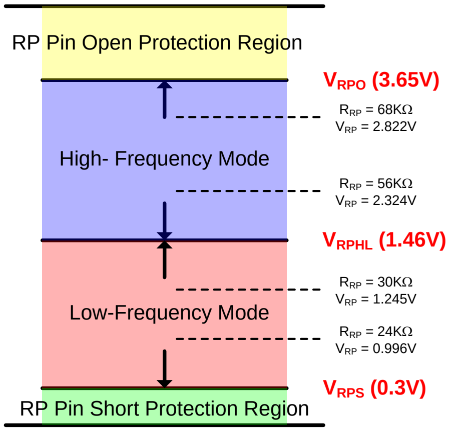

RP Pin Open Protection Region
VRPO (3.65V)
RRP = 68KΩ
VRP = 2.822V
High- Frequency Mode
RRP = 56KΩ
VRP = 2.324V
VRPHL (1.46V)
RRP = 30KΩ
VRP = 1.245V
Low-Frequency Mode
RRP = 24KΩ
VRP = 0.996V
VRPS (0.3V)
RP Pin Short Protection Region

Figure 16. RP Pin Operation

To handle abnormal conditions for IC pins, the RP pin also provides open/short protection. When V_{RP} is less than V_{RPS} (0.3 V) or V_{RP} is higher than V_{RPO} (3.65 V), the protection is triggered. Figure 17 shows the RP pin short protection timing sequence. If $V_{RP} < V_{RPS}$ (0.3 V) for longer than t_{RPOS} (2 µs), FAN6208 is disabled. Figure 18 shows the RP pin open protection timing sequence. If $V_{RP} > V_{RPO}$ (3.65 V) for longer than t_{RPOS} (2 µs), FAN6208 is disabled.

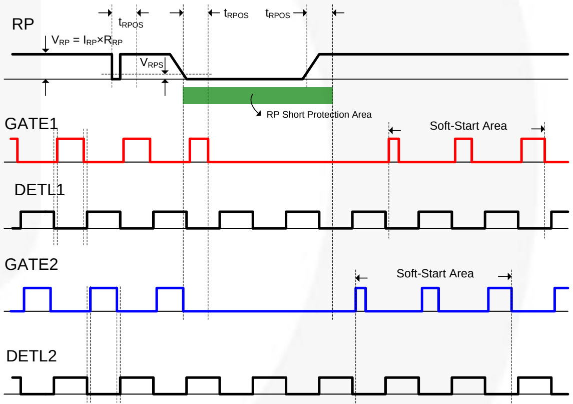

RP
tRPOS
tRPOS
tRPOS
VRP = IRP×RRP
VRPS
RP Short Protection Area
GATE1
Soft-Start Area
DETL1
GATE2
Soft-Start Area
DETL2

Figure 17. RP Pin Short Protection

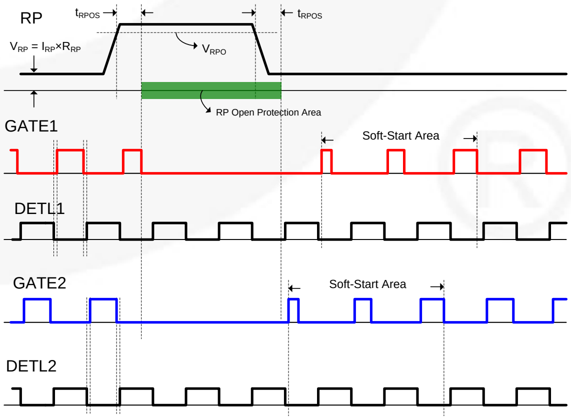

RP
tRPOS
tRPOS
VRP = IRP×RRP
VRPO
RP Open Protection Area
GATE1
Soft-Start Area
DETL1
GATE2
Soft-Start Area
DETL2

Figure 18. RP Pin Open Protection

Green Mode

Switching frequency increases in LLC topology at light-load condition, which increases the power consumption for the SR gate drive. Green mode reduces power loss at light load. FAN6208 has two ways to enable green mode. Green mode is triggered when DETL voltage is pulled LOW for less than 3.75 µs (LF mode) or 1.90 µs (HF mode) for seven switching cycles. FAN6208 resumes normal SR gate driving when DETL voltage is pulled LOW for longer than 3.75 µs (LF mode) or 1.90 µs (HF mode) for seven switching cycles.

When DETL voltage is pulled HIGH for longer than 24 µs. This occurs when the LLC resonant converter operates in burst mode (skipping mode).

Short-Circuit Protection

As depicted in Figure 13, FAN6208 monitors the current through the opto-coupler diode by measuring the voltage across the resistor in series with the opto-coupler diode. When the output of the power supply is short circuited, the output voltage drops and the cathode of the shunt regulator (KA431) is saturated to HIGH. No current flows through the opto coupler diode. The output short protection is triggered when the voltage between V_{DD} and FD is smaller than 0.3 V, as shown in Figure 19.

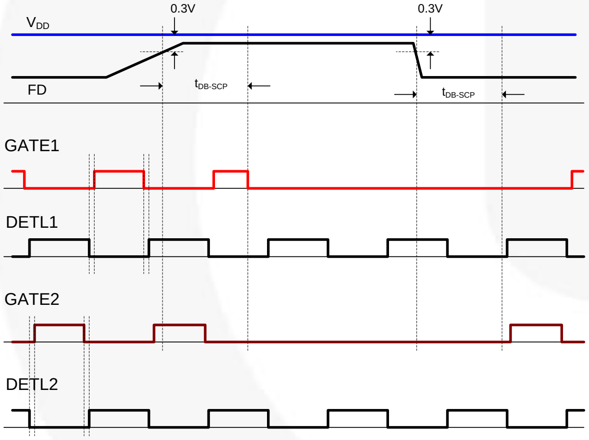


Figure 19. Output Short Protection by Feedback Detection

V_{DD} Pin Over-Voltage Protection

Over-voltage conditions are usually caused by an open feedback loop. V_{DD} over-voltage protection prevents damage of SR MOSFET. When the voltage on the V_{DD} pin exceeds 27 V, FAN6208 disables gate output.

Internal Over-Temperature Protection

Internal over-temperature protection prevents the SR gate from fault triggering in high temperatures. If the temperature is over 140°C, the SR gate is disabled until the temperature drops below 120°C.

Typical Performance Characteristics

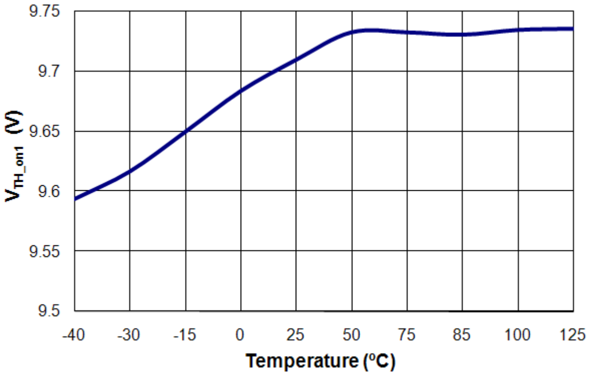


Figure 20. V_{TH_ON1} vs. T_A

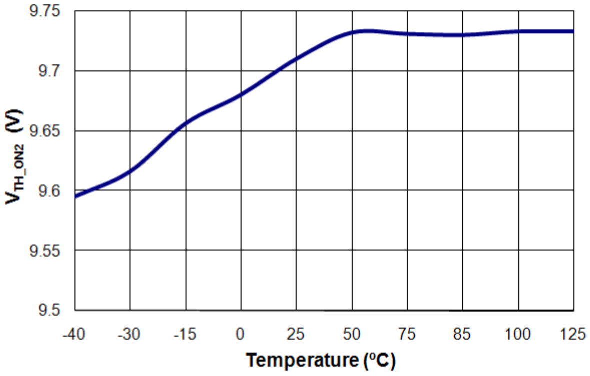


Figure 21. V_{TH_ON2} vs. T_A

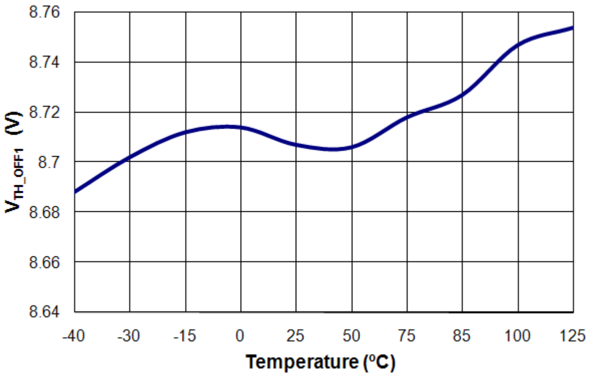


Figure 22. V_{TH_OFF1} vs. T_A

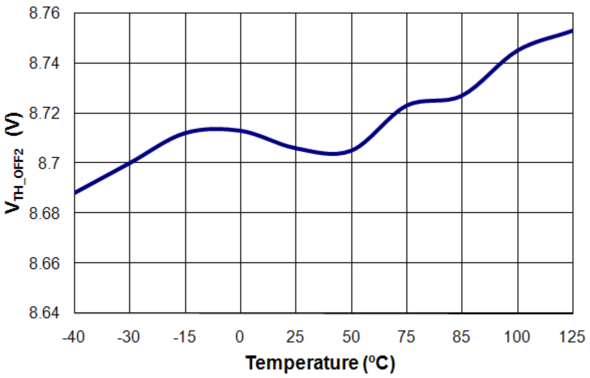


Figure 23. V_{TH_OFF2} vs. T_A

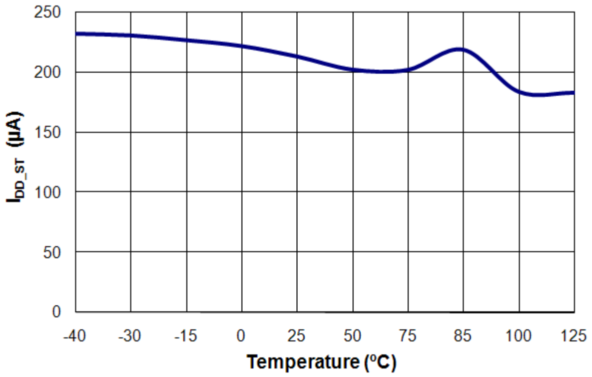


Figure 24. I_{DD_ST} vs. T_A

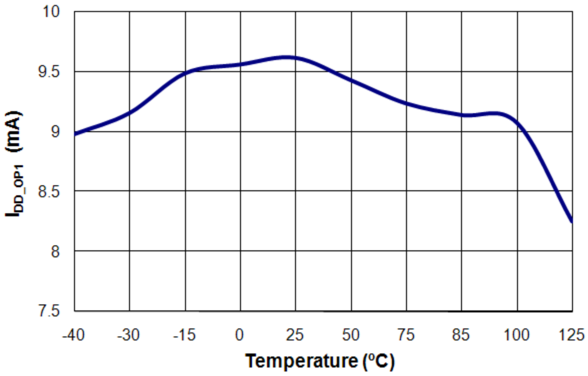


Figure 25. I_{DD_OP1} vs. T_A

Typical Performance Characteristics (Continued)

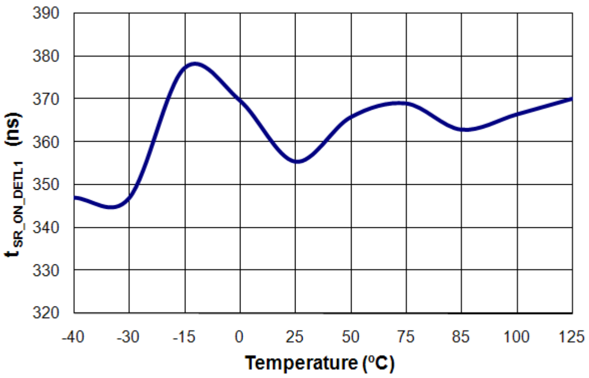


Figure 26. $t_{SR\_ON\_DETL1}$ vs. T_A

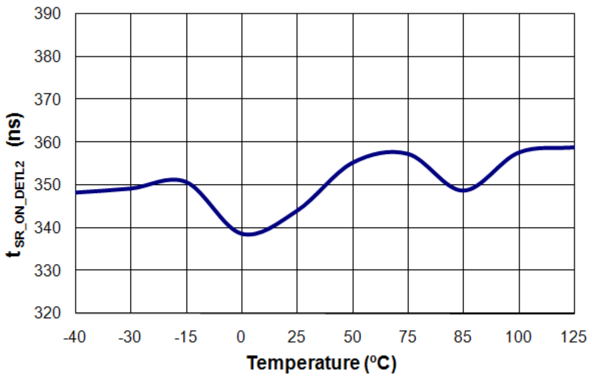


Figure 27. $t_{SR\_ON\_DETL2}$ vs. T_A

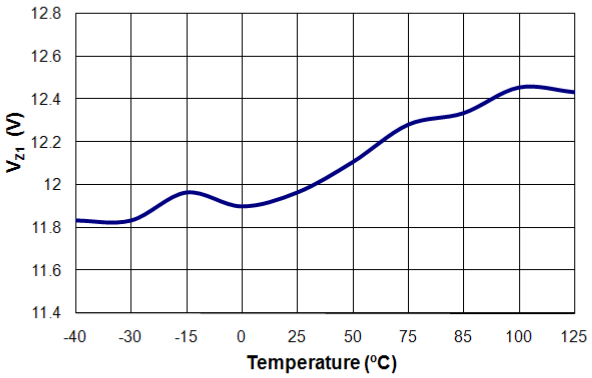


Figure 28. V_{Z1} vs. T_A

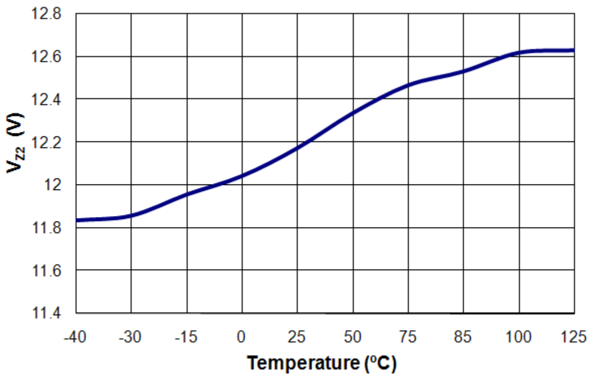


Figure 29. V_{Z2} vs. T_A

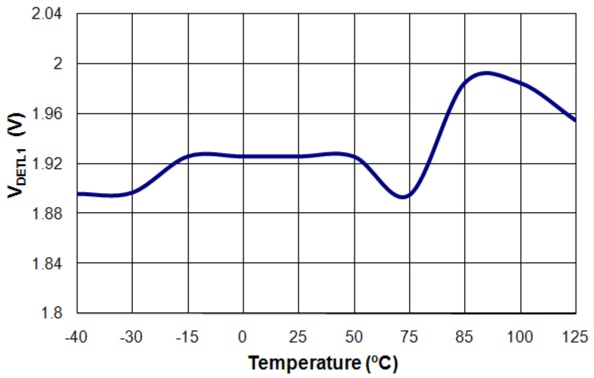


Figure 30. V_{DETL1} vs. T_A

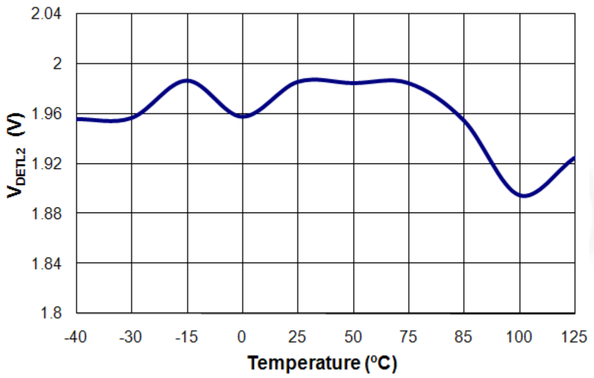


Figure 31. V_{DETL2} vs. T_A

Typical Performance Characteristics (Continued)

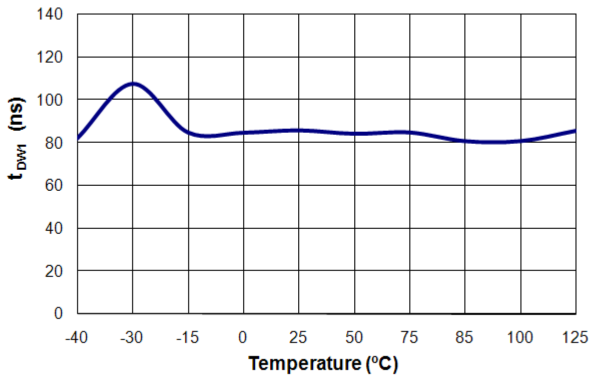


Figure 32. t_{DW1} vs. T_A

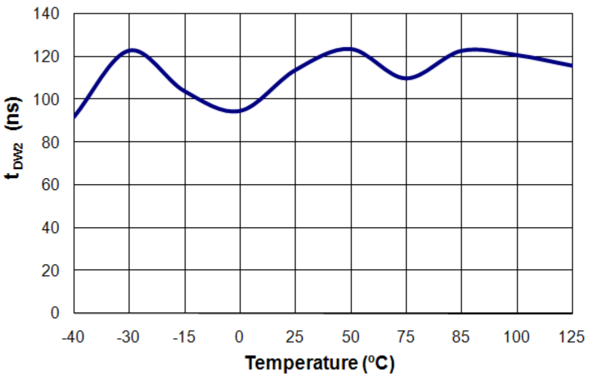


Figure 33. t_{DW2} vs. T_A

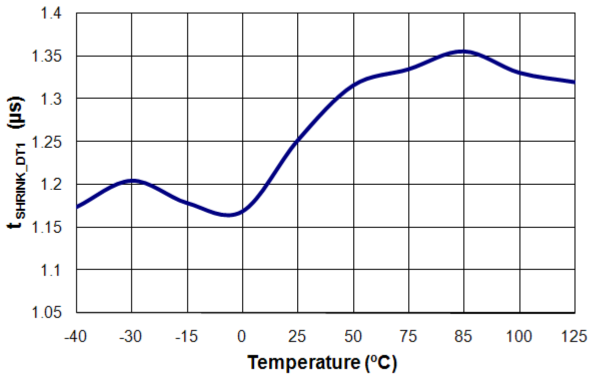


Figure 34. V_{SHRINK_DT1} vs. T_A

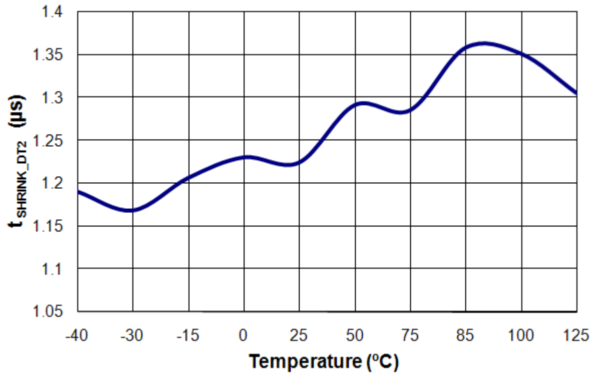


Figure 35. V_{SHRINK_DT2} vs. T_A

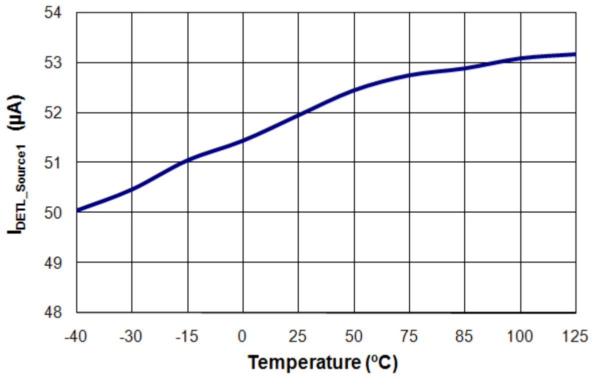


Figure 36. $I_{DETL\_Source1}$ vs. T_A

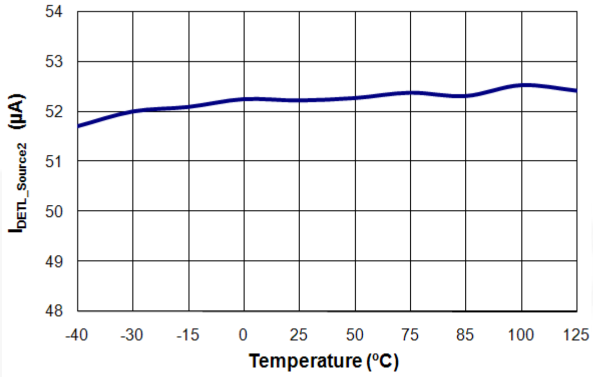


Figure 37. $I_{DETL\_Source2}$ vs. T_A

Typical Performance Characteristics (Continued)

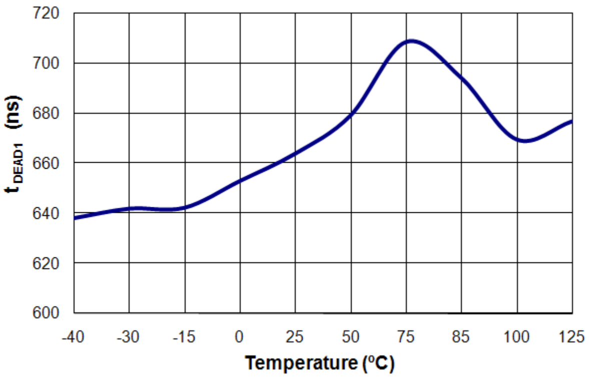


Figure 38. t_{DEAD1} (R_{RP}=20 k, 6 µs) vs. T_A

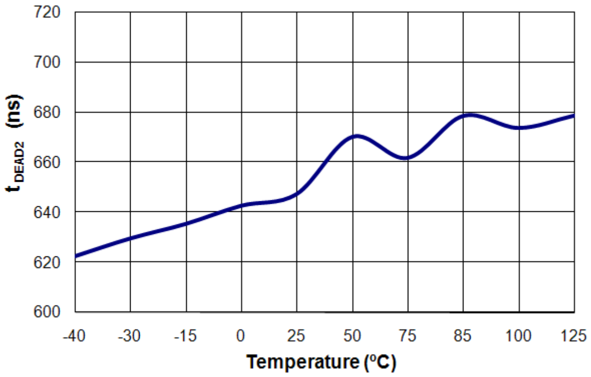


Figure 39. t_{DEAD2} (R_{RP}=20 k, 6 µs) vs. T_A

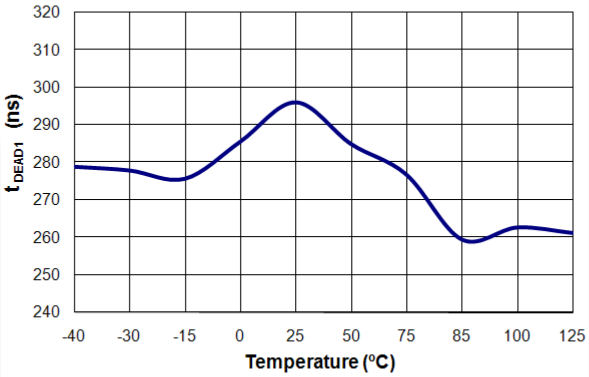


Figure 40. t_{DEAD1} (R_{RP}=43 k, 2.5 µs) vs. T_A

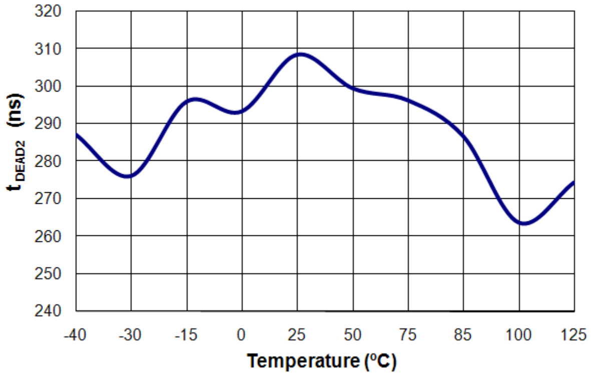


Figure 41. t_{DEAD2} (R_{RP}=43 k, 2.5 µs) vs. T_A

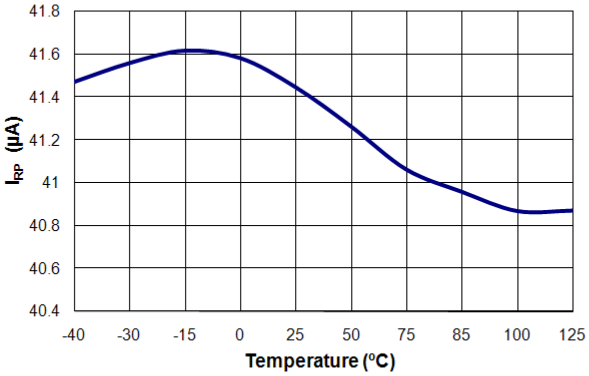


Figure 42. I_{RP} vs. T_A

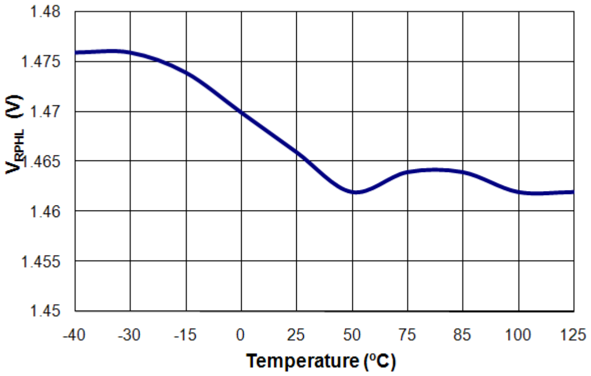
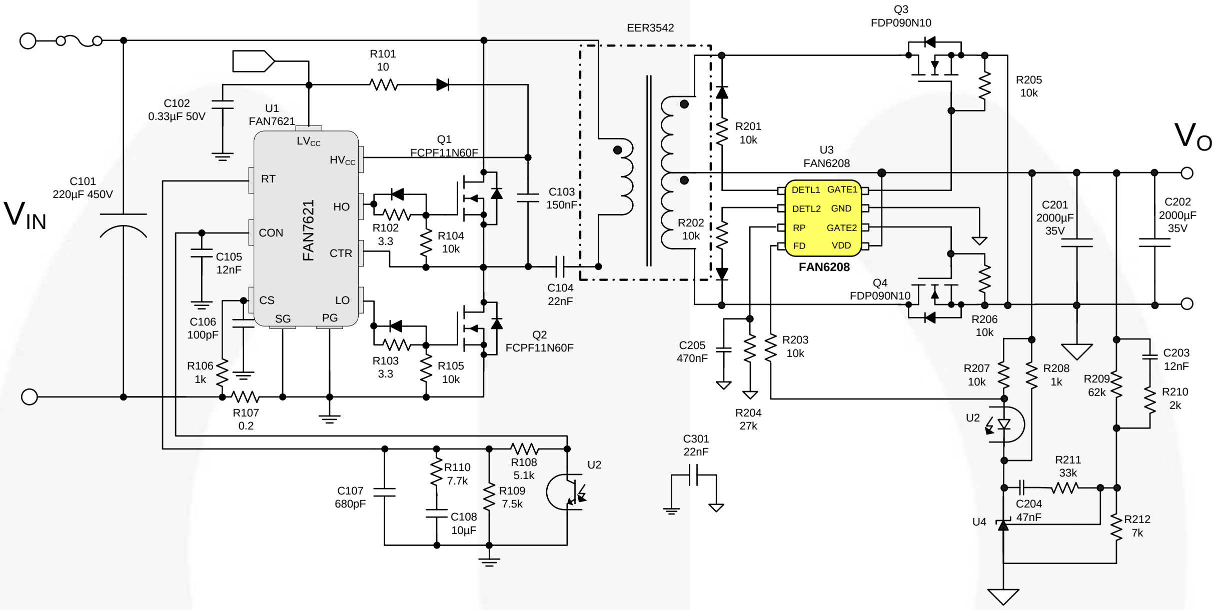


Figure 43. V_{RPHL} vs. T_A

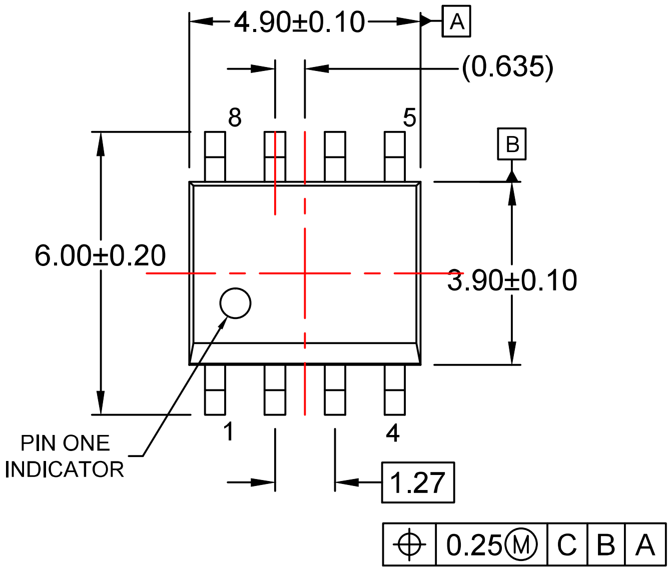
Typical Application Circuit (LLC Converter with SR)

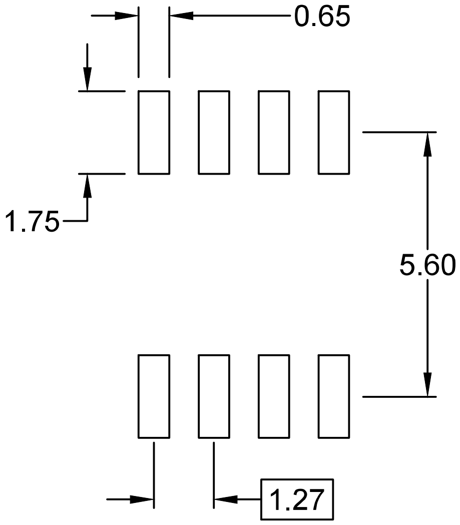
Application	Fairchild Devices	Input Voltage Range	Output
TV Power	FAN7621 FAN6208	350~400 V_{DC}	24 V / 8 A



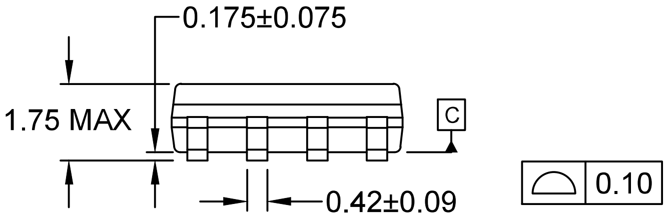
V_{IN}
C101
220µF 450V
C102
0.33µF 50V
U1
FAN7621
R101
10
LV_{CC}
HV_{CC}
RT
CON
HO
CTR
CS
LO
SG
PG
FAN7621
Q1
FCPF11N60F
R102
3.3
R104
10k
C103
150nF
C104
22nF
C105
12nF
C106
100pF
R103
3.3
R105
10k
Q2
FCPF11N60F
R106
1k
R107
0.2
C107
680pF
R110
7.7k
C108
10µF
R108
5.1k
R109
7.5k
U2
EER3542
C301
22nF
Q3
FDP090N10
R205
10k
R201
10k
R202
10k
U3
FAN6208
DETL1
GATE1
DETL2
GND
RP
GATE2
FD
VDD
FAN6208
Q4
FDP090N10
R206
10k
C205
470nF
R203
10k
R204
27k
V_O
C201
2000µF
35V
C202
2000µF
35V
C203
12nF
R207
10k
R208
1k
R209
62k
R210
2k
U2
R211
33k
C204
47nF
U4
R212
7k

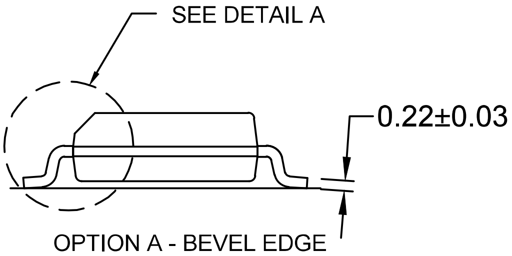
Figure 44. Application Circuit


4.90±0.10
A
(0.635)
8
5
B
6.00±0.20
3.90±0.10
PIN ONE
INDICATOR
1
4
1.27
0.25 M | C | B | A

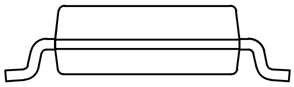

0.65
1.75
5.60
1.27

LAND PATTERN RECOMMENDATION

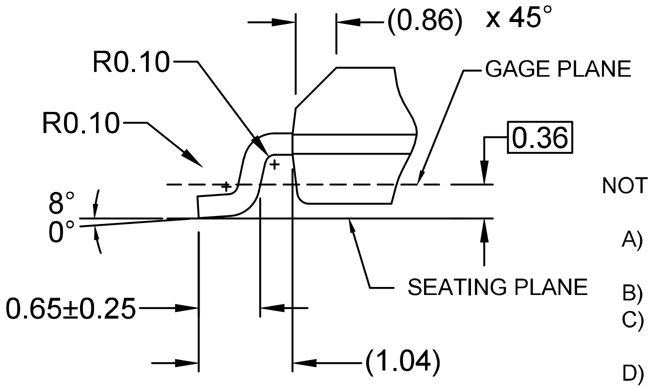

0.175±0.075
1.75 MAX
C
0.42±0.09
0.10


SEE DETAIL A
0.22±0.03

OPTION A - BEVEL EDGE



OPTION B - NO BEVEL EDGE


(0.86) x 45°
R0.10
R0.10
GAGE PLANE
0.36
8°
0°
SEATING PLANE
0.65±0.25
(1.04)

DETAIL A
SCALE: 2:1

NOTES:

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M
E) DRAWING FILENAME: M08Arev16

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SignalWise™
SmartMax™
SMART START™
Solutions for Your Success™
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STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
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μSerDes™
μSerDes™
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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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