FAIRCHILD
SEMICONDUCTOR®

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FDG330P

P-Channel 1.8V Specified PowerTrench® MOSFET

General Description

This P-Channel 1.8V specified MOSFET uses Fairchild's advanced low voltage PowerTrench process. It has been optimized for battery power management applications.

Applications

- Battery management
- Load switch

Features

- −2 A, −12 V. $R_{DS(ON)}$ = 110 mΩ @ V_{GS} = −4.5 V
  $R_{DS(ON)}$ = 150 mΩ @ V_{GS} = −2.5 V
  $R_{DS(ON)}$ = 215 mΩ @ V_{GS} = −1.8 V

- Low gate charge

- High performance trench technology for extremely low $R_{DS(ON)}$

- Compact industry standard SC70-6 surface mount package

SC70-6
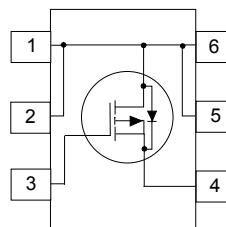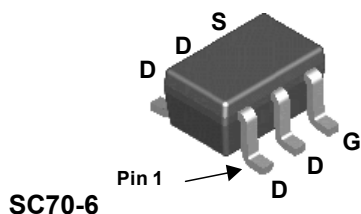
Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		−12	V
V_{GSS}	Gate-Source Voltage		± 8	V
I_D	Drain Current – Continuous	(Note 1a)	−2	A
	– Pulsed		−6	
P_D	Power Dissipation for Single Operation	(Note 1a)	0.75	W
		(Note 1b)	0.48	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	Note 1b)	260	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.30	FDG330P	7"	8mm	3000 units

Electrical Characteristics
$T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = -250$ μA	–12			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250$ μA, Referenced to 25°C		–2.7		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -10$ V, $V_{GS} = 0$ V			–1	μA
I_{GSSF}	Gate–Body Leakage, Forward	$V_{GS} = 8$ V, $V_{DS} = 0$ V			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	$V_{GS} = -8$ V, $V_{DS} = 0$ V			–100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = -250$ μA	–0.4	–0.7	–1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250$ μA, Referenced to 25°C		2.3		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -4.5$ V, $I_D = -2.0$ A $V_{GS} = -2.5$ V, $I_D = -1.7$ A $V_{GS} = -1.8$ V, $I_D = -1.4$ A $V_{GS} = -4.5$ V, $I_D = -2.0$ A, $T_J = 125°C$		84 107 145 98	110 150 215 148	mΩ
$I_{D(on)}$	On–State Drain Current	$V_{GS} = -4.5$ V, $V_{DS} = -5$ V	–6			A
g_{FS}	Forward Transconductance	$V_{DS} = -5$ V, $I_D = -2.0$ A		6.8		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = -6.0$ V, $V_{GS} = 0$ V,		477		pF
C_{oss}	Output Capacitance	f = 1.0 MHz		186		pF
C_{rss}	Reverse Transfer Capacitance			124		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -6.0$ V, $I_D = 1$ A,		10	20	ns
t_r	Turn–On Rise Time	$V_{GS} = -4.5$ V, $R_{GEN} = 6$ Ω		11	20	ns
$t_{d(off)}$	Turn–Off Delay Time			12	22	ns
t_f	Turn–Off Fall Time			18	32	ns
Q_g	Total Gate Charge	$V_{DS} = -6.0$ V, $I_D = -2.0$ A,		5	7	nC
Q_{gs}	Gate–Source Charge	$V_{GS} = -4.5$ V		0.8		nC
Q_{gd}	Gate–Drain Charge			1.4		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				–0.62	A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = -0.62$ A (Note 2)		–0.7	–1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

    a.) 170°C/W when mounted on a 1 in^2 pad of 2 oz. copper.

    b.) 260°C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%
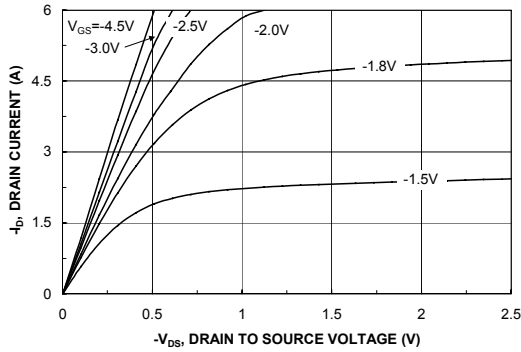
Typical Characteristics

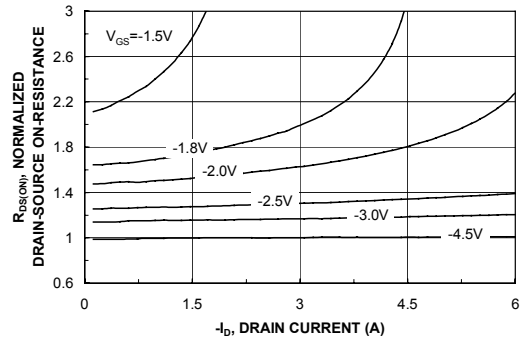**Figure 1. On-Region Characteristics.**

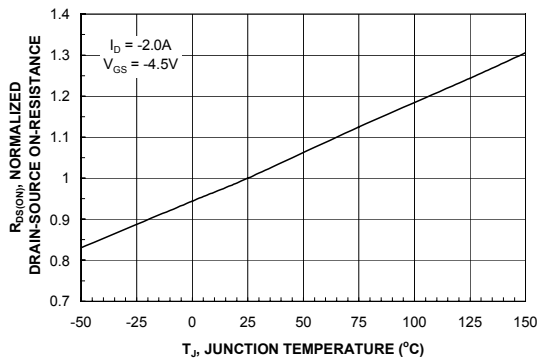**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

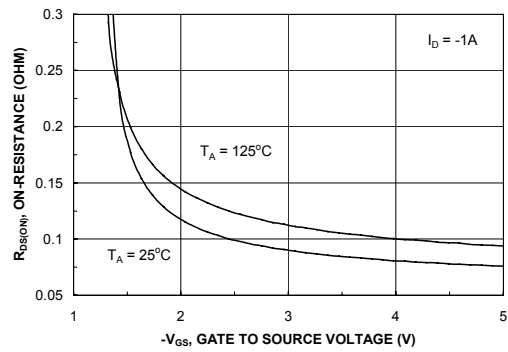**Figure 3. On-Resistance Variation with Temperature.**

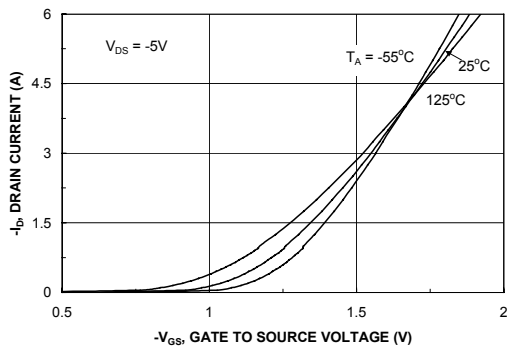**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

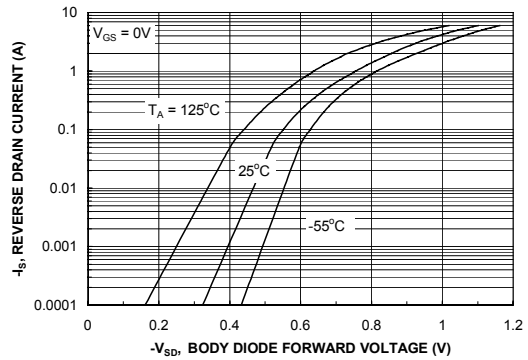**Figure 5. Transfer Characteristics.**

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.
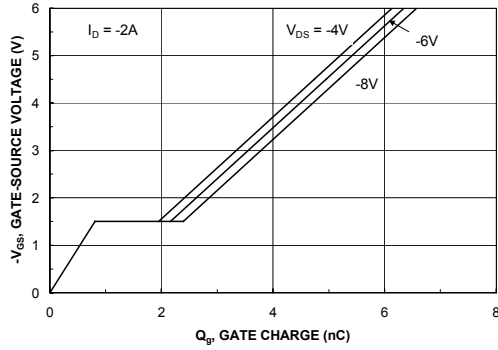
Typical Characteristics
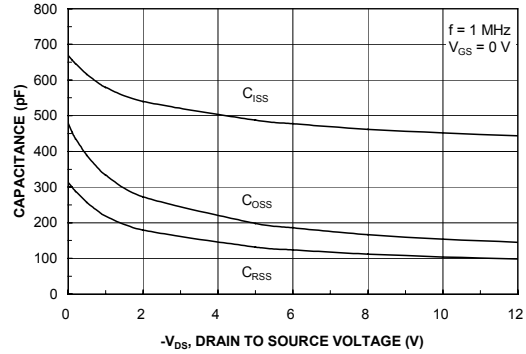

Figure 7. Gate Charge Characteristics.

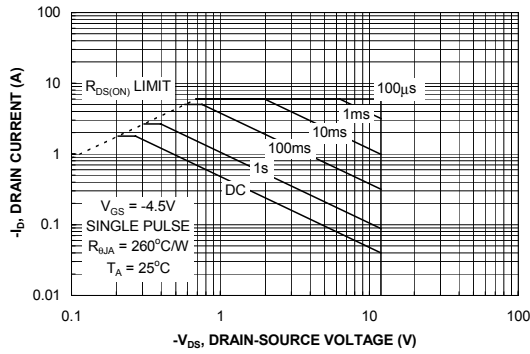**Figure 8. Capacitance Characteristics.**

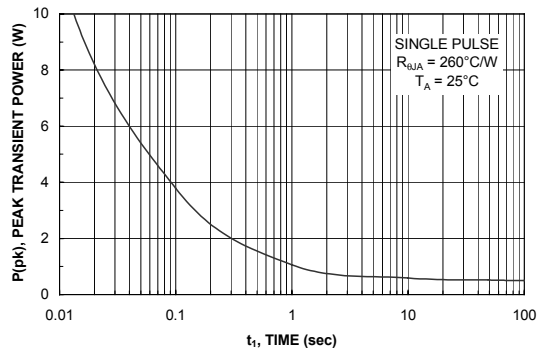**Figure 9. Maximum Safe Operating Area.**

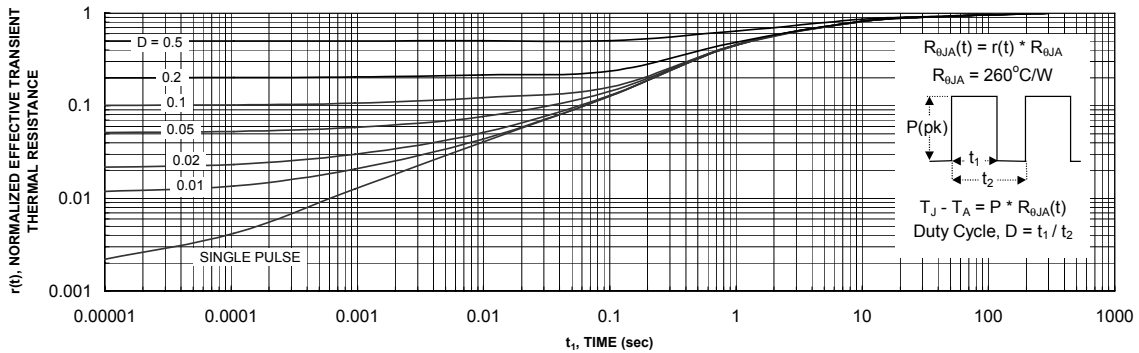**Figure 10. Single Pulse Maximum Power Dissipation.**

Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

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