

# FDP12N50 / FDPF12N50T

## N-Channel UniFET™ MOSFET

500 V, 11.5 A, 650 mΩ

### Features

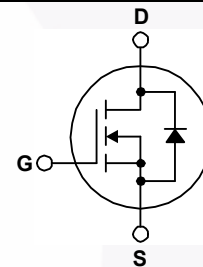
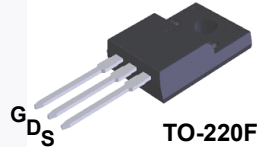
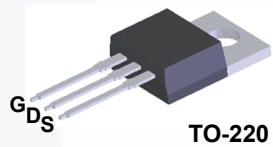
- $R_{DS(on)} = 550 \text{ m}\Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 6 \text{ A}$
- Low Gate Charge (Typ. 22 nC)
- Low  $C_{rss}$  (Typ. 11 pF)
- 100% Avalanche Tested
- RoHS Compliant

### Applications

- LCD/LED/PDP TV
- Lighting
- Uninterruptible Power Supply

### Description

UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDP12N50	FDPF12N50T	Unit	
$V_{DSS}$	Drain to Source Voltage	500		V	
$V_{GSS}$	Gate to Source Voltage	$\pm 30$		V	
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	11.5	11.5 *	A
		- Continuous ( $T_C = 100^\circ\text{C}$ )	6.9	6.9 *	
$I_{DM}$	Drain Current	(Note 1)	46	46 *	A
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	456		mJ
$I_{AR}$	Avalanche Current	(Note 1)	11.5		A
$E_{AR}$	Repetitive Avalanche Energy	(Note 1)	16.7		mJ
$dv/dt$	Peak Diode Recovery $dv/dt$	(Note 3)	4.5		V/ns
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	165	42	W
		- Derate Above $25^\circ\text{C}$	1.33	0.3	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$	
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300		$^\circ\text{C}$	

\*Drain current limited by maximum junction temperature

### Thermal Characteristics

Symbol	Parameter	FDP12N50	FDPF12N50T	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.75	3.0	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	62.5	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP12N50	FDP12N50	TO-220	Tube	N/A	N/A	50 units
FDPF12N50T	FDPF12N50T	TO-220F	Tube	N/A	N/A	50 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}, T_J = 25^\circ\text{C}$	500	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.5	-	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 500 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 400 \text{ V}, T_C = 125^\circ\text{C}$	-	-	1 10	$\mu\text{A}$
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 6 \text{ A}$	-	0.55	0.65	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40 \text{ V}, I_D = 6 \text{ A}$	-	11.5	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$	-	985	1315	pF
$C_{oss}$	Output Capacitance		-	140	190	pF
$C_{rss}$	Reverse Transfer Capacitance		-	11	17	pF
$Q_g$	Total Gate Charge at 10V	$V_{DS} = 400 \text{ V}, I_D = 11.5 \text{ A},$ $V_{GS} = 10 \text{ V}$	-	22	30	nC
$Q_{gs}$	Gate to Source Gate Charge		-	6	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		(Note 4)	-	9	-

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250 \text{ V}, I_D = 11.5 \text{ A},$ $V_{GS} = 10 \text{ V}, R_G = 25 \Omega$	-	24	60	ns
$t_r$	Turn-On Rise Time		-	50	110	ns
$t_{d(off)}$	Turn-Off Delay Time		-	45	100	ns
$t_f$	Turn-Off Fall Time		(Note 4)	-	30	70

### Drain-Source Diode Characteristics

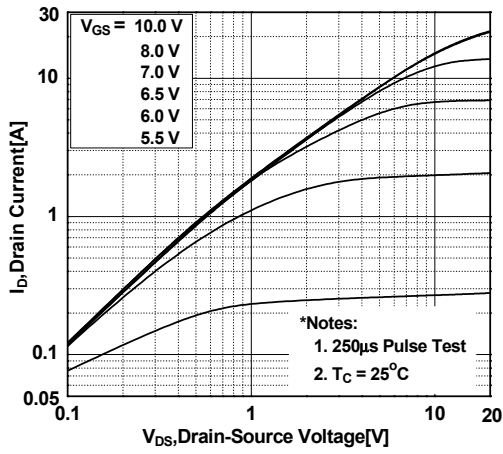
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	11.5	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	46	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{SD} = 11.5 \text{ A}$	-	-	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_{SD} = 11.5 \text{ A},$ $di_F/dt = 100 \text{ A}/\mu\text{s}$	-	375	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	3.5	-	$\mu\text{C}$

#### Notes:

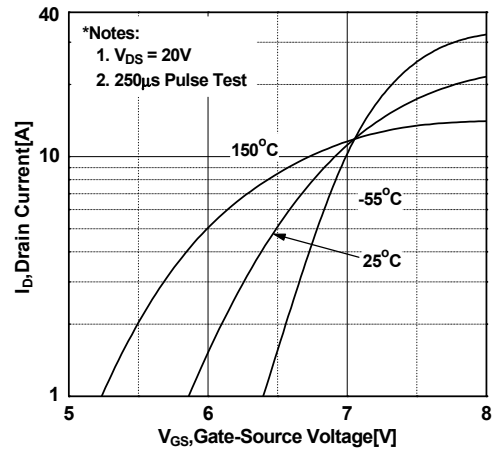
1. Repetitive rating; pulse-width limited by maximum junction temperature.
2.  $L = 6.9 \text{ mH}, I_{AS} = 11.5 \text{ A}, V_{DD} = 50 \text{ V}, R_G = 25 \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 11.5 \text{ A}, di/dt \leq 200 \text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

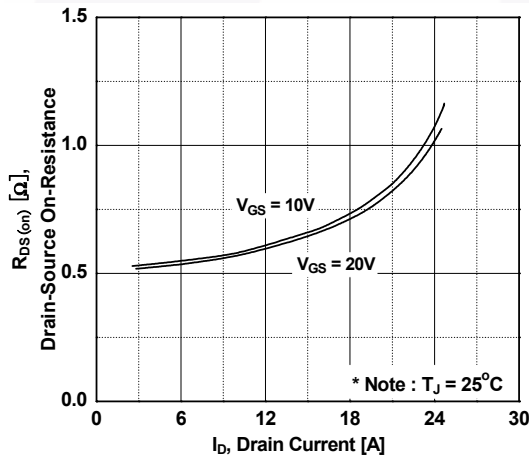
**Figure 1. On-Region Characteristics**



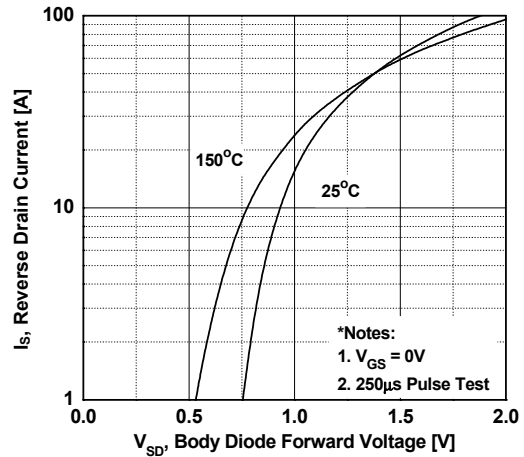
**Figure 2. Transfer Characteristics**



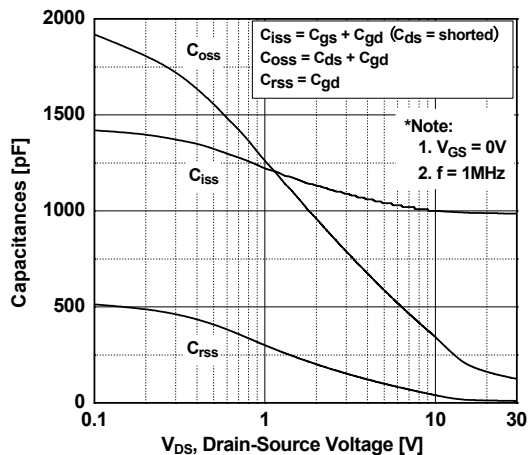
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



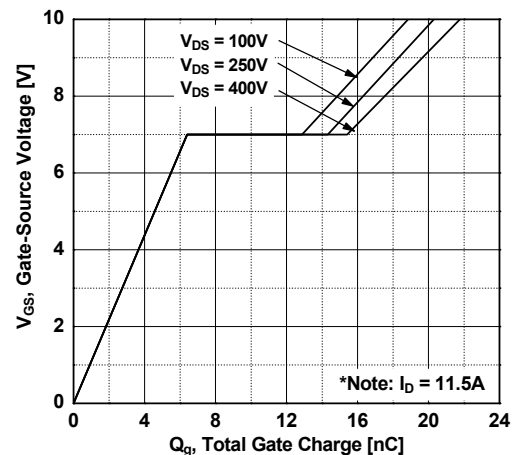
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

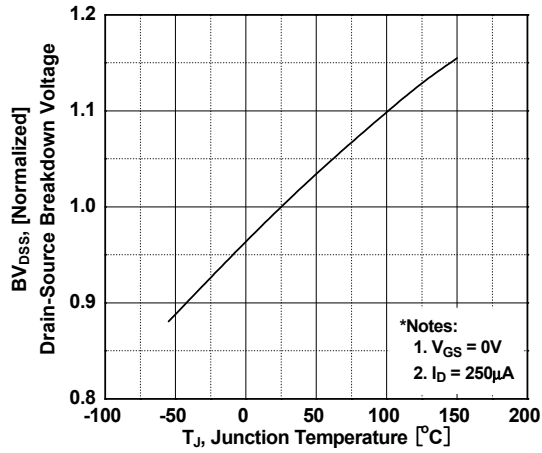


**Figure 6. Gate Charge Characteristics**

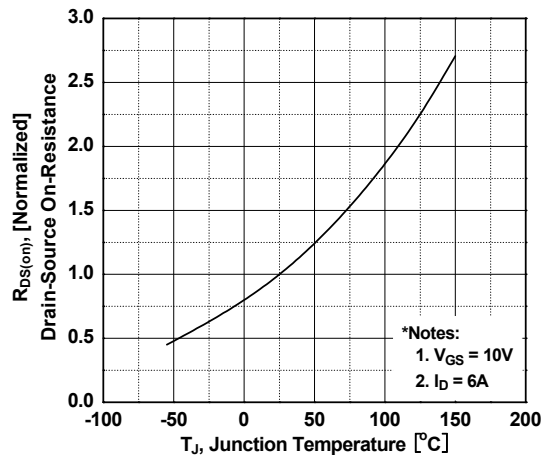


**Typical Performance Characteristics** (Continued)

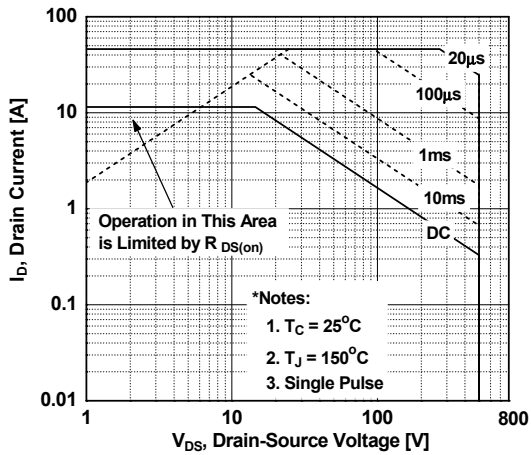
**Figure 7. Breakdown Voltage Variation vs. Temperature**



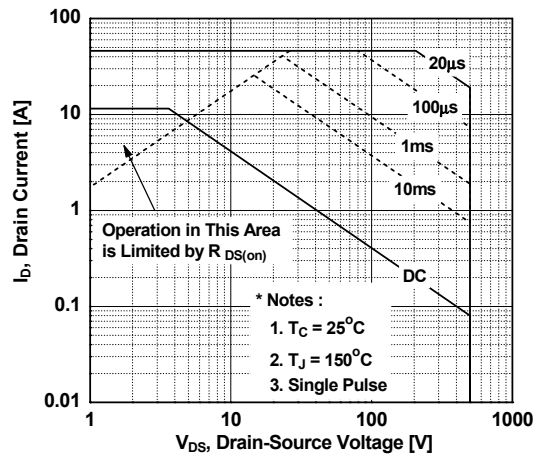
**Figure 8. On-Resistance Variation vs. Temperature**



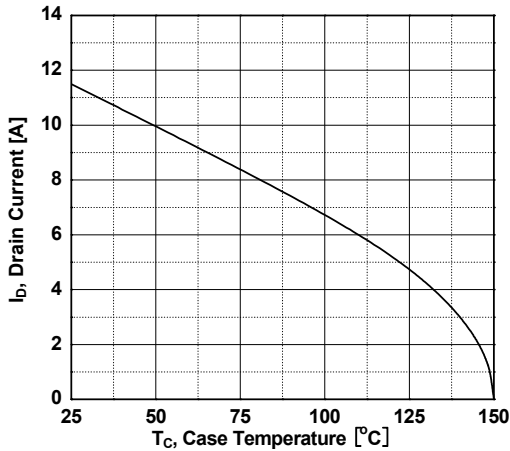
**Figure 9-1. Maximum Safe Operating Area - FDP12N50**



**Figure 9-2. Maximum Safe Operating Area - FDPF12N50T**



**Figure 10. Maximum Drain Current vs. Case Temperature**



Typical Performance Characteristics (Continued)

Figure 11-1. Transient Thermal Response Curve - FDP12N50

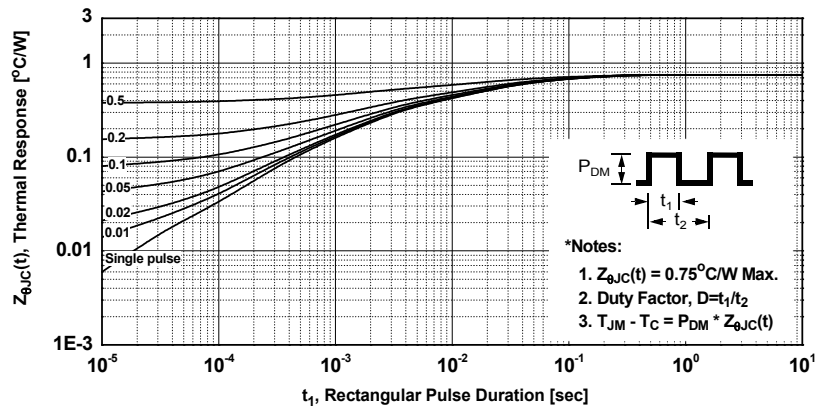


Figure 11-2. Transient Thermal Response Curve - FDPF12N50T

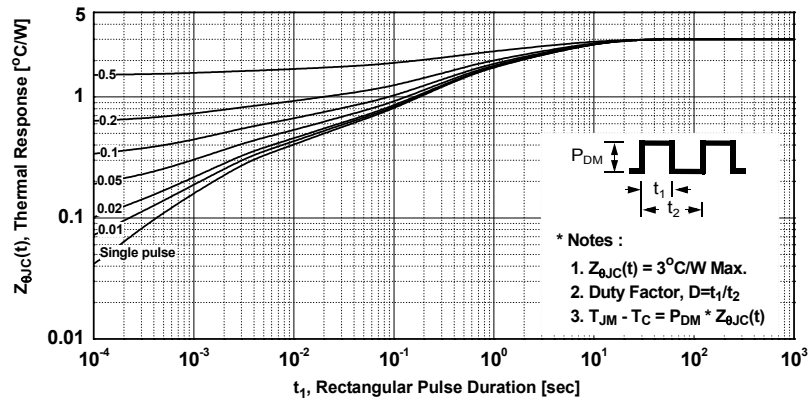




Figure 12. Gate Charge Test Circuit & Waveform



Figure 13. Resistive Switching Test Circuit & Waveforms

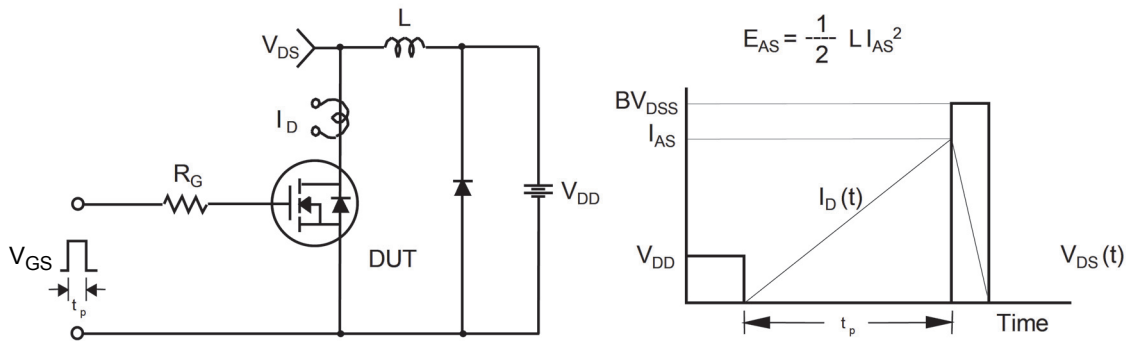


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



**Figure 16. TO-220, Molded, 3-Lead, Jedec Variation AB**

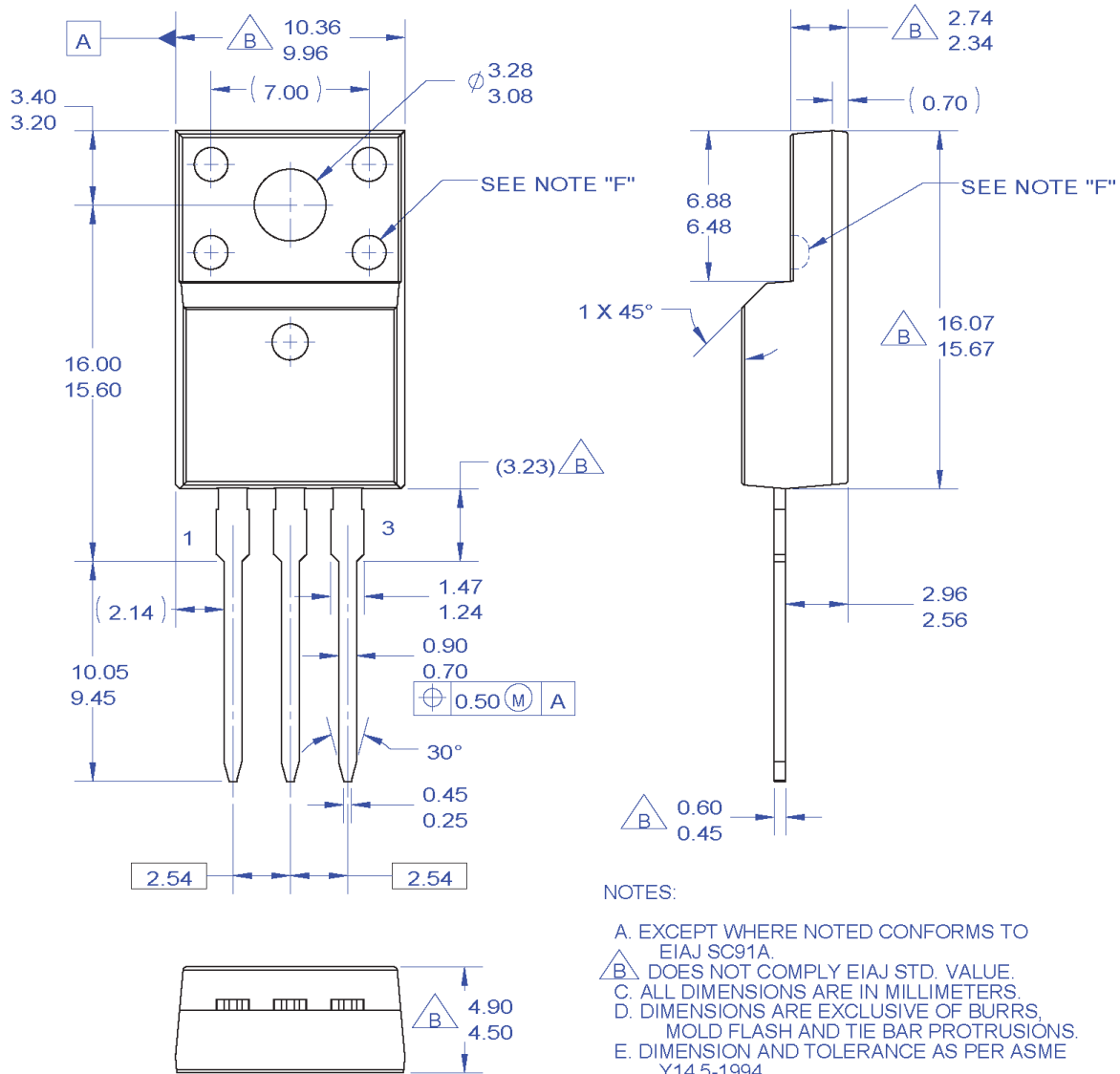
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## Mechanical Dimensions



### NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
- B. DOES NOT COMPLY EIAJ STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- F. OPTION 1 - WITH SUPPORT PIN HOLE.  
OPTION 2 - NO SUPPORT PIN HOLE.
- G. DRAWING FILE NAME: TO220M03REV3

**Figure 17. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead**

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