

# FQB11N40C

## N-Channel QFET® MOSFET

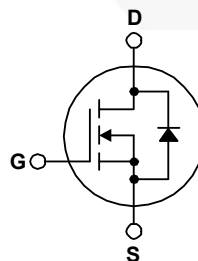
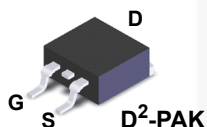
400 V, 10.5 A, 530 mΩ

### Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology.

### Features

- 10.5 A, 400V,  $R_{DS(on)} = 530 \text{ m}\Omega$  (Max.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 5.25 \text{ A}$
- Low Gate Charge (Typ. 28 nC)
- Low Crss (Typ. 85 pF)
- 100% Avalanche Tested



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQB11N40CTM	Unit
$V_{DSS}$	Drain-Source Voltage	400	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ )	10.5	A
	- Continuous ( $T_C = 100^\circ\text{C}$ )	6.6	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	42	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	360	mJ
$I_{AR}$	Avalanche Current (Note 1)	11	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	13.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	135	W
	- Derate above $25^\circ\text{C}$	1.07	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FQB11N40CTM	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.93	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (minimum pad of 2 oz copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (*1 in <sup>2</sup> pad of 2 oz copper), Max.	40	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQB11N40CTM	FQB11N40C	D <sup>2</sup> -PAK	Tape and Reel	330 mm	24 mm	800 units

## Electrical Characteristics T<sub>c</sub> = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### Off Characteristics

BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	400	--	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	--	0.54	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V	--	--	1	μA
		V <sub>DS</sub> = 320 V, T <sub>C</sub> = 125°C	--	--	10	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	--	--	-100	nA

### On Characteristics

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	--	4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5.25 A	--	0.5	0.53	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 5.25 A	--	7.1	--	S

### Dynamic Characteristics

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	--	840	1090	pF
C <sub>oss</sub>	Output Capacitance		--	250	325	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	85	110	pF

### Switching Characteristics

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 200 V, I <sub>D</sub> = 10.5 A, R <sub>G</sub> = 25 Ω  (Note 4)	--	14	40	ns
t <sub>r</sub>	Turn-On Rise Time		--	89	190	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	81	170	ns
t <sub>f</sub>	Turn-Off Fall Time		--	81	170	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 320 V, I <sub>D</sub> = 10.5 A, V <sub>GS</sub> = 10 V  (Note 4)	--	28	35	nC
Q <sub>gs</sub>	Gate-Source Charge		--	4	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	15	--	nC

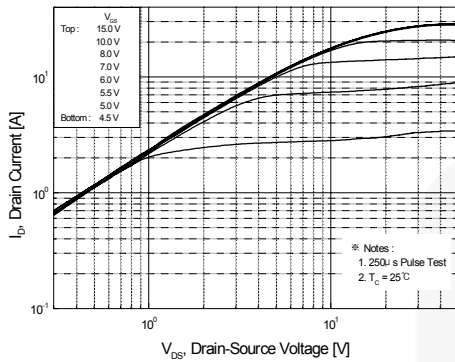
### Drain-Source Diode Characteristics and Maximum Ratings

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current	--	--	10.5	A	
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current	--	--	42	A	
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 10.5 A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 10.5 A, dI <sub>F</sub> / dt = 100 A/μs	--	290	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	2.4	--	μC

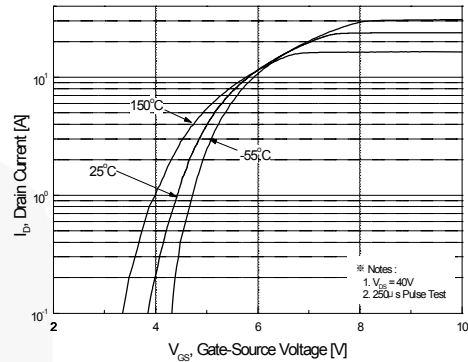
#### Notes:

1. Repetitive rating; pulse-width limited by maximum junction temperature.
2. L = 5.7 mH, I<sub>AS</sub> = 10.5 A, V<sub>DD</sub> = 50 V, R<sub>G</sub> = 25 Ω, starting T<sub>J</sub> = 25°C.
3. I<sub>SD</sub> ≤ 10.5 A, di/dt ≤ 200 A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, starting T<sub>J</sub> = 25°C.
4. Essentially independent of operating temperature.

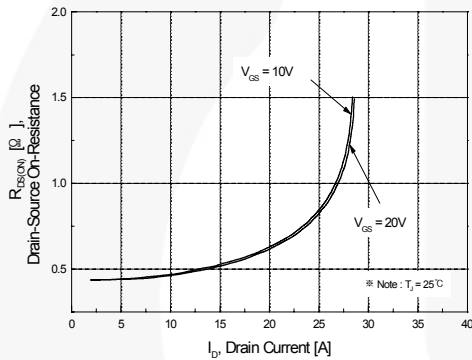
## Typical Characteristics



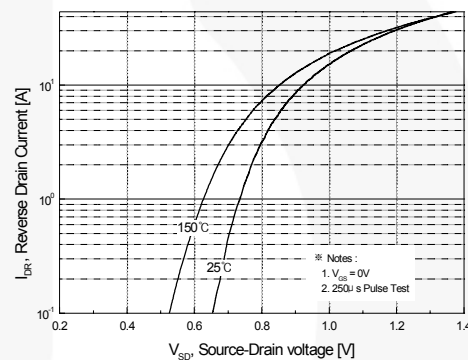
**Figure 1. On-Region Characteristics**



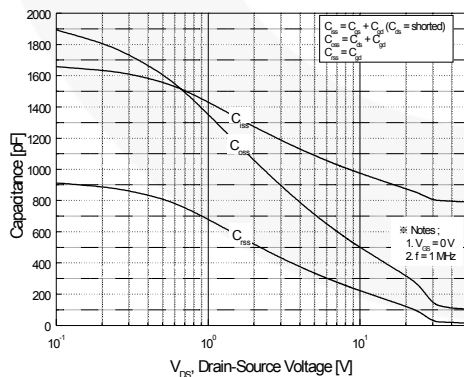
**Figure 2. Transfer Characteristics**



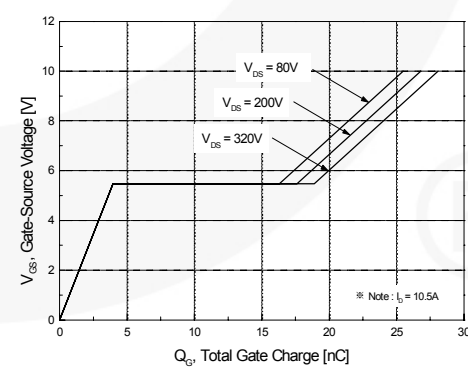
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



**Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature**

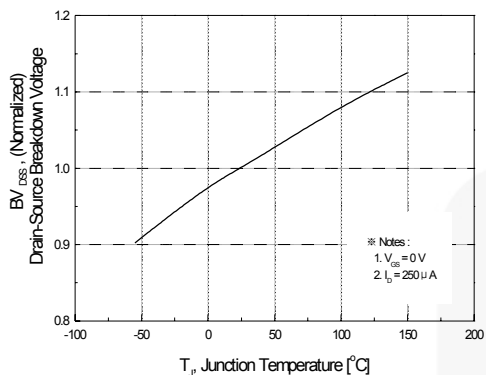


**Figure 5. Capacitance Characteristics**

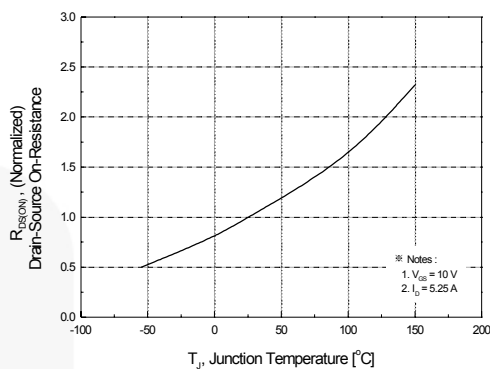


**Figure 6. Gate Charge Characteristics**

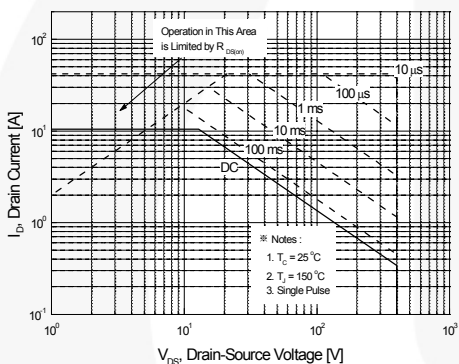
## Typical Characteristics (Continued)



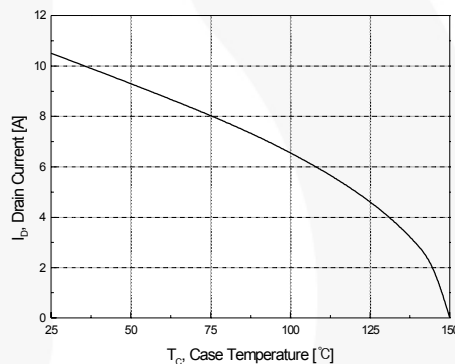
**Figure 7. Breakdown Voltage Variation vs Temperature**



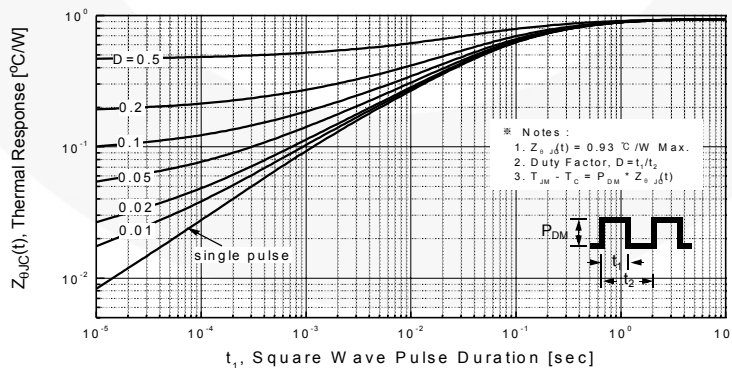
**Figure 8. On-Resistance Variation vs Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs Case Temperature**



**Figure 11. Transient Thermal Response Curve**

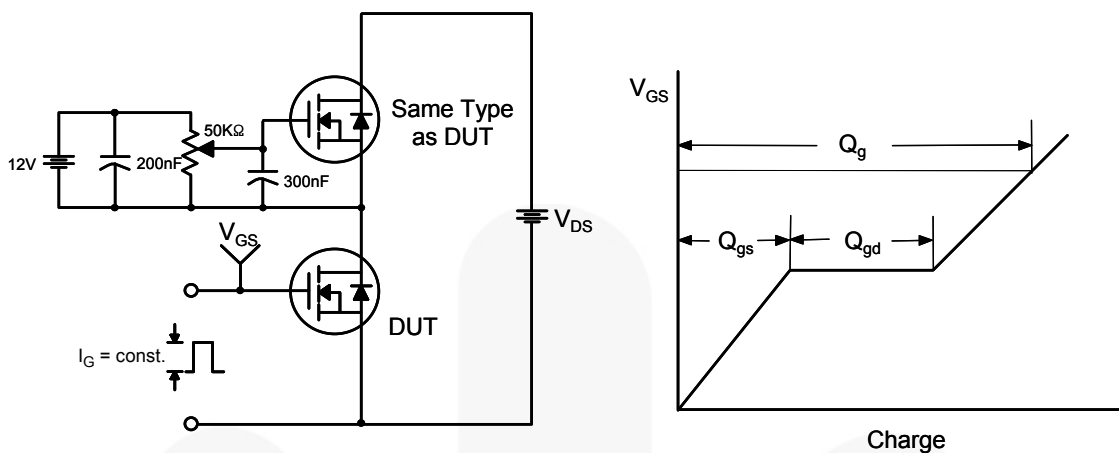


Figure 12. Gate Charge Test Circuit & Waveform

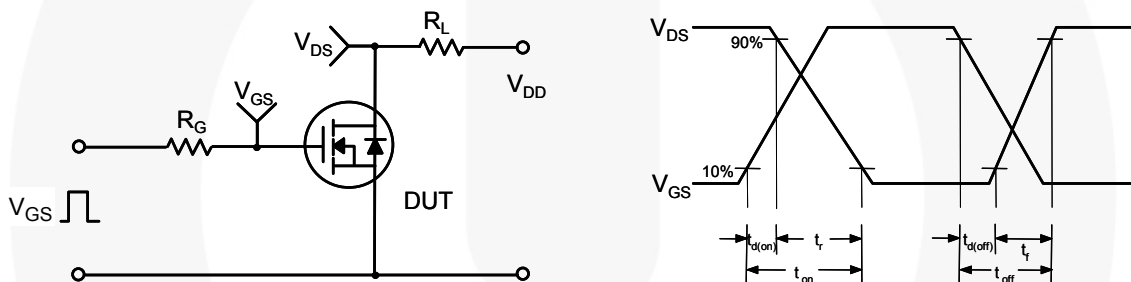


Figure 13. Resistive Switching Test Circuit & Waveforms

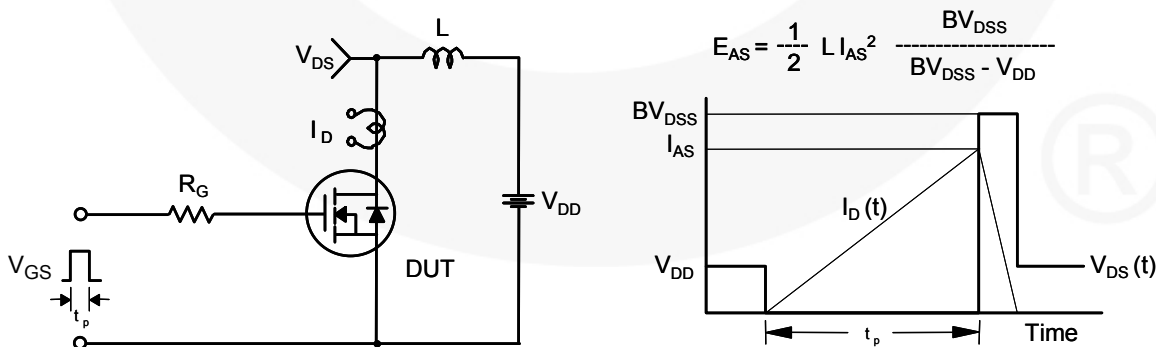


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

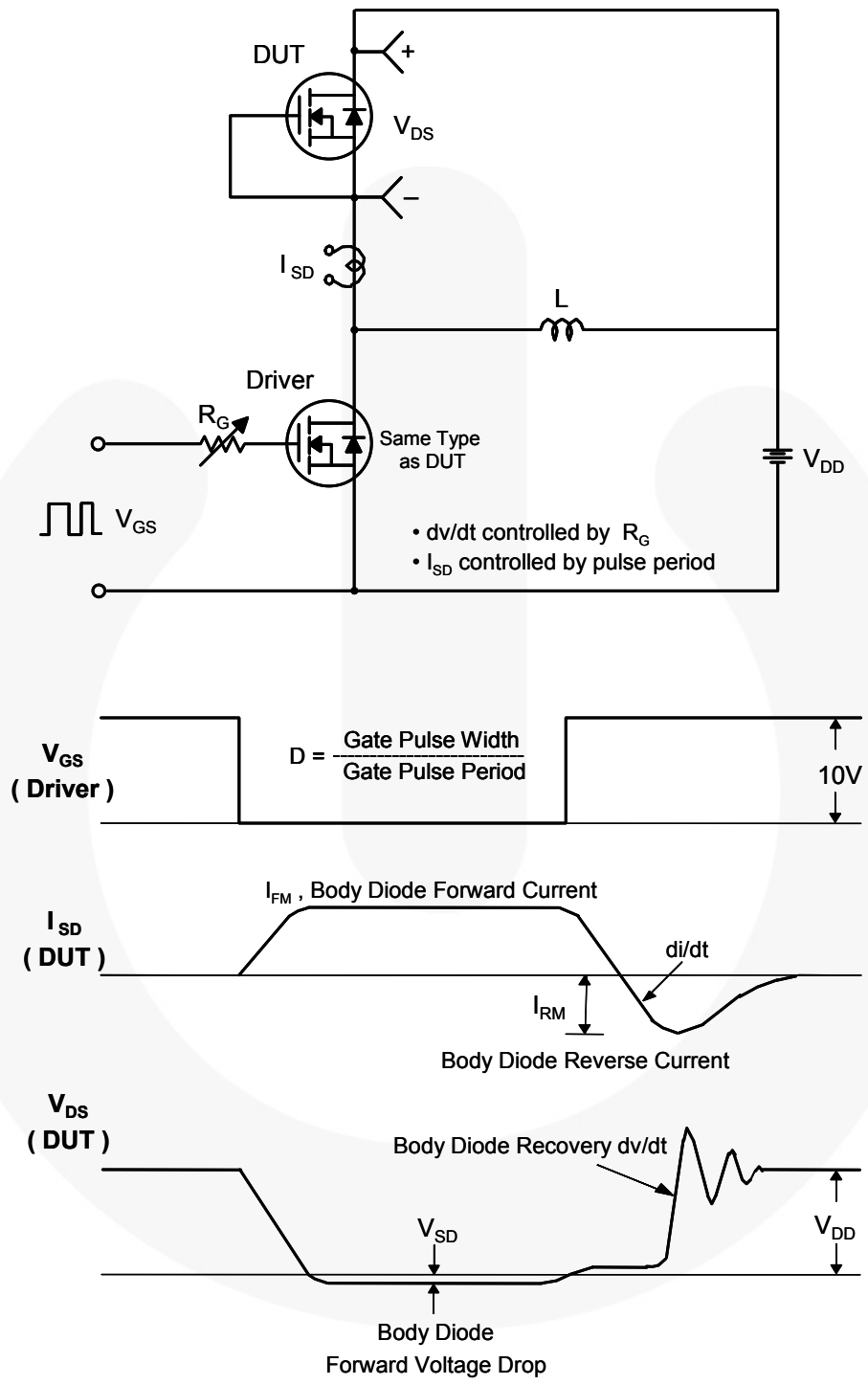
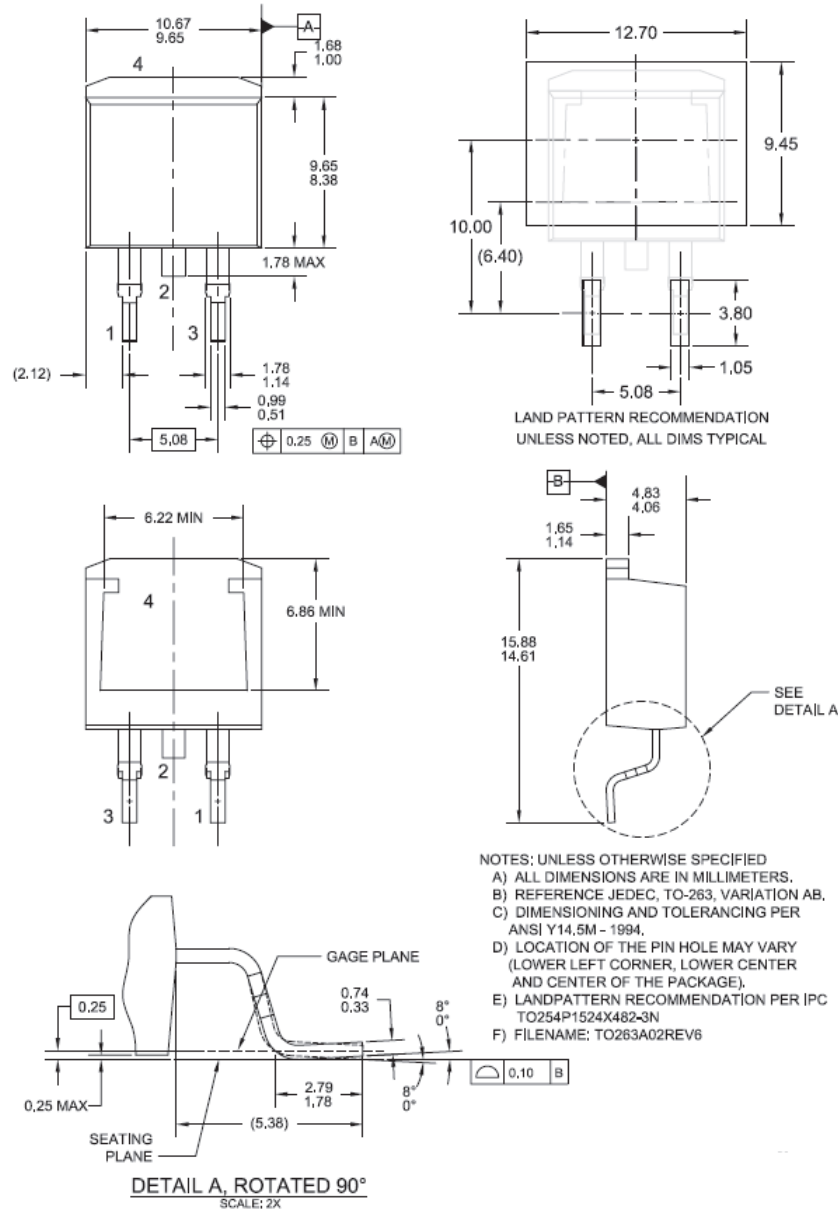


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

## Mechanical Dimensions



**Figure 16. TO263 (D<sup>2</sup>PAK), Molded, 2-Lead, Surface Mount**

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