

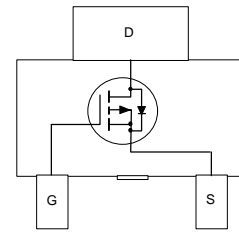
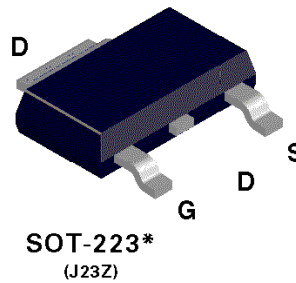
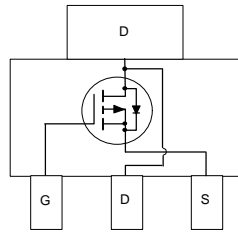
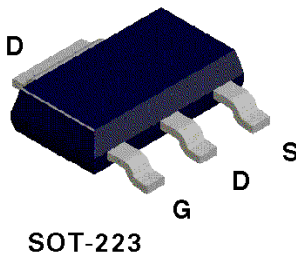
## NDT452AP P-Channel Enhancement Mode Field Effect Transistor

### General Description

Power SOT P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and DC motor control.

### Features

- -5A, -30V.  $R_{DS(ON)} = 0.065\Omega @ V_{GS} = -10V$   
 $R_{DS(ON)} = 0.1\Omega @ V_{GS} = -4.5V.$
- High density cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability in a widely used surface mount package.



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	NDT452AP	Units
$V_{DSS}$	Drain-Source Voltage	-30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current - Continuous (Note 1a)	-5	A
	- Pulsed	- 15	
$P_D$	Maximum Power Dissipation (Note 1a)	3	W
	(Note 1b)	1.3	
	(Note 1c)	1.1	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-65 to 150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	42	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	12	$^\circ\text{C/W}$

\* Order option J23Z for cropped center drain lead.

**Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-30			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$ $T_J = 55^\circ\text{C}$			-1	$\mu\text{A}$
					-10	$\mu\text{A}$
$I_{GSSF}$	Gate - Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
<b>ON CHARACTERISTICS</b> (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$ $T_J = 125^\circ\text{C}$	-1	-1.6	-2.8	V
			-0.7	-1.2	-2.2	
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -5.0\text{ A}$ $T_J = 125^\circ\text{C}$ $V_{GS} = -4.5\text{ V}, I_D = -4.3\text{ A}$		0.052	0.065	$\Omega$
				0.075	0.13	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -10\text{ V}, V_{DS} = -5\text{ V}$ $V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	-15			A
			-5			
$g_{FS}$	Forward Transconductance	$V_{DS} = -10\text{ V}, I_D = -5.0\text{ A}$		7		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		690		pF
$C_{oss}$	Output Capacitance			430		pF
$C_{rss}$	Reverse Transfer Capacitance			160		pF
<b>SWITCHING CHARACTERISTICS</b> (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = -10\text{ V}, I_D = -1\text{ A},$ $V_{GEN} = -10\text{ V}, R_{GEN} = 6\ \Omega$		9	20	ns
$t_r$	Turn - On Rise Time			20	30	ns
$t_{D(off)}$	Turn - Off Delay Time			40	50	ns
$t_f$	Turn - Off Fall Time			19	40	ns
$Q_g$	Total Gate Charge		$V_{DS} = -10\text{ V},$ $I_D = -5.0\text{ A}, V_{GS} = -10\text{ V}$		22	30
$Q_{gs}$	Gate-Source Charge			3.2		nC
$Q_{gd}$	Gate-Drain Charge			5.2		nC

## Electrical Characteristics (T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				-2.5	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -2.5 A (Note 2)		-0.85	-1.2	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>F</sub> = -2.5 A, dI <sub>F</sub> /dt = 100 A/μs			100	ns

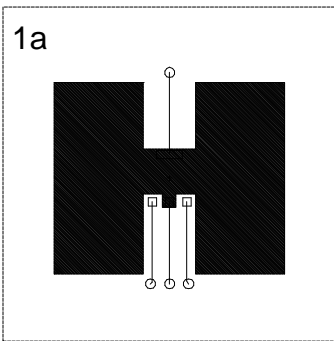
Notes:

- R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.

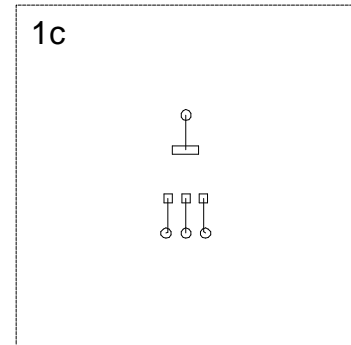
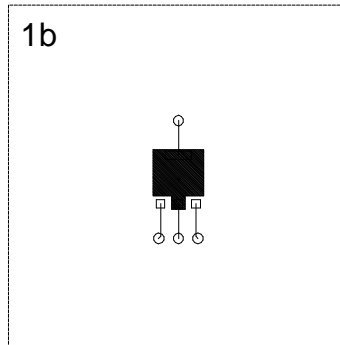
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)} \theta_{TJ}$$

Typical R<sub>θJA</sub> using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- 42°C/W when mounted on a 1 in<sup>2</sup> pad of 2oz copper.
- 95°C/W when mounted on a 0.066 in<sup>2</sup> pad of 2oz copper.
- 110°C/W when mounted on a 0.0123 in<sup>2</sup> pad of 2oz copper.



Scale 1 : 1 on letter size paper



- Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

## Typical Electrical Characteristics

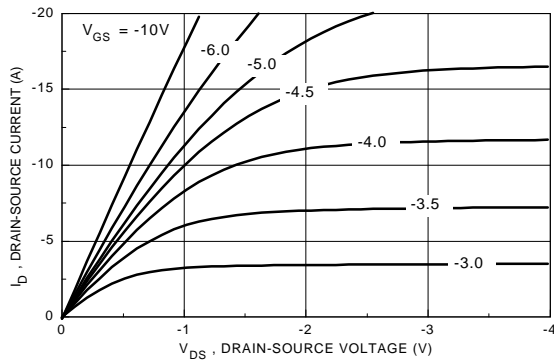


Figure 1. On-Region Characteristics.

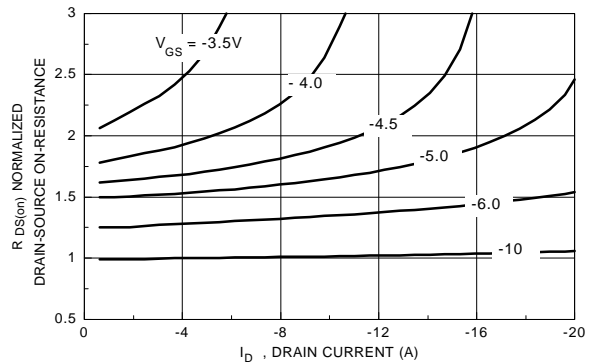


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

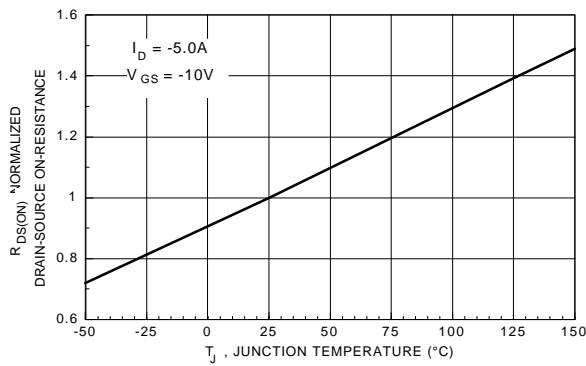


Figure 3. On-Resistance Variation with Temperature.

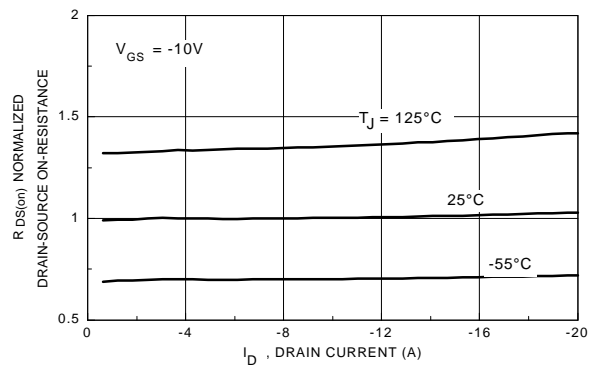


Figure 4. On-Resistance Variation with Drain Current and Temperature.

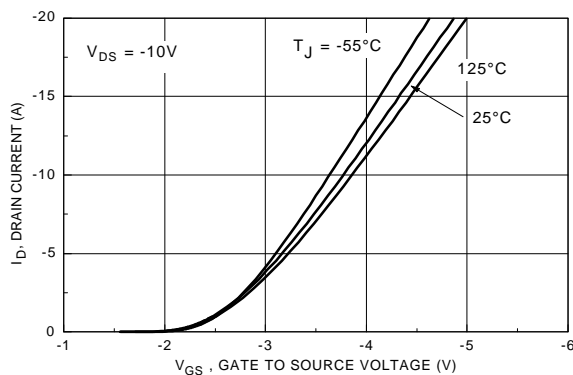


Figure 5. Transfer Characteristics.

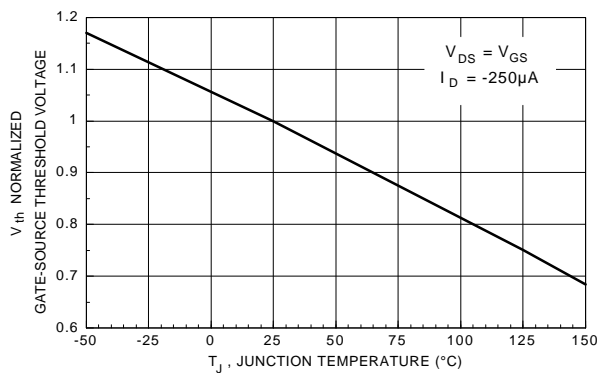


Figure 6. Gate Threshold Variation with Temperature.

## Typical Electrical Characteristics

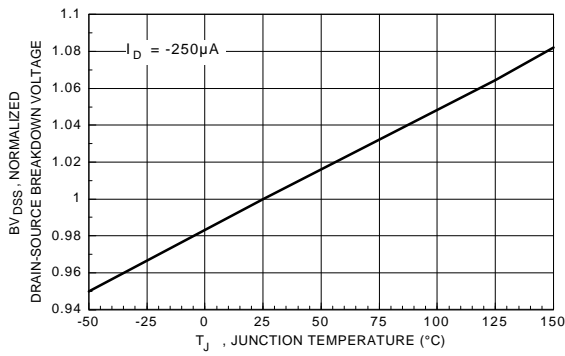


Figure 7. Breakdown Voltage Variation with Temperature.

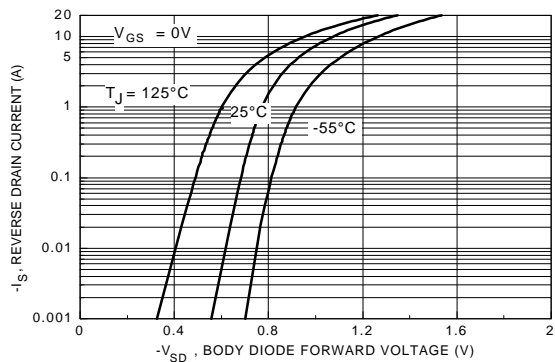


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

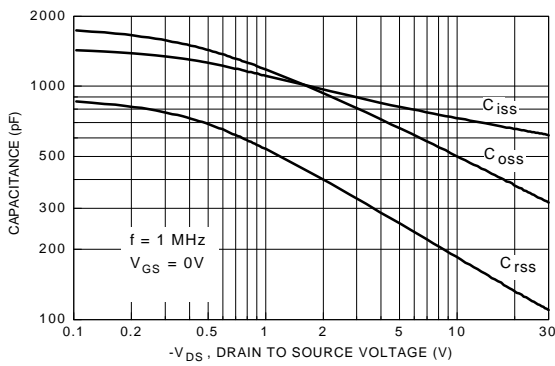


Figure 9. Capacitance Characteristics.

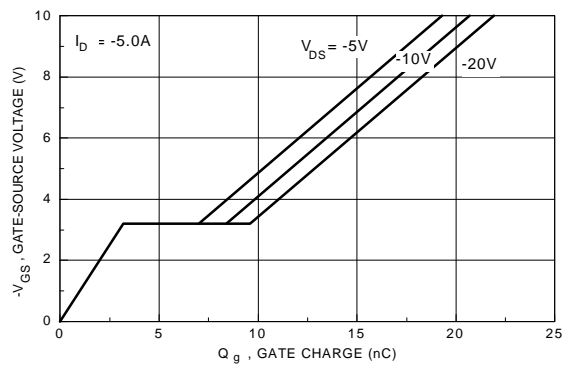


Figure 10. Gate Charge Characteristics.

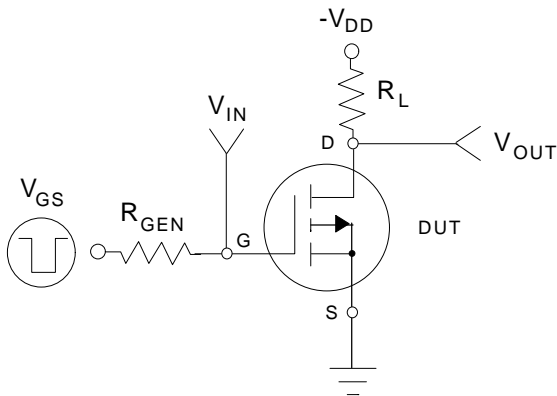


Figure 11. Switching Test Circuit.

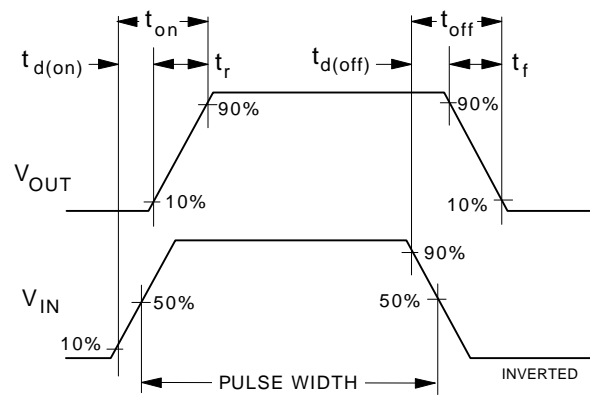
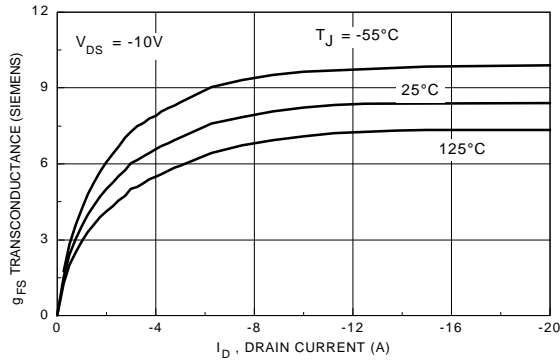
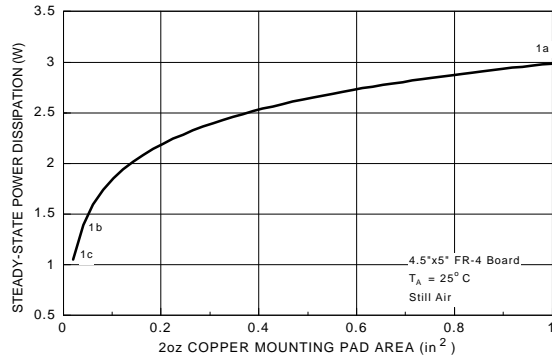


Figure 12. Switching Waveforms.

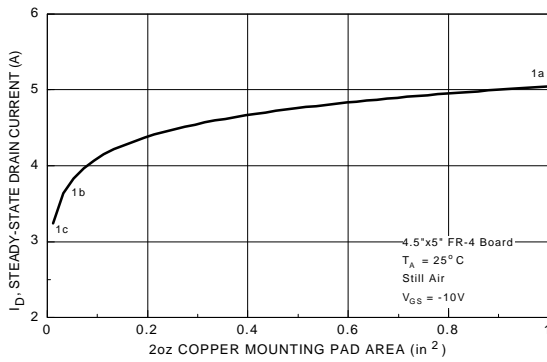
## Typical Thermal Characteristics



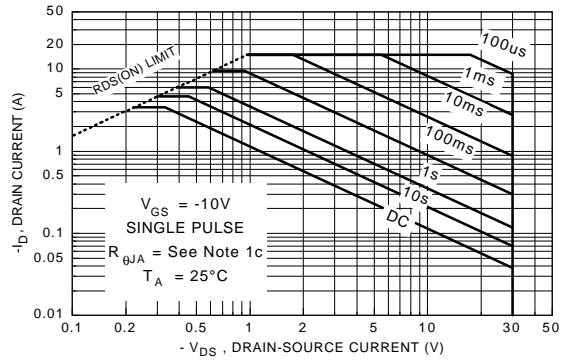
**Figure 13. Transconductance Variation with Drain Current and Temperature.**



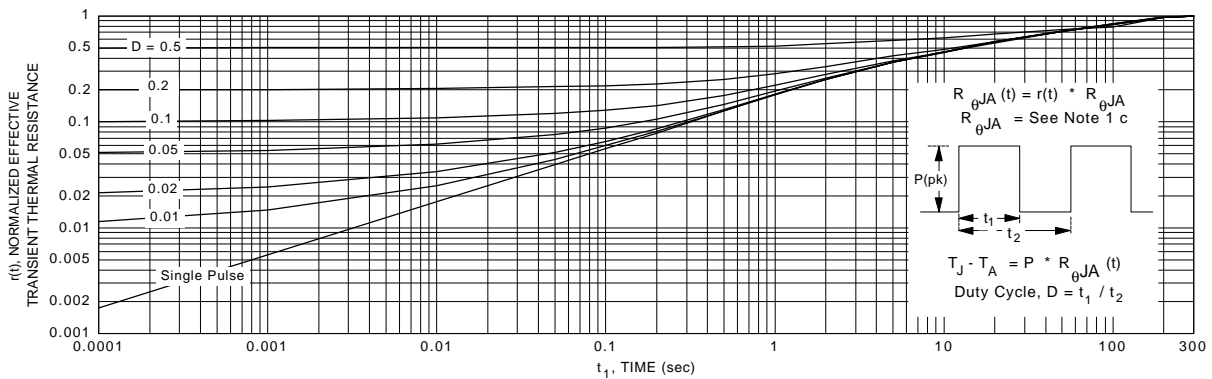
**Figure 14. SOT-223 Maximum Steady-state Power Dissipation versus Copper Mounting Pad Area.**



**Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.**



**Figure 16. Maximum Safe Operating Area.**



**Figure 17. Transient Thermal Response Curve.**

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

## TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE <sub>x</sub> <sup>TM</sup>	FAST <sup>®</sup>	OPTOLOGIC <sup>TM</sup>	SMART START <sup>TM</sup>	VCX <sup>TM</sup>
Bottomless <sup>TM</sup>	FAST <sub>r</sub> <sup>TM</sup>	OPTOPLANAR <sup>TM</sup>	STAR*POWER <sup>TM</sup>	
CoolFET <sup>TM</sup>	FRFET <sup>TM</sup>	PACMAN <sup>TM</sup>	Stealth <sup>TM</sup>	
CROSSVOLT <sup>TM</sup>	GlobalOptoisolator <sup>TM</sup>	POPT <sup>TM</sup>	SuperSOT <sup>TM</sup> -3	
DenseTrench <sup>TM</sup>	GTO <sup>TM</sup>	Power247 <sup>TM</sup>	SuperSOT <sup>TM</sup> -6	
DOMET <sup>TM</sup>	HiSeC <sup>TM</sup>	PowerTrench <sup>®</sup>	SuperSOT <sup>TM</sup> -8	
EcoSPARK <sup>TM</sup>	ISOPLANAR <sup>TM</sup>	QFET <sup>TM</sup>	SyncFET <sup>TM</sup>	
E <sup>2</sup> CMOS <sup>TM</sup>	LittleFET <sup>TM</sup>	QST <sup>TM</sup>	TinyLogic <sup>TM</sup>	
EnSigna <sup>TM</sup>	MicroFET <sup>TM</sup>	QT Optoelectronics <sup>TM</sup>	TruTranslation <sup>TM</sup>	
FACT <sup>TM</sup>	MicroPak <sup>TM</sup>	Quiet Series <sup>TM</sup>	UHC <sup>TM</sup>	
FACT Quiet Series <sup>TM</sup>	MICROWIRE <sup>TM</sup>	SILENT SWITCHER <sup>®</sup>	UltraFET <sup>®</sup>	

STAR\*POWER is used under license

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Fairchild Semiconductor:](#)

[NDT452AP](#)