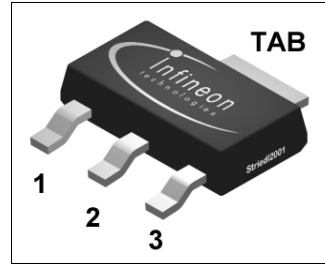




**Features**

- Logic Level Input
- Input protection (ESD)
- Thermal shutdown with auto restart
- Overload protection
- Short circuit protection
- Overvoltage protection
- Current limitation
- Green Product (RoHS compliant)
- AEC Stress Test Qualification



**Application**

- All kinds of resistive, inductive and capacitive loads in switching applications
- $\mu\text{C}$  compatible power switch for 12 V and 24 V DC applications and for 42 Volt Powernet
- Replaces electromechanical relays and discrete circuits

**General Description**

N channel vertical power FET in Smart Power Technology. Fully protected by embedded protection functions.

Type	Ordering Code	Package
HITFET® BSP 75N	on request	PG-SOT223-4

**Product Summary**

Parameter	Symbol	Value	Unit
Continuous drain source voltage	$V_{DS}$	60	V
On-state resistance	$R_{DS(ON)}$	550	$\text{m}\Omega$
Current limitation	$I_{D(lim)}$	1	A
Nominal load current	$I_{D(Nom)}$	0.7	A
Clamping energy	$E_{AS}$	550	mJ



## Circuit Description

The BSP 75N is a monolithic power switch in Smart Power Technology (SPT) with a logic level input, an open drain DMOS output stage and integrated protection functions. It is designed for all kind of resistive and inductive loads (relays, solenoid) in automotive and industrial applications.

## Protection Functions

- **Over voltage protection:** An internal clamp limits the output voltage at  $V_{DS(AZ)}$  (min. 60V) when inductive loads are switched off.
- **Current limitation:** By means of an internal current measurement the drain current is limited at  $I_{D(lim)}$  (1.4 - 1.5 A typ.). If the current limitation is active the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. This operation leads to an increasing junction temperature until the over temperature threshold is reached.
- **Over temperature and short circuit protection:** This protection is based on sensing the chip temperature. The location of the sensor ensures a fast and accurate junction temperature detection. Over temperature shutdown occurs at minimum 150 °C. A hysteresis of typ. 10 K enables an automatic restart by cooling.

The device is ESD protected according Human Body Model (4 kV) and load dump protected (see Maximum Ratings).

**Absolute Maximum Ratings**
 $T_j = 25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Values	Unit	Remarks
Continuous drain source voltage <sup>1)</sup>	$V_{DS}$	60	V	–
Drain source voltage for short circuit protection	$V_{DS}$	36	V	–
Continuous input voltage	$V_{IN}$	-0.2 ... +10	V	–
Peak input voltage	$V_{IN}$	-0.2 ... +20	V	–
Continuous Input Current -0.2V ≤ $V_{IN}$ ≤ 10V $V_{IN}$ < -0.2V or $V_{IN}$ > 10V	$I_{IN}$	no limit   $I_{IN}$   ≤ 2mA	mA	–
Operating temperature range	$T_j$	-40 ... +150	°C	–
Storage temperature range	$T_{stg}$	-55 ... +150	°C	–
Power dissipation (DC)	$P_{tot}$	1.8	W	–
Unclamped single pulse inductive energy	$E_{AS}$	550	mJ	$I_{D(ISO)} = 0.7\text{ A}$ ; $V_{bb} = 32\text{ V}$
Load dump protection <sup>2)</sup> IN = low or high (8 V); $R_L = 50\ \Omega$ IN = high (8 V); $R_L = 22\ \Omega$	$V_{LoadDump}$	80 47	V	$V_{LoadDump} =$ $V_P + V_S$ ; $V_P = 13.5\text{ V}$ $R_1^{3)} = 2\ \Omega$ ; $t_d = 400\text{ ms}$ ;
<b>Electrostatic discharge voltage (Human Body Model)</b> according to MIL STD 883D, method 3015.7 and EOS/ESD assn. standard S5.1 - 1993	$V_{ESD}$	4000	V	–

**Thermal Resistance**

Junction soldering point	$R_{thJS}$	≤ 10	K/W	–
Junction - ambient <sup>4)</sup>	$R_{thJA}$	≤ 70	K/W	–

<sup>1)</sup> See also [Figure 7](#) and [Figure 10](#).

<sup>2)</sup>  $V_{LoadDump}$  is setup without DUT connected to the generator per ISO 7637-1 and DIN 40 839. See also [page 7](#).

<sup>3)</sup>  $R_1$  = internal resistance of the load dump test pulse generator LD200.

<sup>4)</sup> Device on epoxy pcb 40 mm × 40 mm × 1.5 mm with 6 cm<sup>2</sup> copper area for pin 4 connection.

**Electrical Characteristics**
 $T_j = 25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		

**Static Characteristics**

Drain source clamp voltage	$V_{DS(AZ)}$	60	–	75	V	$I_D = 10\text{ mA}$ , $T_j = -40 \dots +150\text{ °C}$
Off state drain current	$I_{DSS}$	–	–	5	$\mu\text{A}$	$V_{IN} = 0\text{ V}$ , $V_{DS} = 32\text{ V}$ , $T_j = -40 \dots +150\text{ °C}$
Input threshold voltage	$V_{IN(th)}$	1	1.8	2.5	V	$I_D = 10\text{ mA}$
Input current: normal operation, $I_D < I_{D(lim)}$ ; current limitation mode, $I_D = I_{D(lim)}$ ; After thermal shutdown, $I_D = 0\text{ A}$ :	$I_{IN(1)}$ $I_{IN(2)}$ $I_{IN(3)}$	– – 1000	100 250 1500	200 400 2000	$\mu\text{A}$	$V_{IN} = 5\text{ V}$
On-state resistance $T_j = 25\text{ °C}$ $T_j = 150\text{ °C}$	$R_{DS(on)}$	– –	490 850	675 1350	$\text{m}\Omega$	$I_D = 0.7\text{ A}$ , $V_{IN} = 5\text{ V}$
On-state resistance $T_j = 25\text{ °C}$ $T_j = 150\text{ °C}$	$R_{DS(on)}$	– –	430 750	550 1000	$\text{m}\Omega$	$I_D = 0.7\text{ A}$ , $V_{IN} = 10\text{ V}$
Nominal load current	$I_{D(Nom)}$	0.7	–	–	A	$V_{BB} = 12\text{ V}$ , $V_{DS} = 0.5\text{ V}$ , $T_S = 85\text{ °C}$ , $T_j < 150\text{ °C}$
Current limit	$I_{D(lim)}$	1	1.5	1.9	A	$V_{IN} = 10\text{ V}$ , $V_{DS} = 12\text{ V}$

**Dynamic Characteristics <sup>1)</sup>**

Turn-on time	$V_{IN}$ to 90% $I_D$ :	$t_{on}$	–	10	20	$\mu\text{s}$	$R_L = 22\ \Omega$ , $V_{IN} = 0$ to 10 V, $V_{BB} = 12\text{ V}$
Turn-off time	$V_{IN}$ to 10% $I_D$ :	$t_{off}$	–	10	20	$\mu\text{s}$	$R_L = 22\ \Omega$ , $V_{IN} = 10$ to 0 V, $V_{BB} = 12\text{ V}$

**Electrical Characteristics (cont'd)**
 $T_j = 25\text{ °C}$ , unless otherwise specified

Parameter	Sym- bol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Slew rate on      70 to 50% $V_{BB}$ :	$-dV_{DS}/dt_{on}$	–	5	10	V/ $\mu$ s	$R_L = 22\ \Omega$ , $V_{IN} = 0$ to 10 V, $V_{BB} = 12$ V
Slew rate off      50 to 70% $V_{BB}$ :	$dV_{DS}/dt_{off}$	–	10	15	V/ $\mu$ s	$R_L = 22\ \Omega$ , $V_{IN} = 10$ to 0 V, $V_{BB} = 12$ V

**Protection Functions<sup>2)</sup>**

Thermal overload trip temperature	$T_{jt}$	150	165	180	°C	–
Thermal hysteresis	$\Delta T_{jt}$	–	10	–	K	–
Unclamped single pulse inductive energy	$E_{AS}$	550	–	–	mJ	$I_{D(ISO)} = 0.7$ A, $V_{BB} = 32$ V
	$T_j = 25\text{ °C}$	200	–	–		
	$T_j = 150\text{ °C}$					

**Inverse Diode**

Continuous source drain voltage	$V_{SD}$	–	1	–	V	$V_{IN} = 0$ V, $-I_D = 2 \times 0.7$ A
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<sup>1)</sup> See also [Figure 9](#).

<sup>2)</sup> Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous, repetitive operation.

## EMC-Characteristics

The following EMC-Characteristics outline the behavior of typical devices. They are not part of any production test.

**Table 1 Test Conditions**

Parameter	Symbol	Value	Unit	Remark
Temperature	$T_A$	23 ±5	°C	–
Supply Voltage	$V_S$	13.5	V	–
Load	$R_L$	27	Ω	ohmic
Operation mode	PWM DC	– –	– –	$f_{INx}=100\text{Hz}$ , $D=0.5$ ON / OFF
DUT specific	$V_{IN}(\text{'HIGH'})=5\text{V}$			

### Fast electrical transients

acc. to ISO 7637

Test <sup>1)</sup> Pulse	Max. Test Level	Test Result		Pulse Cycle Time and Generator Impedance
		OUT <sub>x</sub> stressed		
		ON	OFF	
1	-200V	C	C	500ms ; 10Ω
2	+200V	C	C	500ms ; 10Ω
3a	-200V	C	C	100ms ; 50Ω
3b	+200V	C	C	100ms ; 50Ω
4	-7V	C	C	0.01Ω
5	175V	E(65V)	E(75V)	400ms ; 2Ω

<sup>1)</sup> The test pulses are applied at  $V_S$

### Definition of functional status

Class	Content
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more function of a device does not perform as designed after exposure and can not be returned to proper operation without repairing or replacing the device. The value after the character shows the limit.

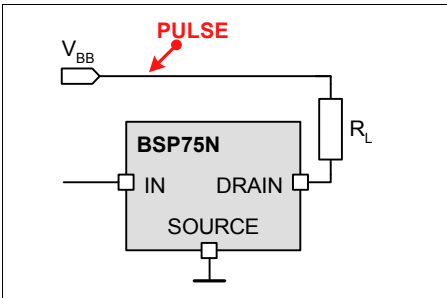


Figure 3 Test circuit for ISO pulse

**Conducted Emissions**

Acc. IEC 61967-4 (1Ω/150Ω method)

**Typ. V<sub>bb</sub> Emissions at PWM-mode with 150Ω-matching network**

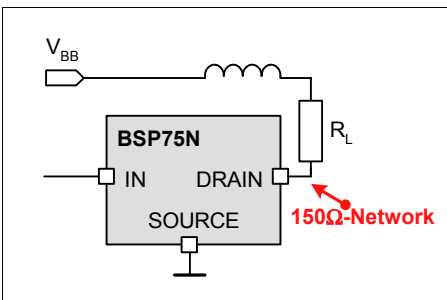
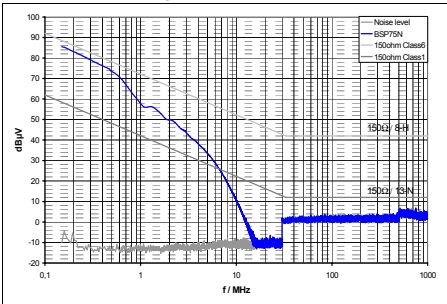


Figure 4 Test circuit for conducted emission 1)

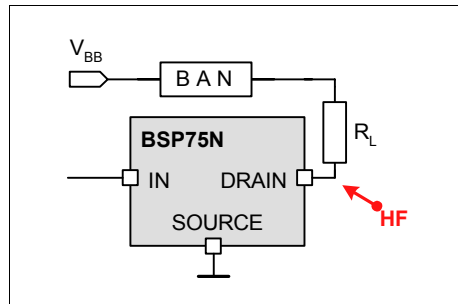
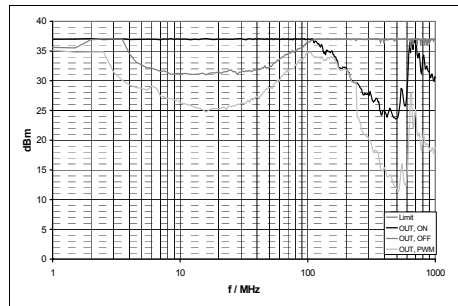
**Conducted Susceptibility**

Acc. 47A/658/CD IEC 62132-4 (Direct Power Injection)

**Direct Power Injection:** Forward Power CW

**Failure Criteria:** Amplitude or frequency variation max. 10% at OUT

**Typ. V<sub>bb</sub> Susceptibility at DC-ON/OFF and at PWM**

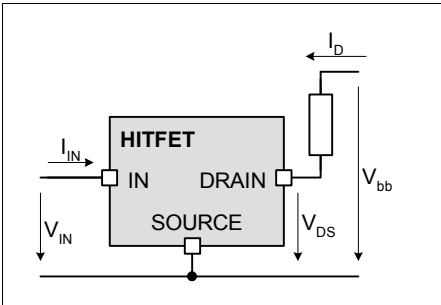


Test circuit for conducted susceptibility 2)

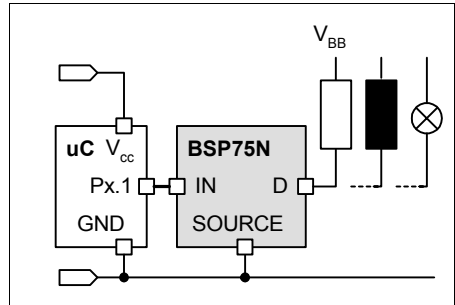
- 1) For defined de coupling and high reproducibility a defined choke (5μH at 1MHz) is inserted in the V<sub>bb</sub>-Line.
- 2) Broadband Artificial Network (short: BAN) consists of the same choke (5μH at 1MHz) and the same 150 Ohm-matching network as for emission measurement for defined de coupling and high reproducibility.



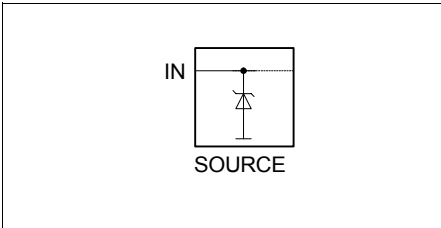
### Block diagram



**Figure 5** Terms

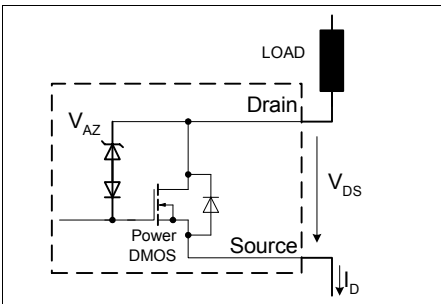


**Figure 8** Application Circuit



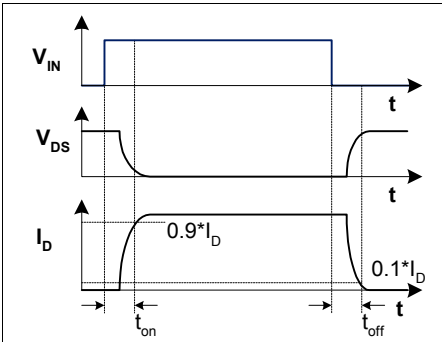
**Figure 6** Input Circuit (ESD protection)

ESD zener diodes are not designed for DC current.

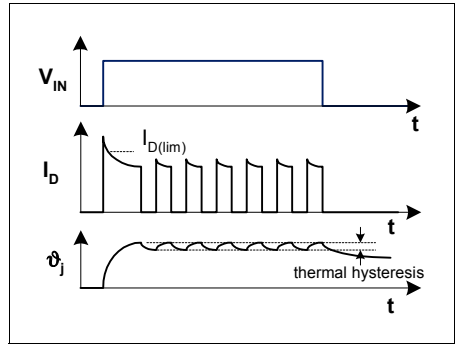


**Figure 7** Inductive and Over voltage Output Clamp

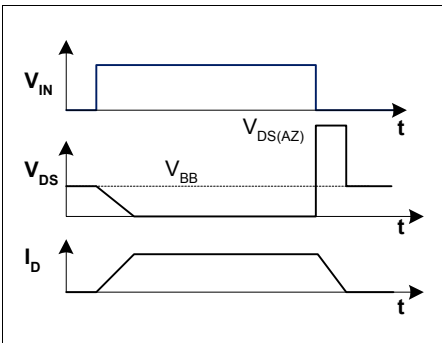
### Timing diagrams



**Figure 9** Switching a Resistive Load



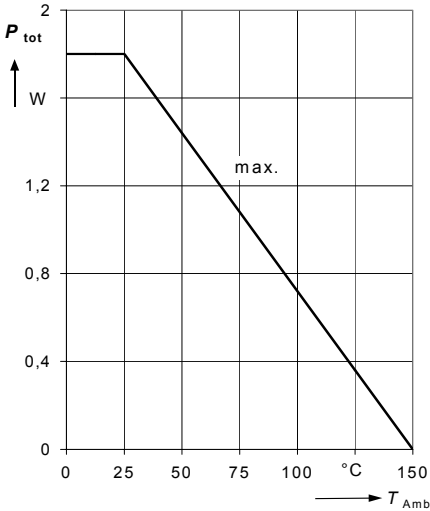
**Figure 11** Short circuit



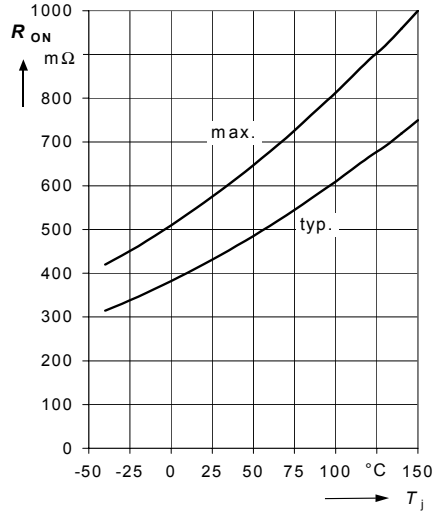
**Figure 10** Switching an Inductive Load

**1 Max. allowable power dissipation**

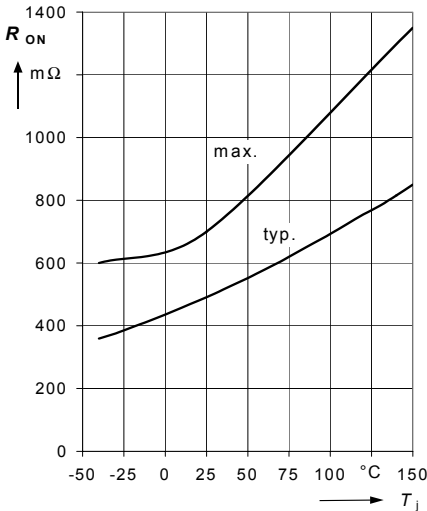
$$P_{\text{tot}} = f(T_{\text{Amb}})$$


**2 On-state resistance  $R_{\text{ON}} = f(T_j)$ ;**

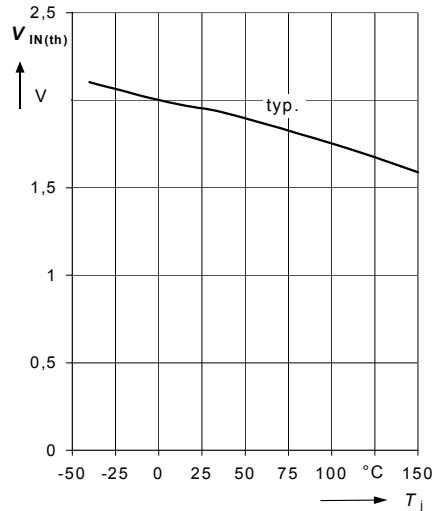
$$I_D = 0.7 \text{ A}; V_{\text{IN}} = 10 \text{ V}$$


**3 On-state resistance  $R_{\text{ON}} = f(T_j)$ ;**

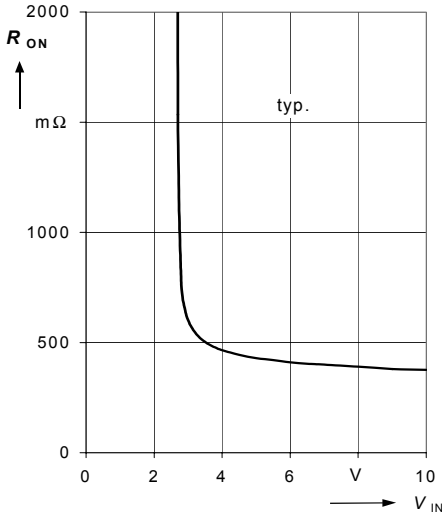
$$I_D = 0.7 \text{ A}; V_{\text{IN}} = 5 \text{ V}$$


**4 Typ. input threshold voltage**

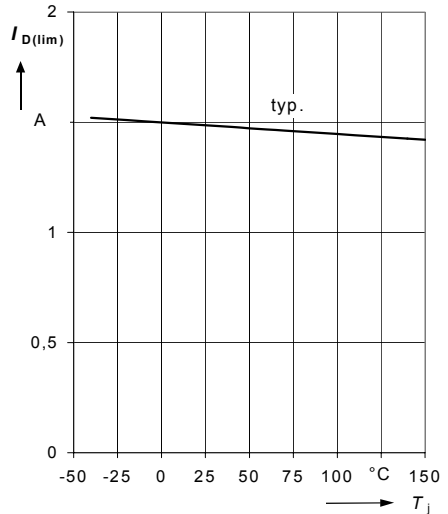
$$V_{\text{IN(th)}} = f(T_j); I_D = 10 \text{ mA}; V_{\text{DS}} = 12 \text{ V}$$



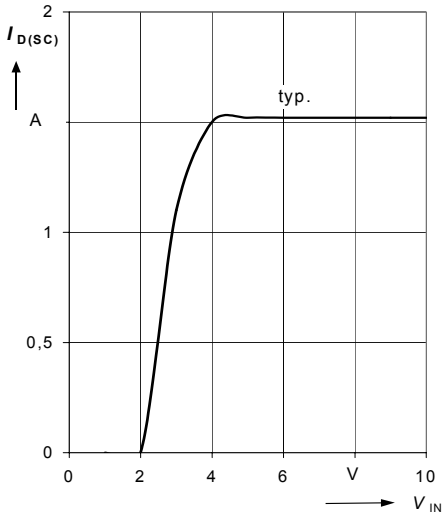
**5 Typ. on-state resistance  $R_{ON} = f(V_{IN})$ ;**  
 $I_D = 0.7 \text{ A}$ ;  $T_j = 25 \text{ °C}$



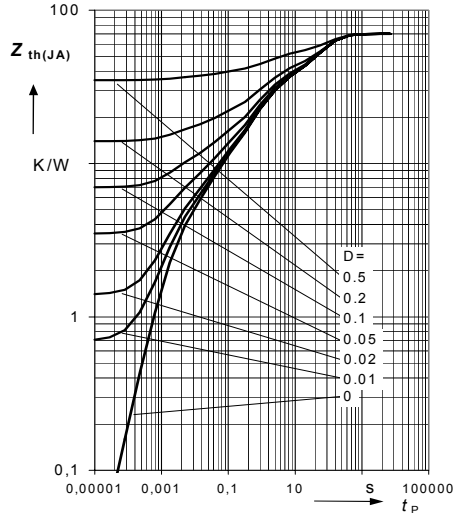
**6 Typ. current limitation  $I_{D(lim)} = f(T_j)$ ;**  
 $V_{DS} = 12 \text{ V}$ ,  $V_{IN} = 10 \text{ V}$

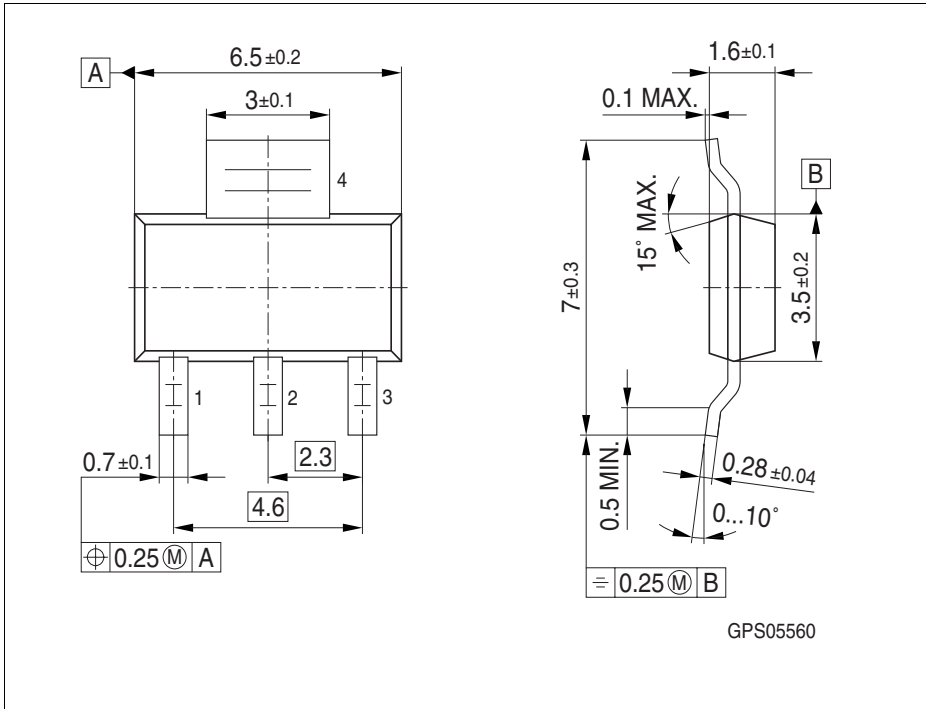


**7 Typ. short circuit current  $I_{D(sc)} = f(V_{IN})$ ;**  
 $V_{DS} = 12 \text{ V}$ ,  $T_j = 25 \text{ °C}$



**8 Max. transient thermal impedance  $Z_{thJA} = f(t_p)$  @  $6\text{cm}^2$ ;** Parameter:  $D = t_p/T$



**1 Package Outlines HITFET® BSP 75N**

**Figure 12 PG-SOT223-4 (Plastic Green Small Outline Transistor Package)**
**Green Product (RoHS compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Please specify the package needed (e.g. green package) when placing an order



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