TVS Diode

Transient Voltage Suppressor Diodes

ESD5V3U2U Series

Uni-directional Ultra Low ESD / Transient Protection Diode

ESD5V3U2U-03F
ESD5V3U2U-03LRH

Data Sheet

Revision 1.3, 2013-08-16
Final

Power Management & Multimarket

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Revision History: Rev. 1.2, 2013-08-16	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.3, 2013-08-16	
4 + 16	All marking infos for TSLP-3-7 updated

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Last Trademarks Update 2010-10-26

1 Uni-directional Ultra Low ESD / Transient Protection Diode

1.1 Features

- ESD / Transient protection of High-Speed data lines exceeding
  - **IEC61000-4-2 (ESD): ± 20 kV (air / contact)**
  - **IEC61000-4-4 (EFT): ±50 A (5/50 ns)**
  - **IEC61000-4-5 (surge): ±3 A (8/20 µs)**
- Maximum working voltage: V_{RWM} **5.3 V**
- Extremely low capacitance: down to 0.4 pF
- Very low reverse current: I_R < 1 nA typical
- Pb-free package (RoHS compliant) and halogen free package

1.2 Application Examples

- ESD / Transient protection of High Speed Interfaces:
  - HDMI, USB 2.0/USB 3.0, DisplayPort, DVI
  - Mobile HDMI Link, MDDI, MIPI.
  - 10/100/1000 Ethernet, Firewire, S-ATA, etc.

1.3 Product Description

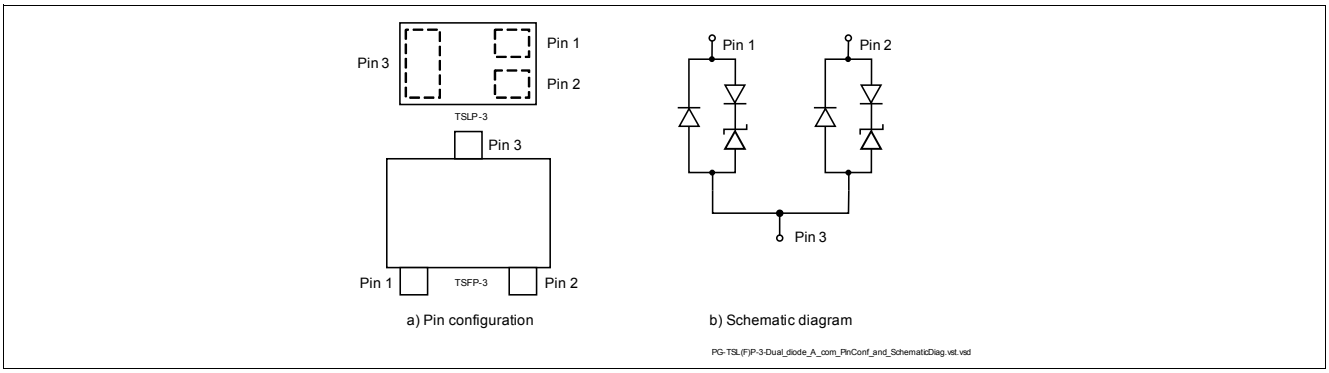

Figure 1-1 Pin Configuration (a) and Schematic Diagram (b)

Table 1-1 Ordering information

Type	Package	Configuration	Marking code
ESD5V3U2U-03F	PG-TSFP-3-1	2 lines, uni-directional[1)]	Z1
ESD5V3U2U-03LRH	PG-TSLP-3-7	2 lines, uni-directional[1)]	Z1

1) Or 1 line, bi-directional between pins 1 and 2, if pin 3 is not connected

2 Characteristics

Table 2-1 Maximum Rating at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD (air / contact) discharge[1)]	V_{ESD}	-20	–	20	kV
Peak pulse current (t_p = 8/20 µs)[2)]	I_{PP}	-3	–	3	A
Operating temperature range	T_{OP}	-40	–	125	°C
Storage temperage	T_{stg}	-65	–	150	°C

1) V_{ESD} according to IEC61000-4-2

2) I_{PP} according to IEC61000-4-5

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

2.1 Electrical Characteristics at T_A = 25 °C, unless otherwise specified

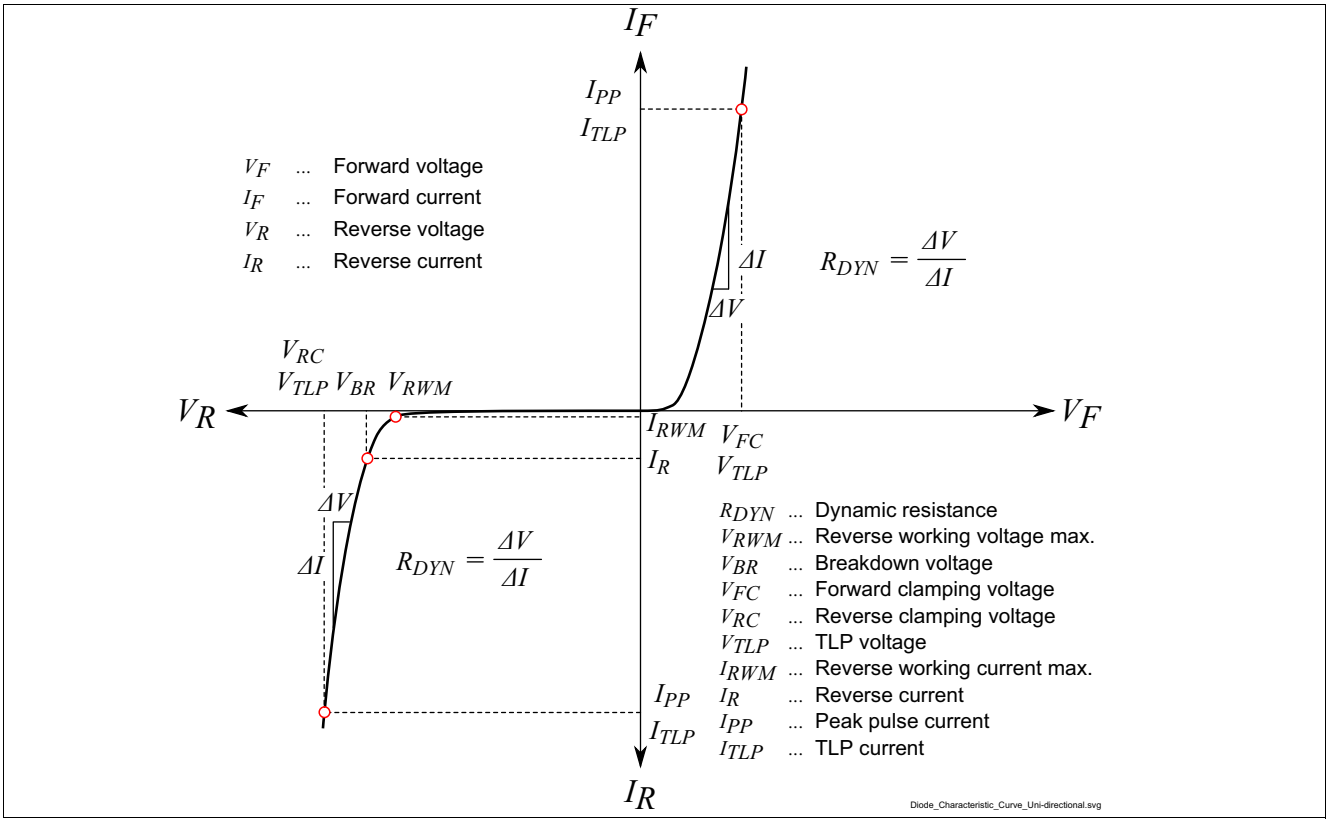

Figure 2-1 Definitions of electrical characteristics

Table 2-2 DC characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	–	–	5.3	V	
Breakdown voltage	V_{BR}	6	–	–	V	I_{BR} = 1 mA, from Pin 1/2 to Pin 3
Reverse current	I_R	–	<1	50	nA	V_R = 5.3 V, from Pin 1/2 to Pin 3

Table 2-3 RF characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance[1)]	C_L	–	0.4	0.6	pF	V_R = 0 V, f = 1 MHz from pin 1/2 to pin 3
		–	0.2	0.4	pF	V_R = 0 V, f = 1 MHz from pin 1 to 2, pin 3[1)] not connected

1) Total capacitance line to ground

Table 2-4 ESD Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage[1)]	V_{CL}	–	19	–	V	I_{TLP} = 16 A, from Pin 1/2 to Pin 3
		–	28	–	V	I_{TLP} = 30 A, from Pin 1/2 to Pin 3
Forward clamping voltage[1)]	V_{FC}	–	10	–	V	I_{TLP} = 16 A, from Pin 3 to Pin 1/2
		–	17	–	V	I_{TLP} = 30 A, from Pin 3 to Pin 1/2
Dynamic resistance[1)]	R_{DYN}	–	0.6	–	V	Pin 1/2 to Pin 3
		–	0.4	–	V	Pin 3 to Pin 1/2

1)Please refer to Application Note AN210[1]. TLP parameter: Z_0 = 50 Ω , t_p = 100ns, t_r = 300ps, averaging window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using least squares fit of TLP charactertistics between I_{PP1} = 10 A and I_{PP2} = 40 A.

Table 2-5 Surge characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage	V_{CL}	–	10	13	V	I_{PP} = 1 A, t_p=8/20 µs[1] from Pin 1/2 to Pin 3
		–	12	15	V	I_{PP} = 3A, t_p =8/20 µs[1] from Pin 1/2 to Pin 3
Forward clamping voltage	V_{FC}	–	2	4	V	I_{PP} = 1 A, t_p =8/20 µs[1] from Pin 3 to Pin 1/2
		–	4	6	V	I_{PP} = 3A, t_p =8/20 µs[1] from Pin 3to Pin 1/2

1) I_{PP} according to IEC61000-4-5

3 Typical characteristics

Typical characteristics at = 25 °C, unless otherwise specified

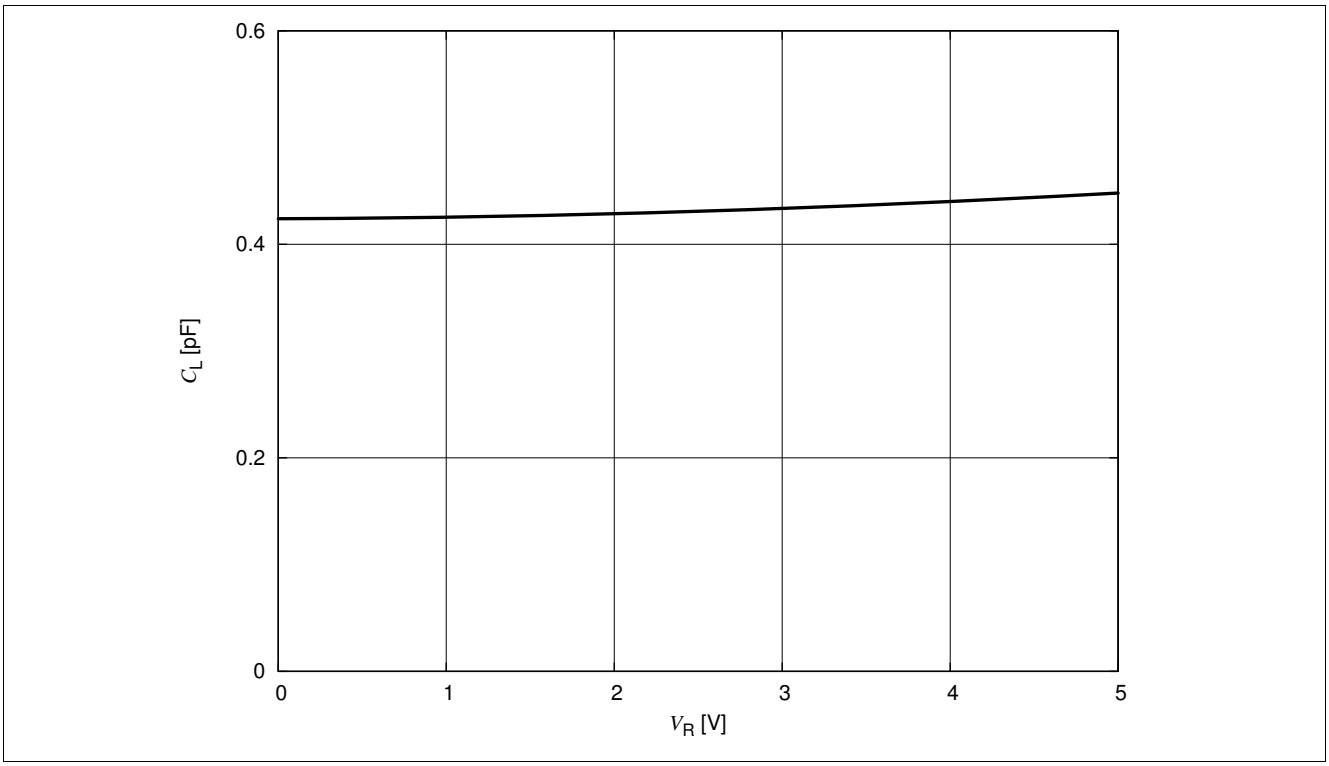

Figure 3-1 Line capacitance $C_L=f(V_R)$, from pin 1/2 to 3, f = 1 MHz

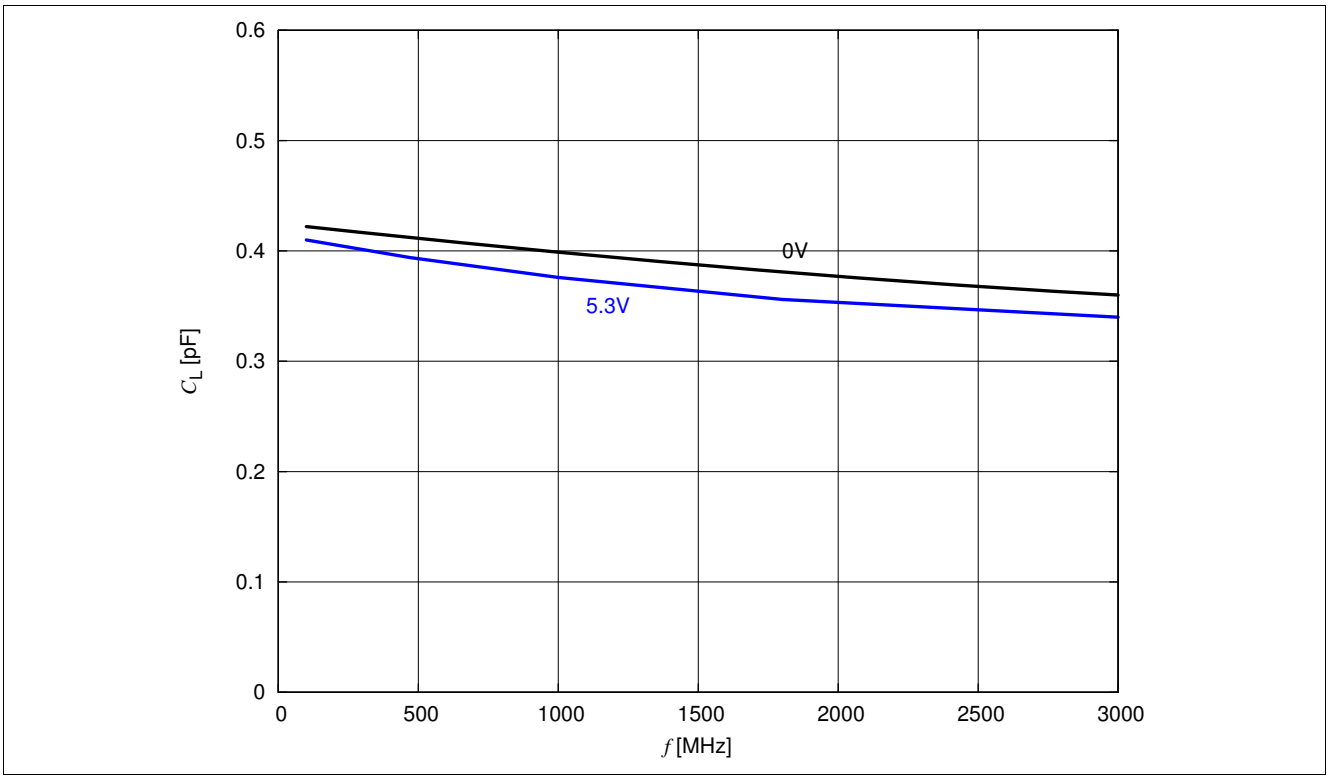

Figure 3-2 Line capacitance $C_L=f(f)$, from pin 1/2 to 3

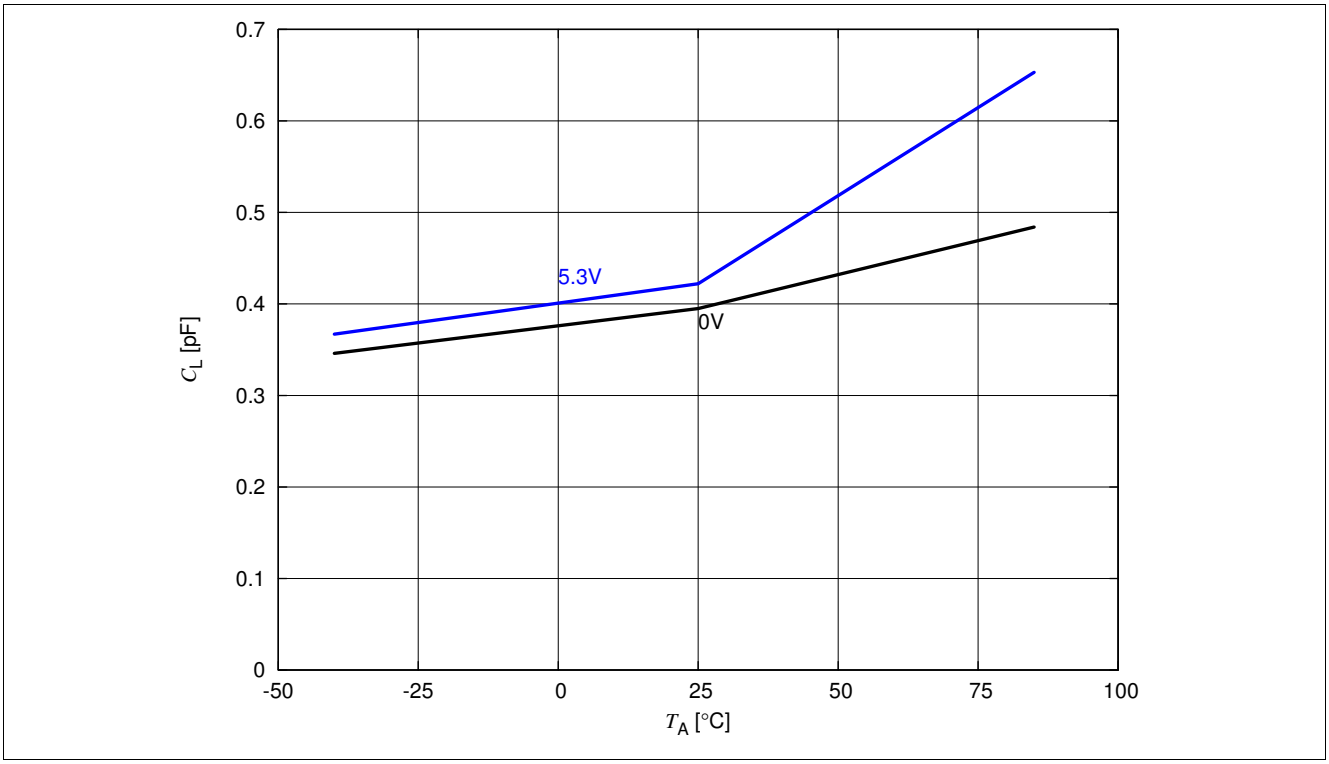

Figure 3-3 Line capacitance $C_L=f(T_A)$

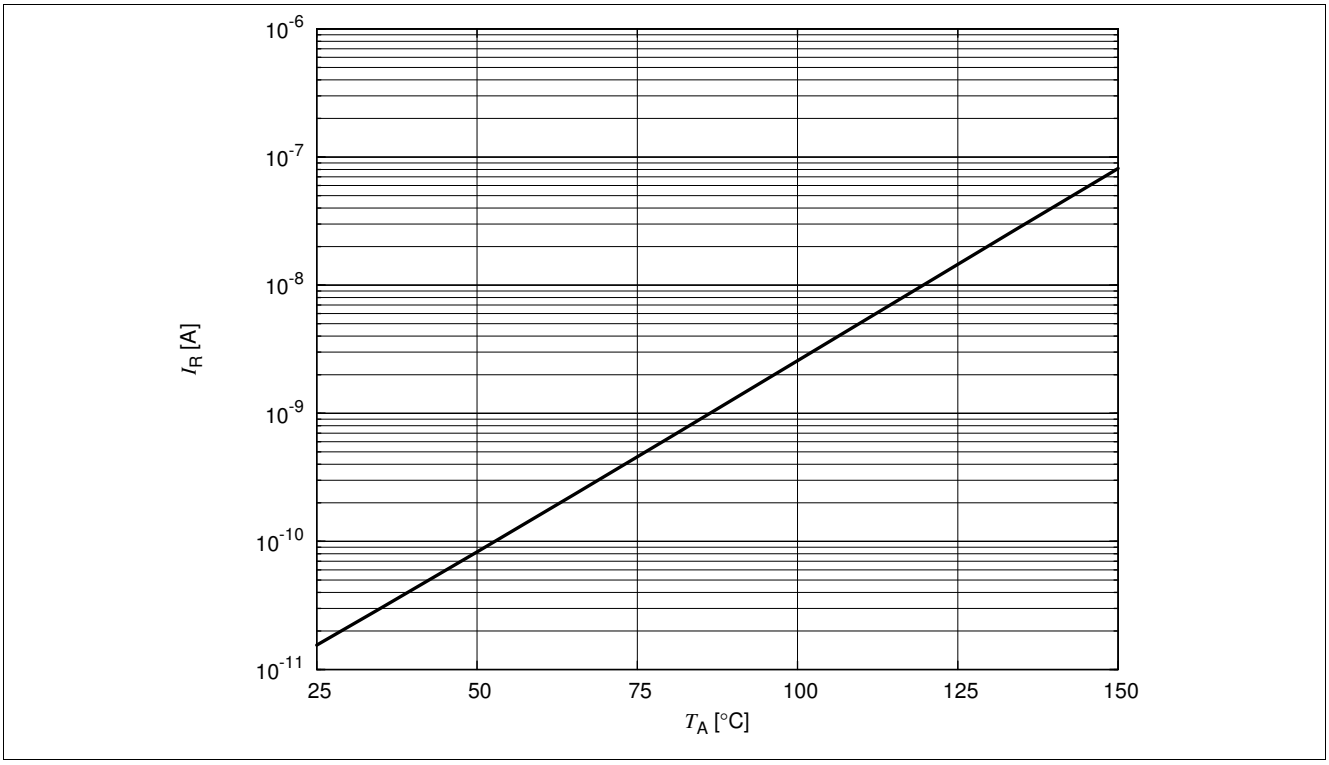

Figure 3-4 Reverse current $I_R=f(T_A)$, V_R=5.3 V, from pin 1/2 to pin 3

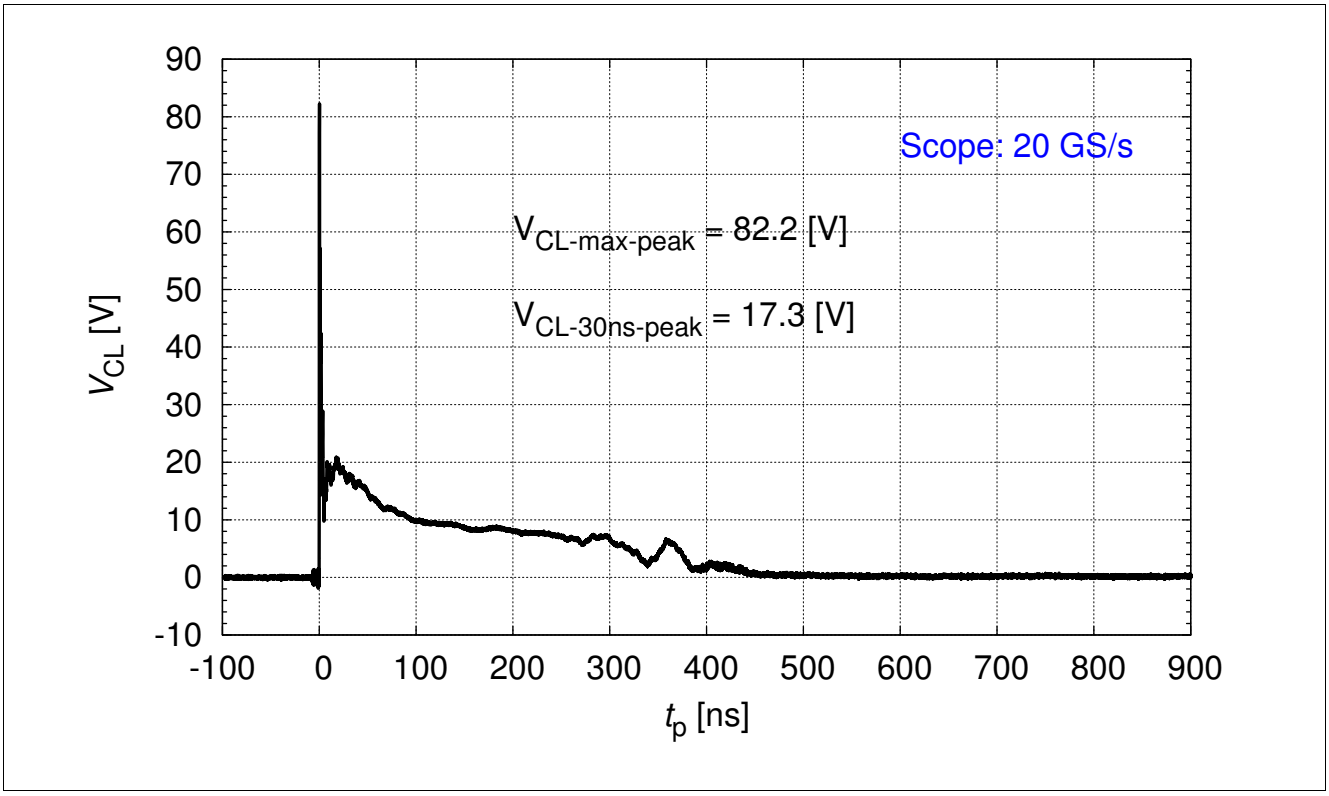

Figure 3-5 IEC61000-4-2: $V_{CL} = f(t)$, 8 kV positive pulse from pin 1 to pin 2 (R = 330 Ω, C = 150 pF)

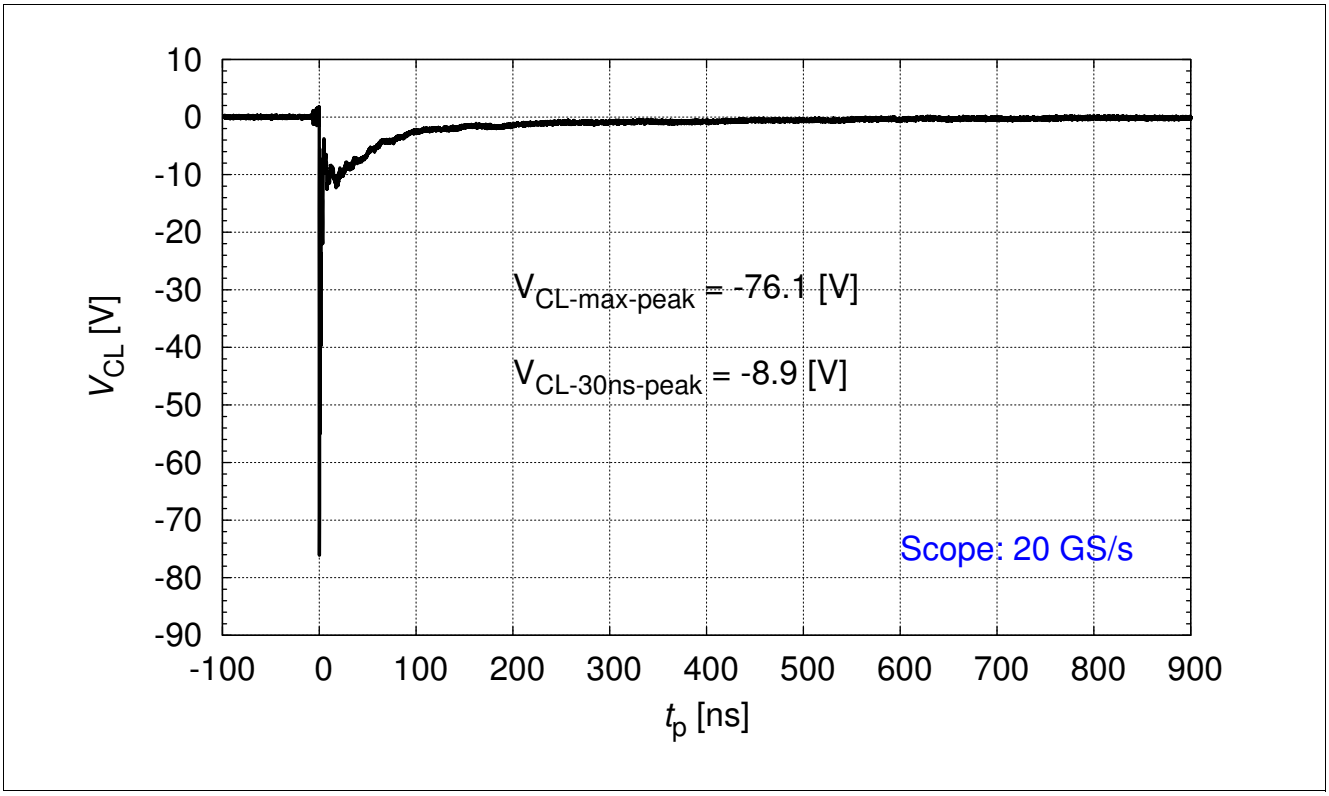

Figure 3-6 IEC61000-4-2: $V_{CL} = f(t)$, 8 kV negative pulse from pin 1 to pin 2 (R = 330 Ω, C = 150 pF)

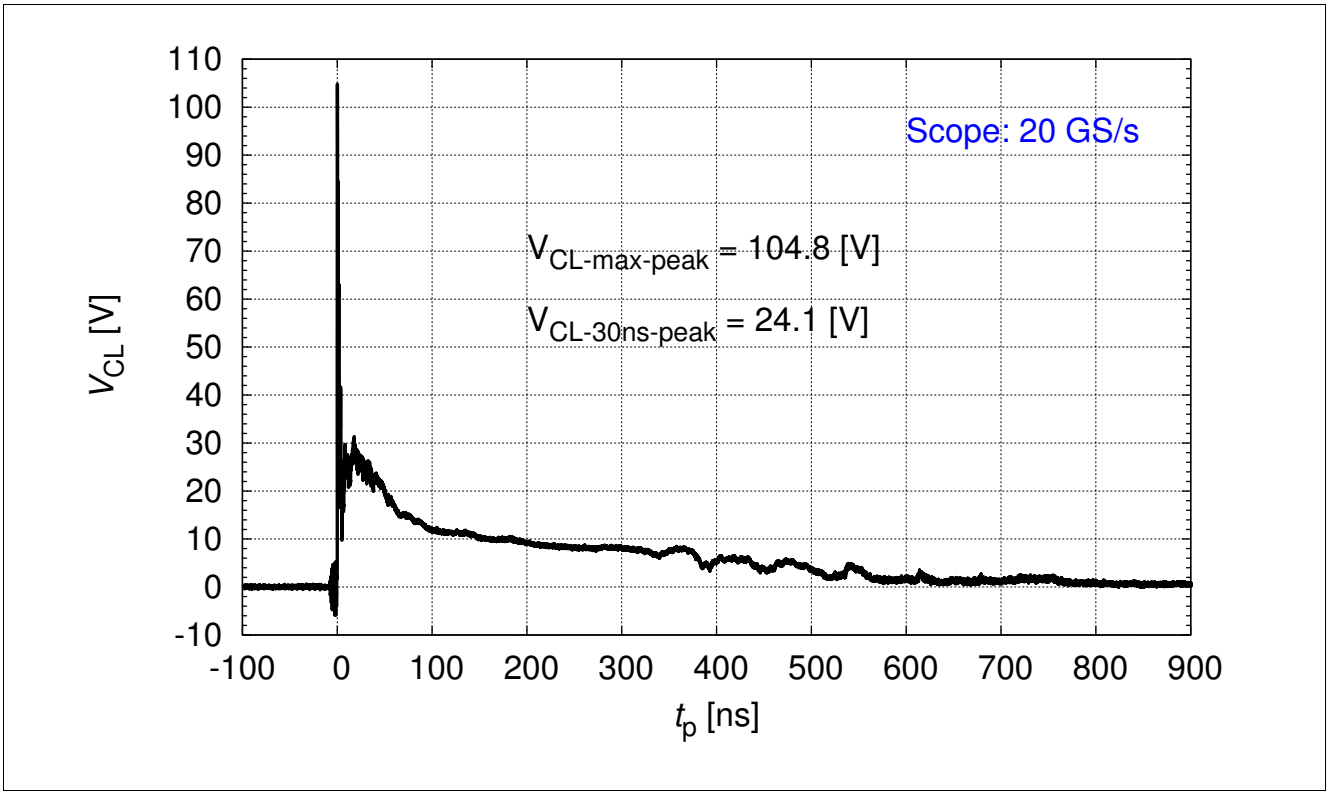

Figure 3-7 IEC61000-4-2: $V_{CL} = f(t)$, 15 kV positive pulse from pin 1 to pin 2 (R = 330 Ω, C = 150 pF)

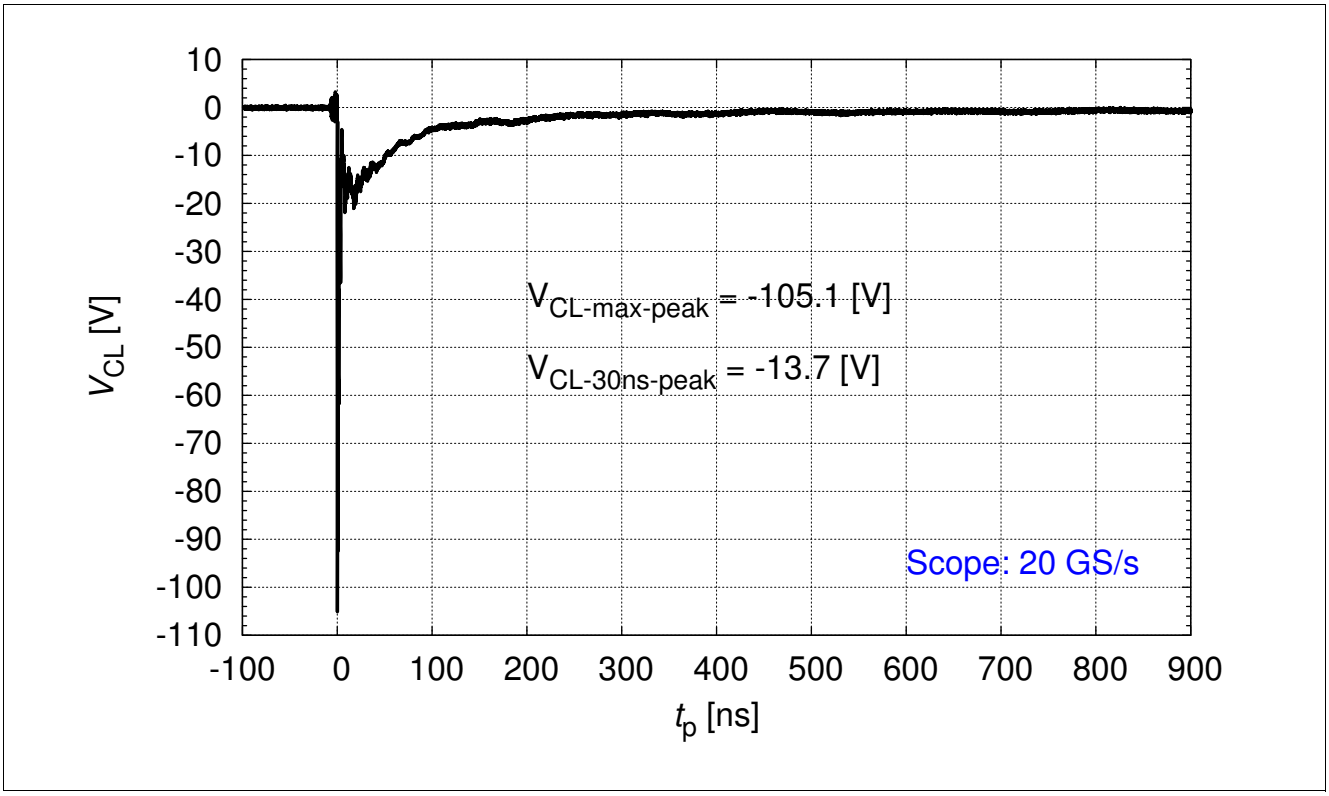

Figure 3-8 IEC61000-4-2: $V_{CL} = f(t)$, 15 kV negative pulse from pin 1 to pin 2 (R = 330 Ω, C = 150 pF)

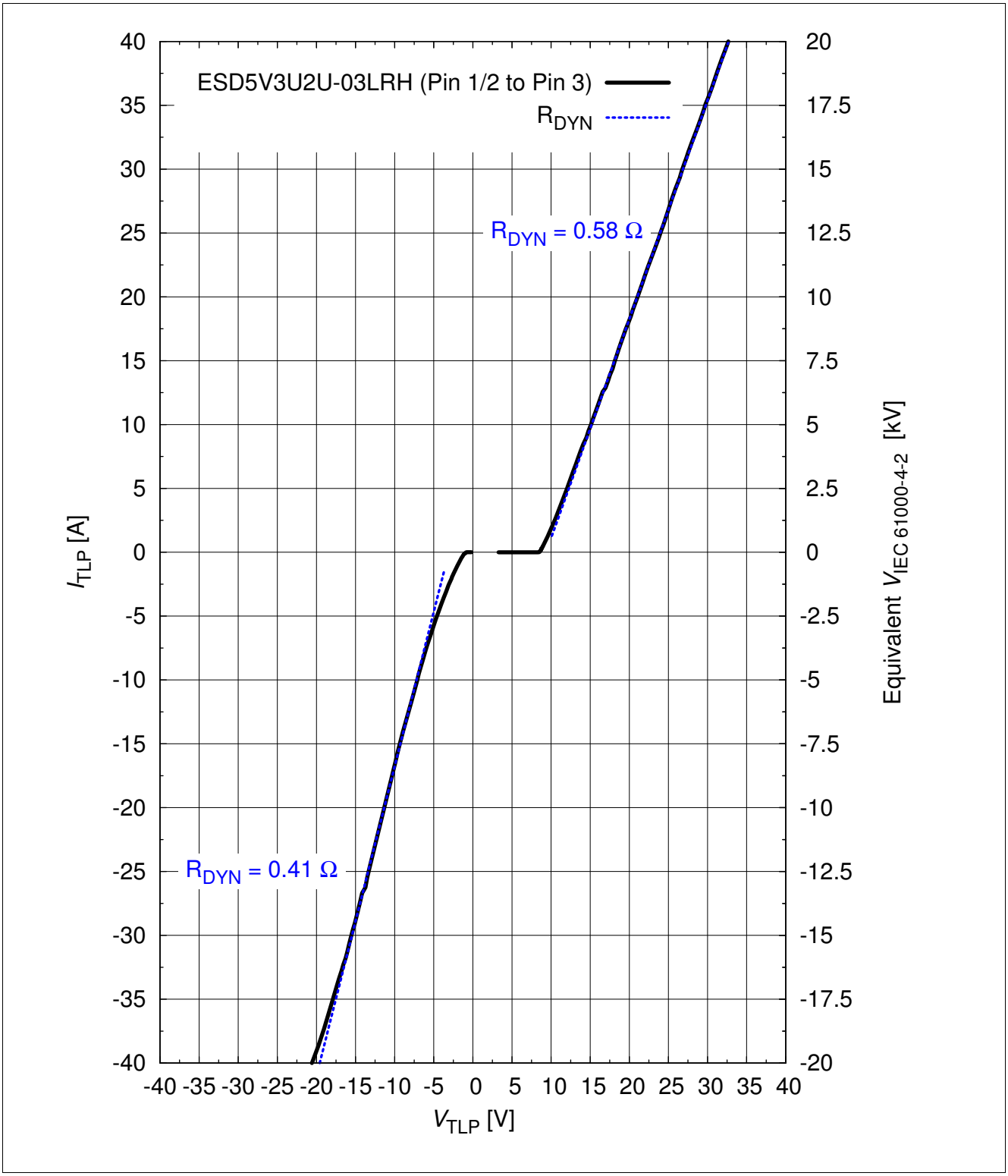

Figure 3-9 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ according ANSI/ESD STM5.5.1- Electrostatic Dischange Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 0.6 ns, I_{TLP} and V_{TLP} averaging window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using squares fit to ELP characterisitic between I_{TLP1} = 10 A and I_{TLP2} = 30 A. Please refer to Application Note AN210 [1]

4 Application Information

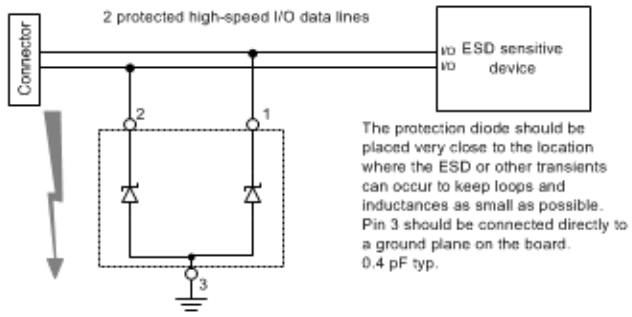

Figure 4-1 2 lines, uni-directional TVS protection

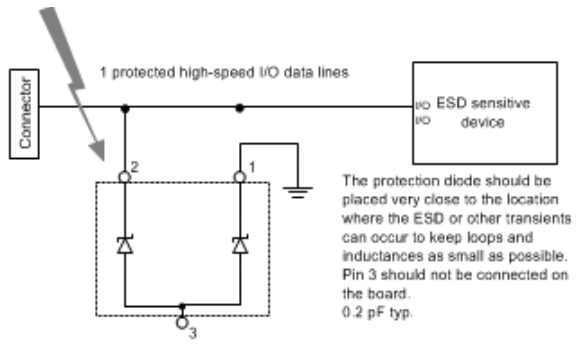

Figure 4-2 1 line, bi-directional TVS protection

5 Ordering information scheme (examples)

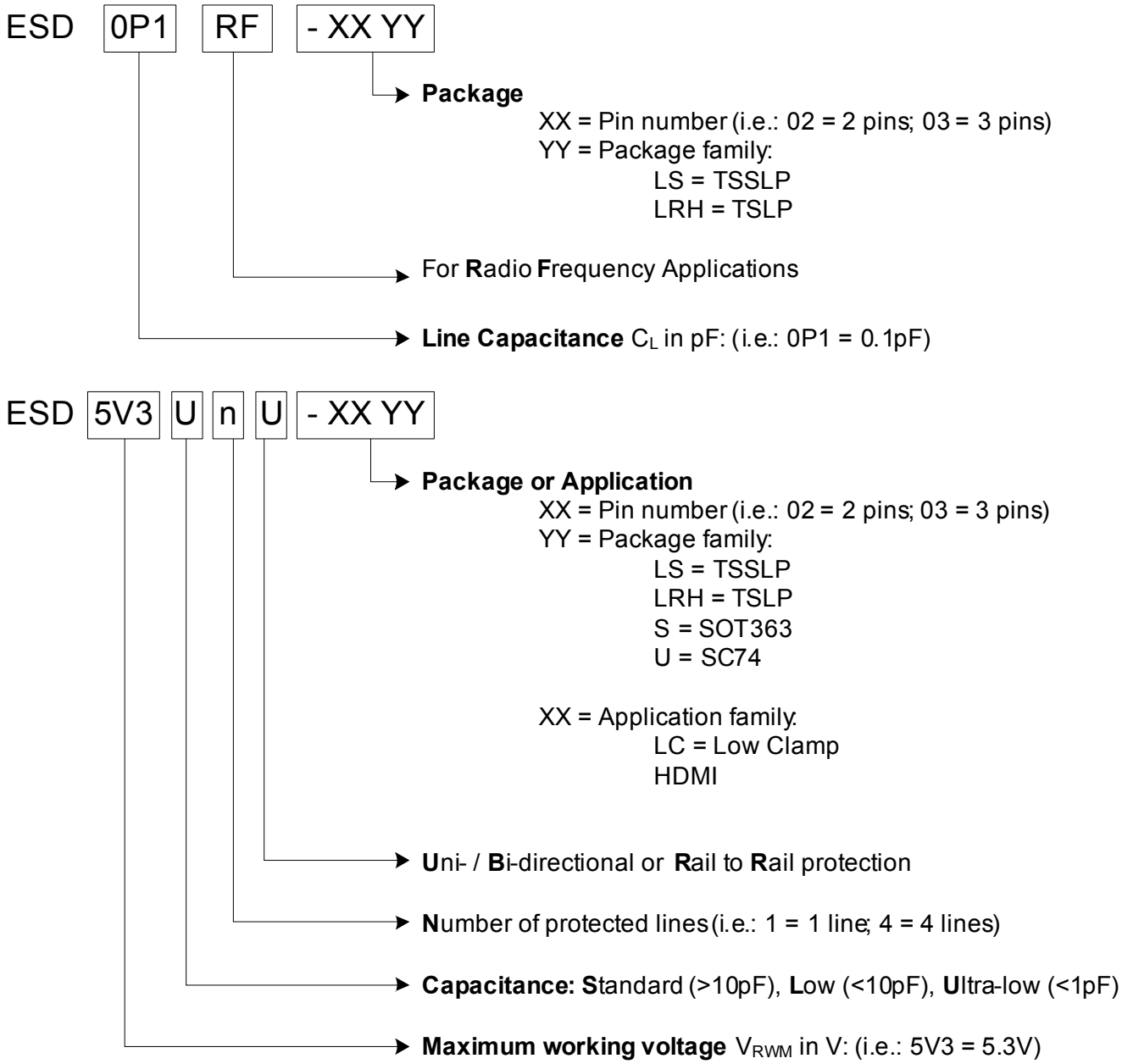

Figure 5-1 Ordering Information Scheme

6 Package Information

6.1 PG-TSFP-3-1

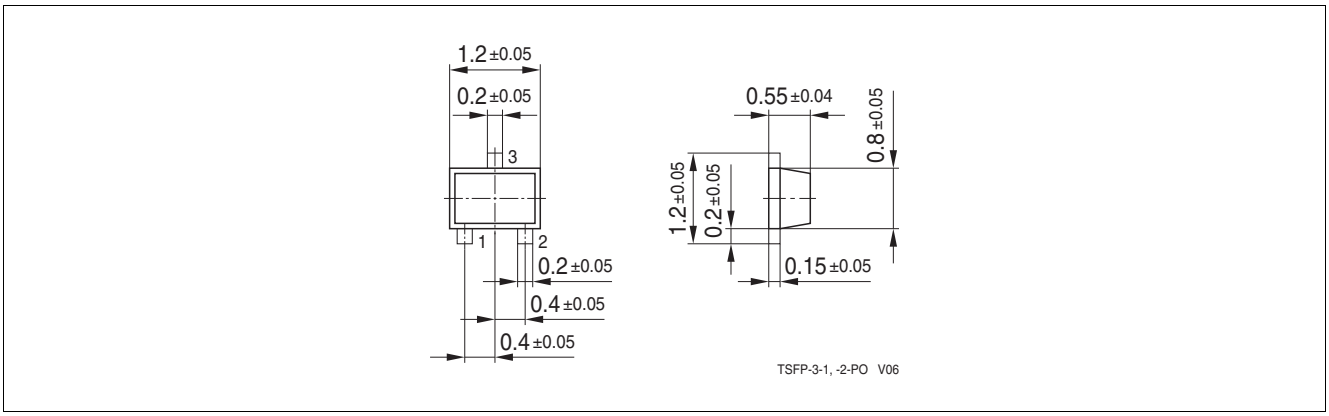

Figure 6-1 PG-TSFP-3-1: Package Overview

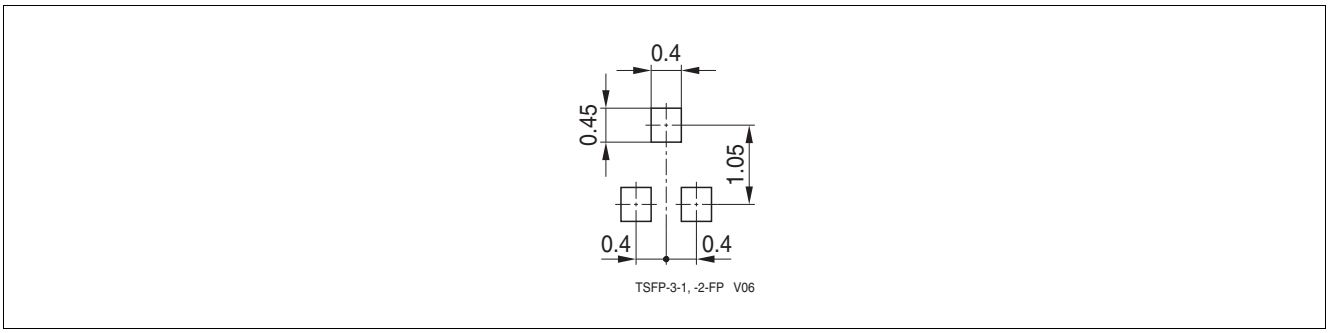

Figure 6-2 PG-TSFP-3-1: Footprint

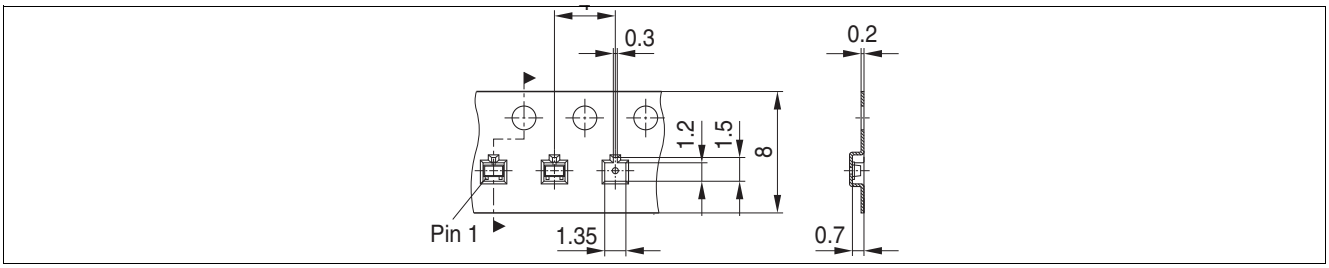

Figure 6-3 PG-TSFP-3-1: Packing

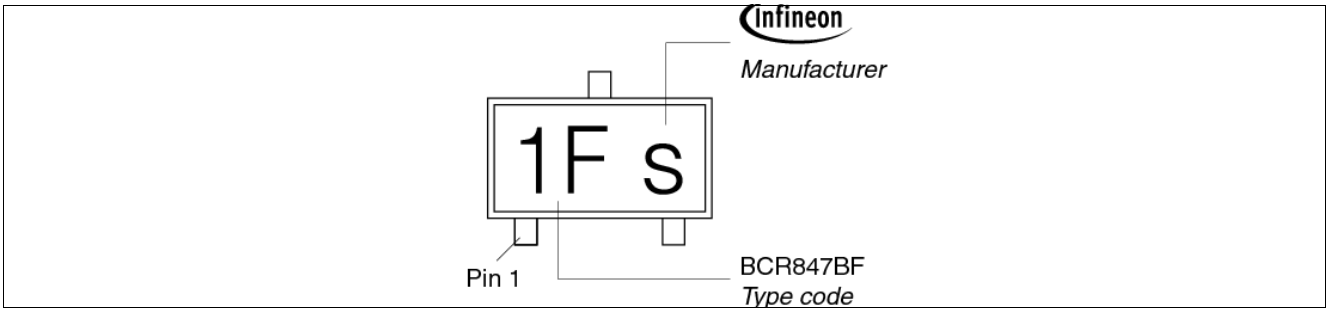

Figure 6-4 PG-TSFP-3-1: Marking (example)

6.2 PG-TSLP-3-7

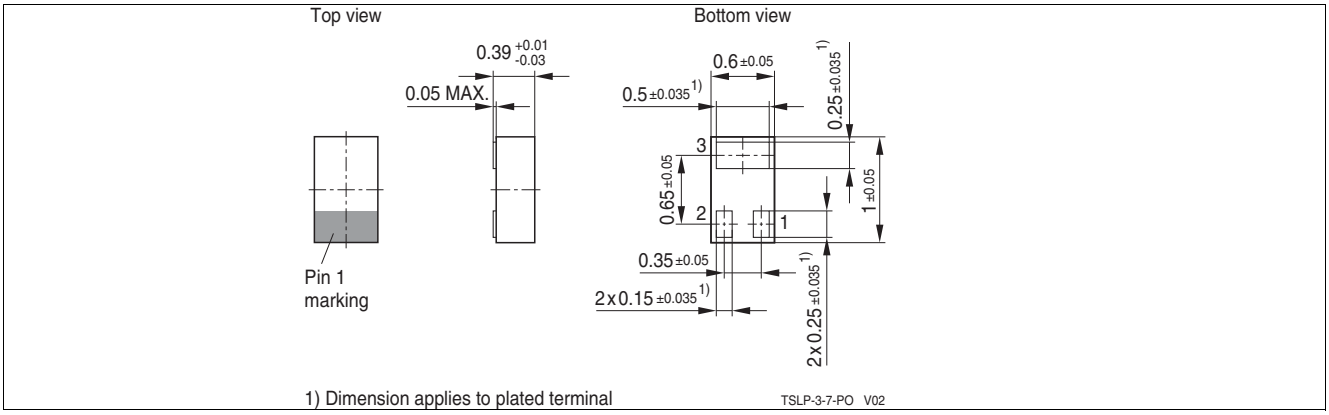

Figure 6-5 PG-TSLP-3-7: Package Overview

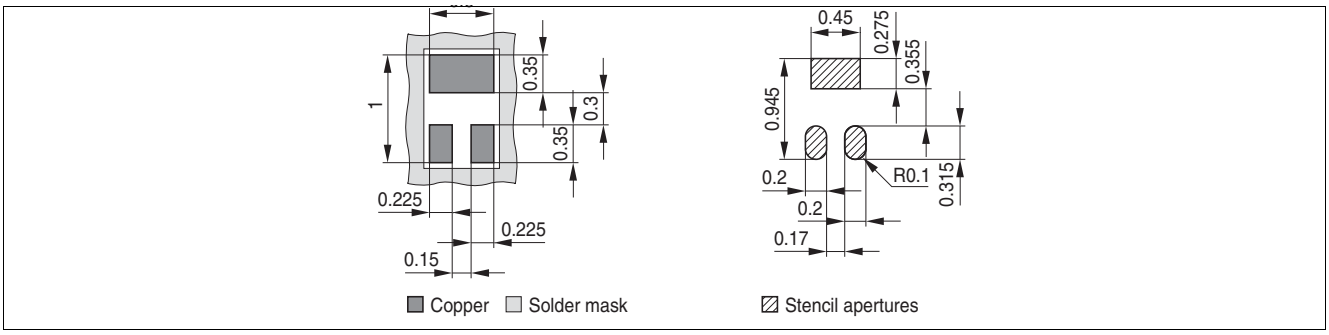

Figure 6-6 PG-TSLP-3-7: Footprint

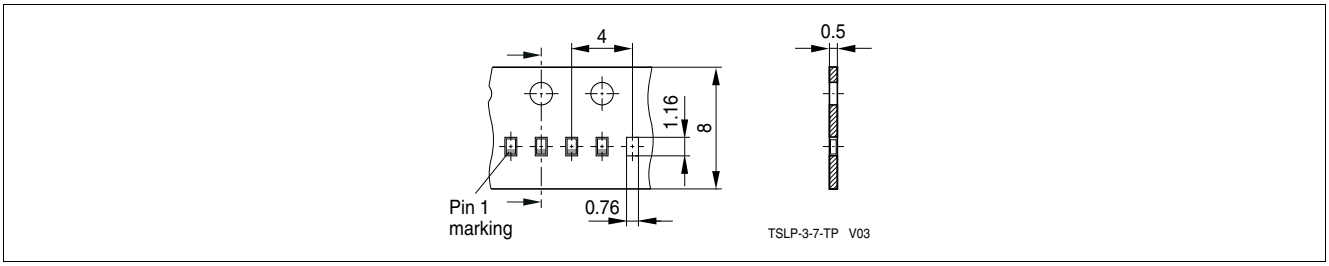

Figure 6-7 PG-TSLP-3-7: Packing

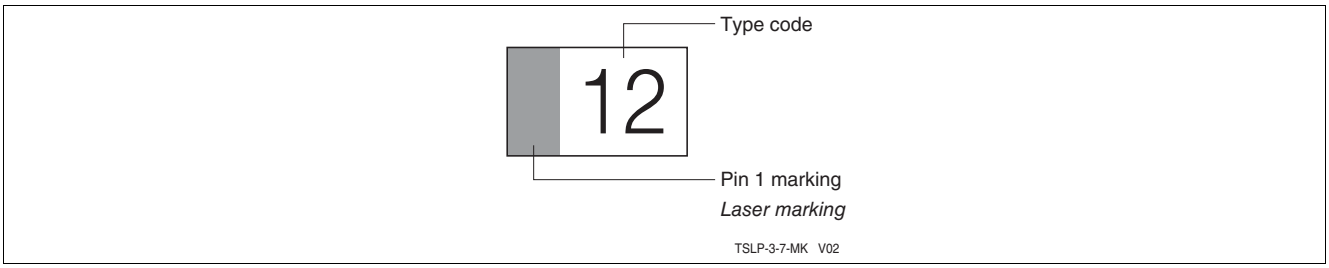

Figure 6-8 PG-TSLP-3-7: Marking (example)

References

[1] Infineon Technologie AG - **Application Note AN210**: Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology

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