

MOSFET

800V CoolMOS™ P7 Power Transistor

The latest 800V CoolMOS™ P7 series sets a new benchmark in 800V super junction technologies and combines best-in-class performance with state of the art ease-of-use, resulting from Infineon's over 18 years pioneering super junction technology innovation.

Features

- Best-in-class FOM $R_{DS(on)} * E_{oss}$; reduced Q_g , C_{iss} , and C_{oss}
- Best-in-class DPAK $R_{DS(on)}$
- Best-in-class $V_{(GS)th}$ of 3V and smallest $V_{(GS)th}$ variation of $\pm 0.5V$
- Integrated Zener Diode ESD protection
- Best-in-class CoolMOS™ quality and reliability; qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)
- Fully optimized portfolio

Benefits

- Best-in-class performance
- Enabling higher power density designs, BOM savings and lower assembly costs
- Easy to drive and to parallel
- Better production yield by reducing ESD related failures
- Less production issues and reduced field returns
- Easy to select right parts for fine tuning of designs

Applications

Recommended for hard and soft switching flyback topologies for LED Lighting, low power Chargers and Adapters, Audio, AUX power and Industrial power. Also suitable for PFC stage in Consumer applications and Solar.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

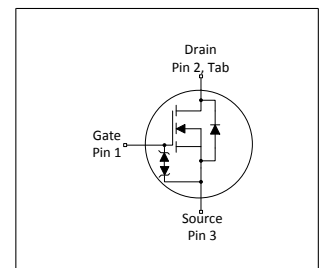
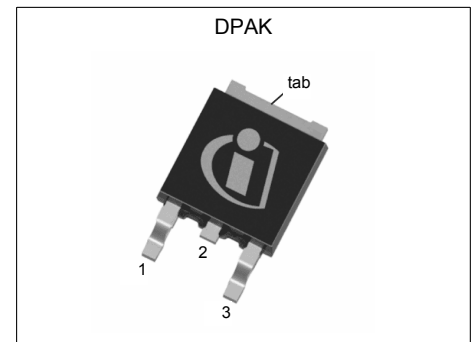


Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|----------------------------|-------|----------|
| $V_{DS} @ T_J=25^{\circ}C$ | 800 | V |
| $R_{DS(on),max}$ | 0.45 | Ω |
| $Q_{g,typ}$ | 24 | nC |
| I_D | 11 | A |
| $E_{oss} @ 500V$ | 2.7 | μJ |
| $V_{GS(th),typ}$ | 3 | V |
| ESD class (HBM) | 2 | - |

| Type / Ordering Code | Package | Marking | Related Links |
|----------------------|-----------|----------|----------------|
| IPD80R450P7 | PG-TO 252 | 80R450P7 | see Appendix A |

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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|----------------|------------|------|-----------|------------------|---|
| | | Min. | Typ. | Max. | | |
| Continuous drain current ¹⁾ | I_D | - | - | 11 7.1 | A | $T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$ |
| Pulsed drain current ²⁾ | $I_{D,pulse}$ | - | - | 29 | A | $T_C=25^\circ\text{C}$ |
| Avalanche energy, single pulse | E_{AS} | - | - | 29 | mJ | $I_D=1.8\text{A}$; $V_{DD}=50\text{V}$ |
| Avalanche energy, repetitive | E_{AR} | - | - | 0.22 | mJ | $I_D=1.8\text{A}$; $V_{DD}=50\text{V}$ |
| Avalanche current, repetitive | I_{AR} | - | - | 1.8 | A | - |
| MOSFET dv/dt ruggedness | dv/dt | - | - | 100 | V/ns | $V_{DS}=0$ to 400V |
| Gate source voltage | V_{GS} | -20 -30 | - | 20 30 | V | static; AC ($f>1$ Hz) |
| Power dissipation | P_{tot} | - | - | 73 | W | $T_C=25^\circ\text{C}$ |
| Operating and storage temperature | T_j, T_{stg} | -55 | - | 150 | $^\circ\text{C}$ | - |
| Continuous diode forward current | I_S | - | - | 8 | A | $T_C=25^\circ\text{C}$ |
| Diode pulse current ²⁾ | $I_{S,pulse}$ | - | - | 29 | A | $T_C=25^\circ\text{C}$ |
| Reverse diode dv/dt ³⁾ | dv/dt | - | - | 1 | V/ns | $V_{DS}=0$ to 400V, $I_{SD}\leq 2.2\text{A}$, $T_j=25^\circ\text{C}$ |
| Maximum diode commutation speed ³⁾ | di/dt | - | - | 50 | A/ μs | $V_{DS}=0$ to 400V, $I_{SD}\leq 2.2\text{A}$, $T_j=25^\circ\text{C}$ |

2 Thermal characteristics

Table 3 Thermal characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|------------|--------|------|------|--------------------|--|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | R_{thJC} | - | - | 1.7 | $^\circ\text{C/W}$ | - |
| Thermal resistance, junction - ambient | R_{thJA} | - | - | 62 | $^\circ\text{C/W}$ | Device on PCB, minimal footprint |
| Thermal resistance, junction - ambient for SMD version | R_{thJA} | - | 35 | 45 | $^\circ\text{C/W}$ | Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm ² (one layer 70 μm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling. |
| Soldering temperature, wave- & reflow soldering allowed | T_{sold} | - | - | 260 | $^\circ\text{C}$ | reflow MSL1 |

1) Limited by $T_{j,max}$. Maximum duty cycle $D=0.5$

2) Pulse width t_p limited by $T_{j,max}$

3) $V_{DClink}=400\text{V}$; $V_{DS,peak}<V_{(BR)DSS}$; identical low side and high side switch with identical R_G ; $t_{cond}<2\mu\text{s}$

3 Electrical characteristics

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---------------|--------|------|------|---------------|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 800 | - | - | V | $V_{GS}=0V, I_D=1mA$ |
| Gate threshold voltage | $V_{GS(th)}$ | 2.5 | 3 | 3.5 | V | $V_{DS}=V_{GS}, I_D=0.22mA$ |
| Zero gate voltage drain current | I_{DSS} | - | - | 1 | μA | $V_{DS}=800V, V_{GS}=0V, T_j=25^\circ\text{C}$ $V_{DS}=800V, V_{GS}=0V, T_j=150^\circ\text{C}$ |
| Gate-source leakage current incl. zener diode | I_{GSS} | - | - | 1 | μA | $V_{GS}=20V, V_{DS}=0V$ |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 0.38 | 0.45 | Ω | $V_{GS}=10V, I_D=4.5A, T_j=25^\circ\text{C}$ $V_{GS}=10V, I_D=4.5A, T_j=150^\circ\text{C}$ |
| Gate resistance | R_G | - | 1 | - | Ω | $f=250kHz, \text{open drain}$ |

Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|--------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance | C_{iss} | - | 770 | - | pF | $V_{GS}=0V, V_{DS}=500V, f=250kHz$ |
| Output capacitance | C_{oss} | - | 14 | - | pF | $V_{GS}=0V, V_{DS}=500V, f=250kHz$ |
| Effective output capacitance, energy related ¹⁾ | $C_{o(er)}$ | - | 24 | - | pF | $V_{GS}=0V, V_{DS}=0 \text{ to } 500V$ |
| Effective output capacitance, time related ²⁾ | $C_{o(tr)}$ | - | 305 | - | pF | $I_D=\text{constant}, V_{GS}=0V, V_{DS}=0 \text{ to } 500V$ |
| Turn-on delay time | $t_{d(on)}$ | - | 10 | - | ns | $V_{DD}=400V, V_{GS}=13V, I_D=4.5A, R_G=7.5\Omega$ |
| Rise time | t_r | - | 6 | - | ns | $V_{DD}=400V, V_{GS}=13V, I_D=4.5A, R_G=7.5\Omega$ |
| Turn-off delay time | $t_{d(off)}$ | - | 40 | - | ns | $V_{DD}=400V, V_{GS}=13V, I_D=4.5A, R_G=7.5\Omega$ |
| Fall time | t_f | - | 10 | - | ns | $V_{DD}=400V, V_{GS}=13V, I_D=4.5A, R_G=7.5\Omega$ |

Table 6 Gate charge characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-----------------------|---------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | Q_{gs} | - | 4 | - | nC | $V_{DD}=640V, I_D=4.5A, V_{GS}=0 \text{ to } 10V$ |
| Gate to drain charge | Q_{gd} | - | 9 | - | nC | $V_{DD}=640V, I_D=4.5A, V_{GS}=0 \text{ to } 10V$ |
| Gate charge total | Q_g | - | 24 | - | nC | $V_{DD}=640V, I_D=4.5A, V_{GS}=0 \text{ to } 10V$ |
| Gate plateau voltage | $V_{plateau}$ | - | 4.5 | - | V | $V_{DD}=640V, I_D=4.5A, V_{GS}=0 \text{ to } 10V$ |

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 500V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 500V

Table 7 Reverse diode characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-------------------------------|-----------|--------|------|------|---------|---|
| | | Min. | Typ. | Max. | | |
| Diode forward voltage | V_{SD} | - | 0.9 | - | V | $V_{GS}=0V, I_F=4.5A, T_i=25^\circ C$ |
| Reverse recovery time | t_{rr} | - | 1000 | - | ns | $V_R=400V, I_F=2.2A, di_F/dt=50A/\mu s$ |
| Reverse recovery charge | Q_{rr} | - | 11 | - | μC | $V_R=400V, I_F=2.2A, di_F/dt=50A/\mu s$ |
| Peak reverse recovery current | I_{rrm} | - | 17 | - | A | $V_R=400V, I_F=2.2A, di_F/dt=50A/\mu s$ |

4 Electrical characteristics diagrams

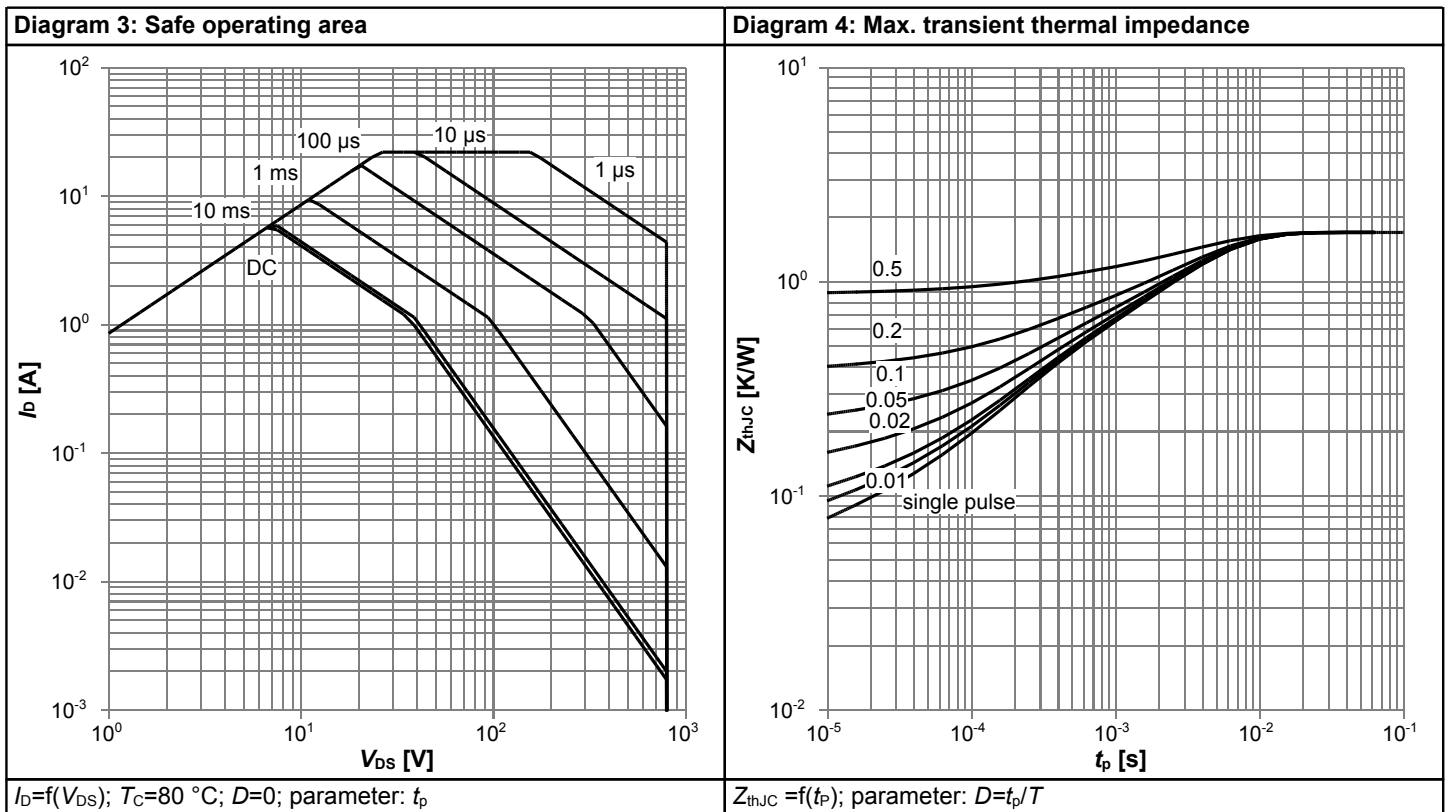
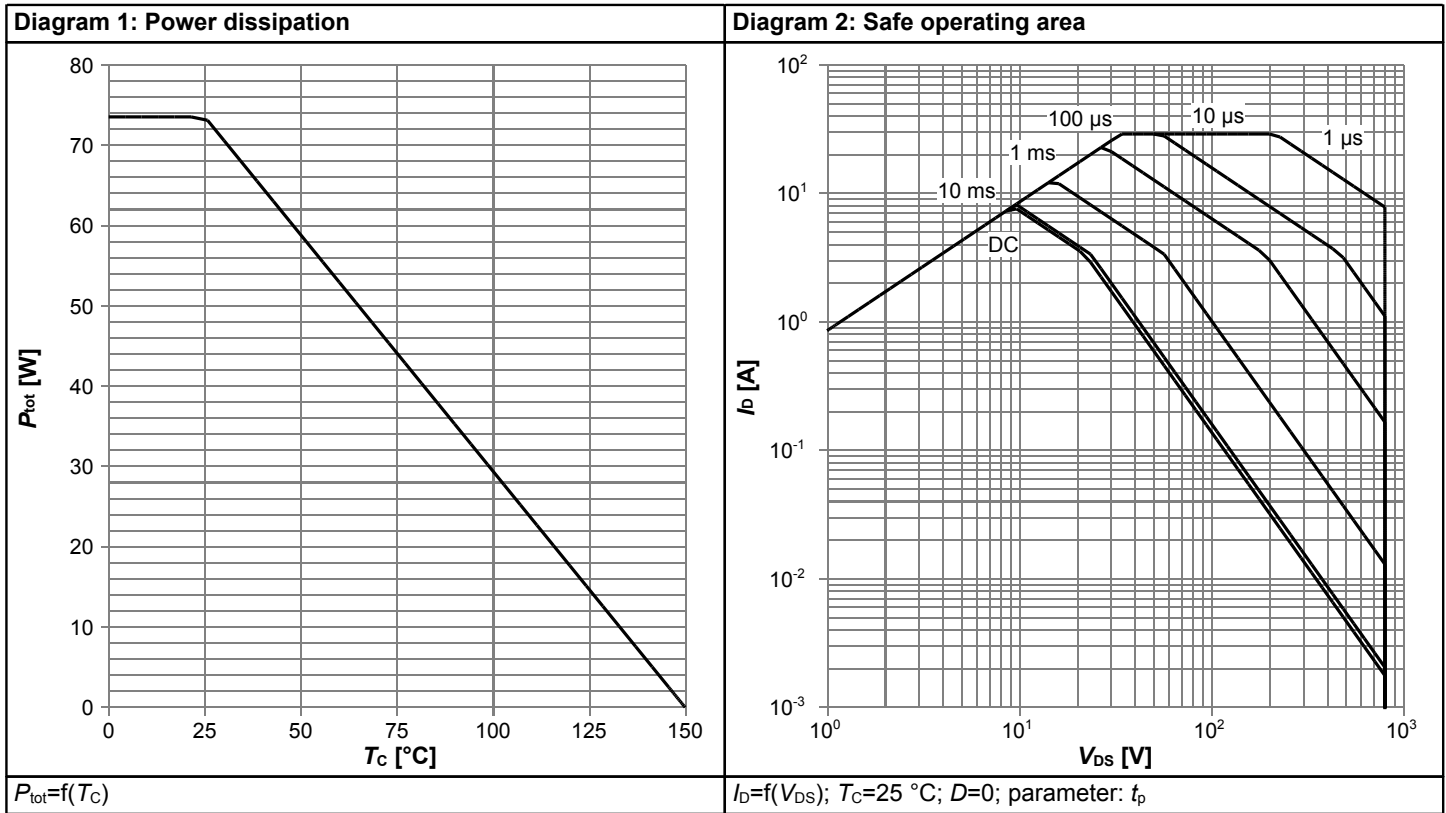
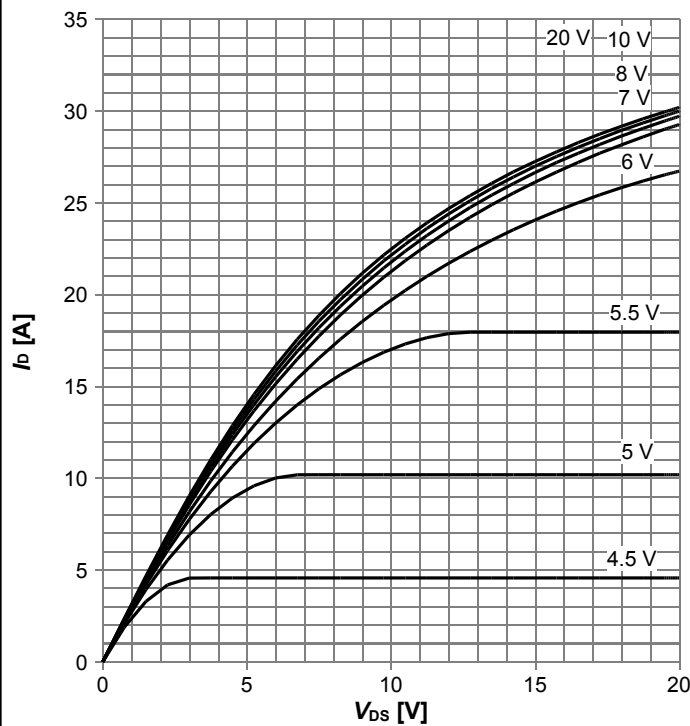
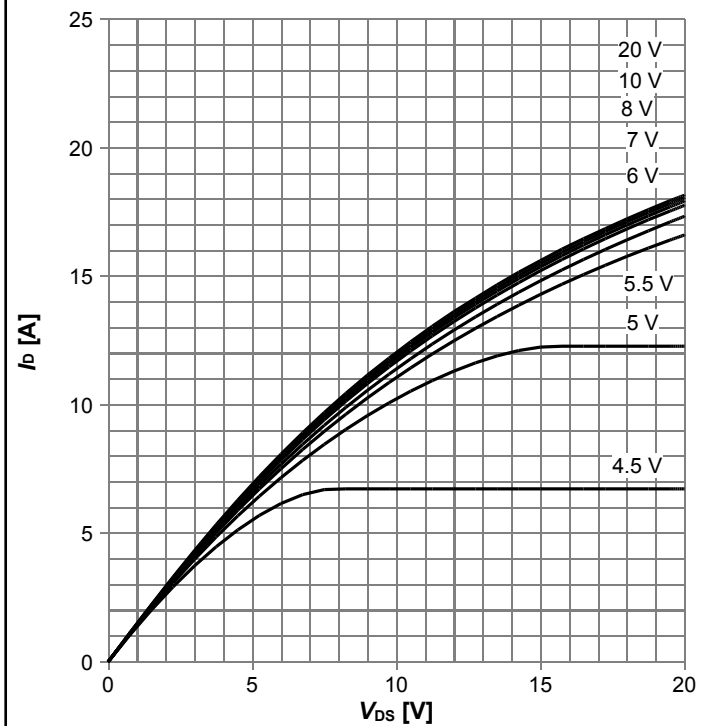


Diagram 5: Typ. output characteristics



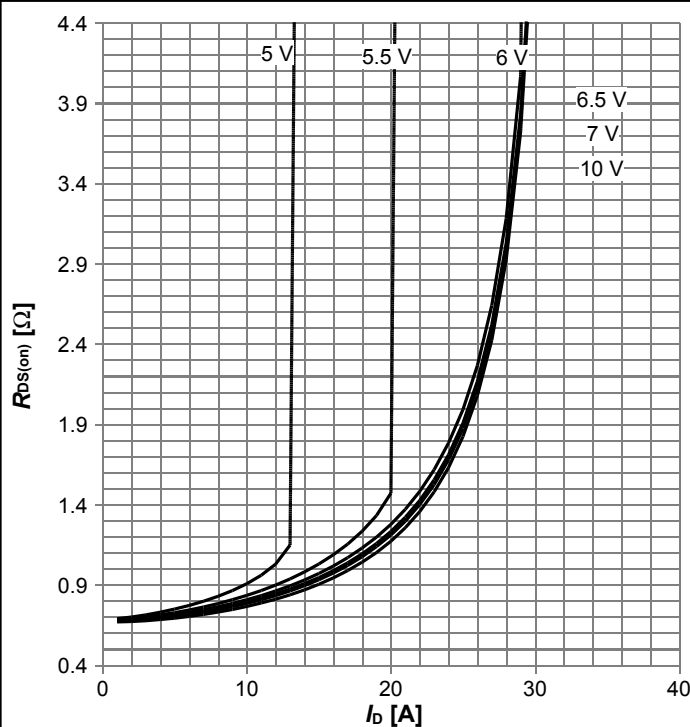
$I_D=f(V_{DS})$; $T_j=25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



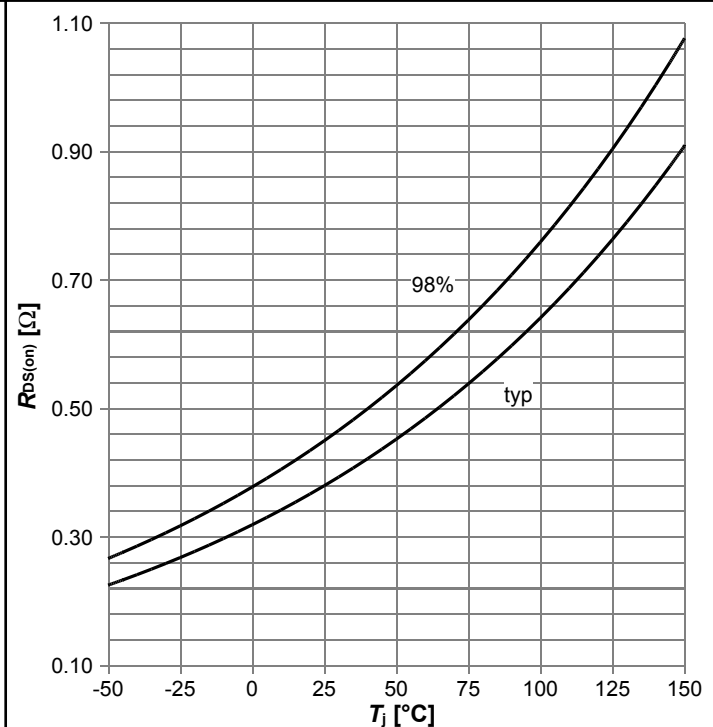
$I_D=f(V_{DS})$; $T_j=125\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



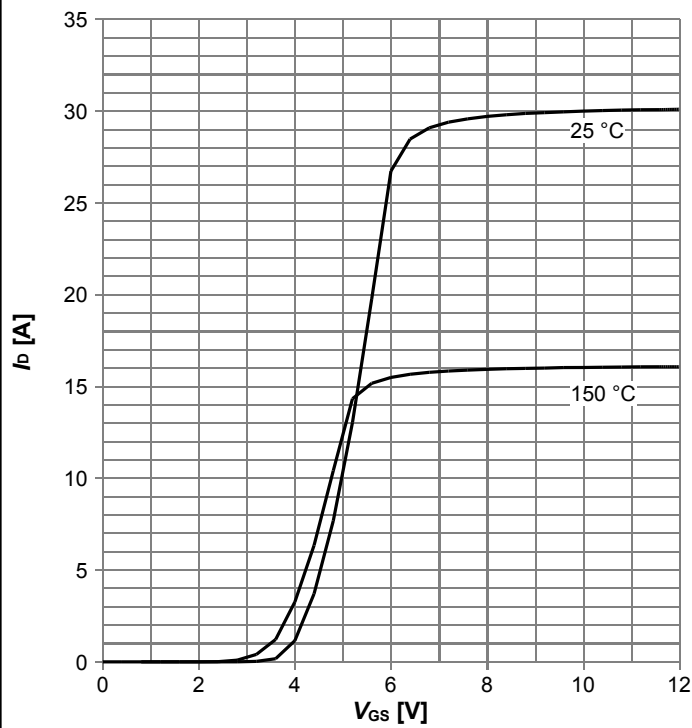
$R_{DS(on)}=f(I_D)$; $T_j=125\text{ °C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



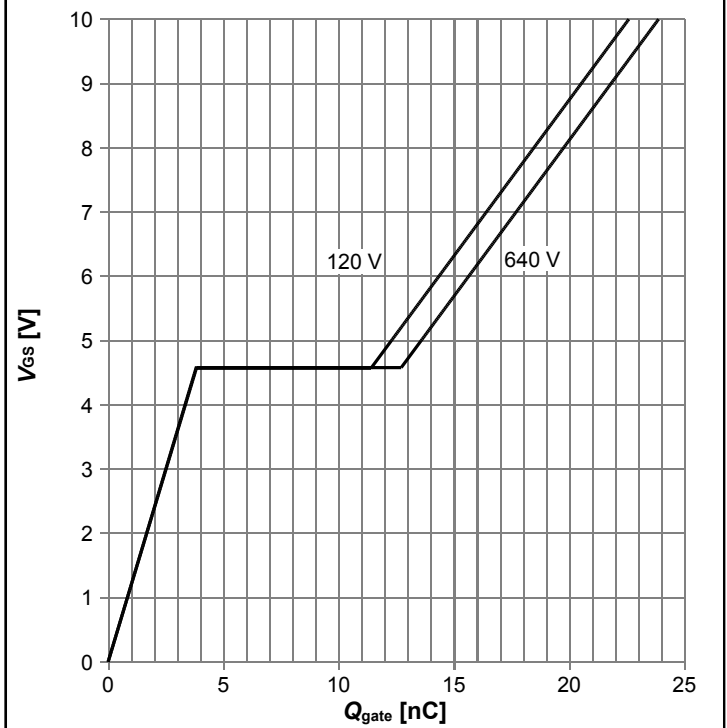
$R_{DS(on)}=f(T_j)$; $I_D=4.5\text{ A}$; $V_{GS}=10\text{ V}$

Diagram 9: Typ. transfer characteristics



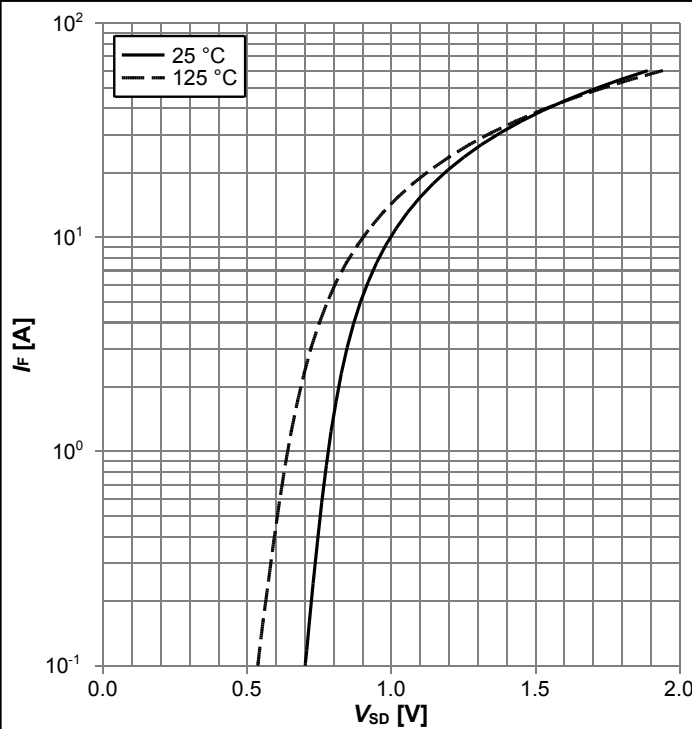
$I_D = f(V_{GS}); V_{DS} = 20V; \text{parameter: } T_j$

Diagram 10: Typ. gate charge



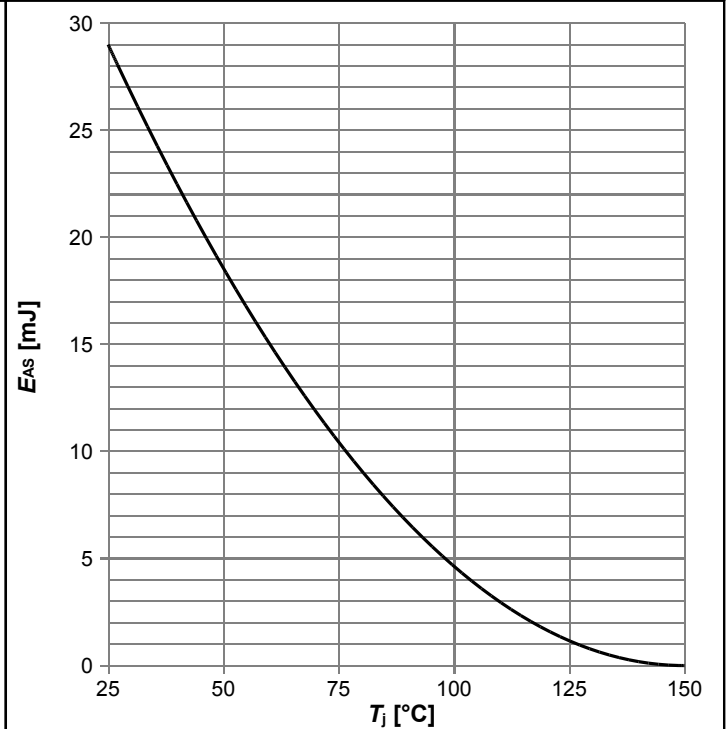
$V_{GS} = f(Q_{gate}); I_D = 4.5 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Forward characteristics of reverse diode



$I_F = f(V_{SD}); \text{parameter: } T_j$

Diagram 12: Avalanche energy



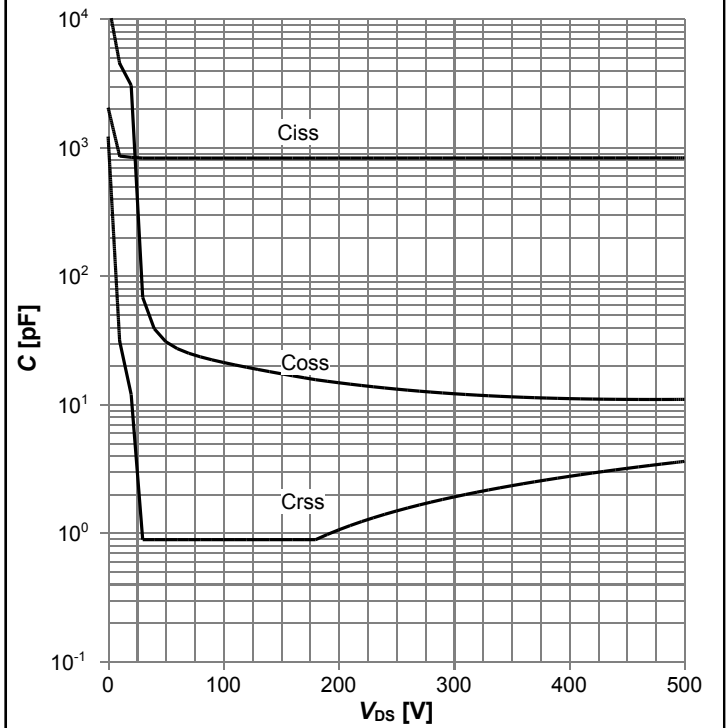
$E_{AS} = f(T_j); I_D = 1.8 \text{ A}; V_{DD} = 50 \text{ V}$

Diagram 13: Drain-source breakdown voltage



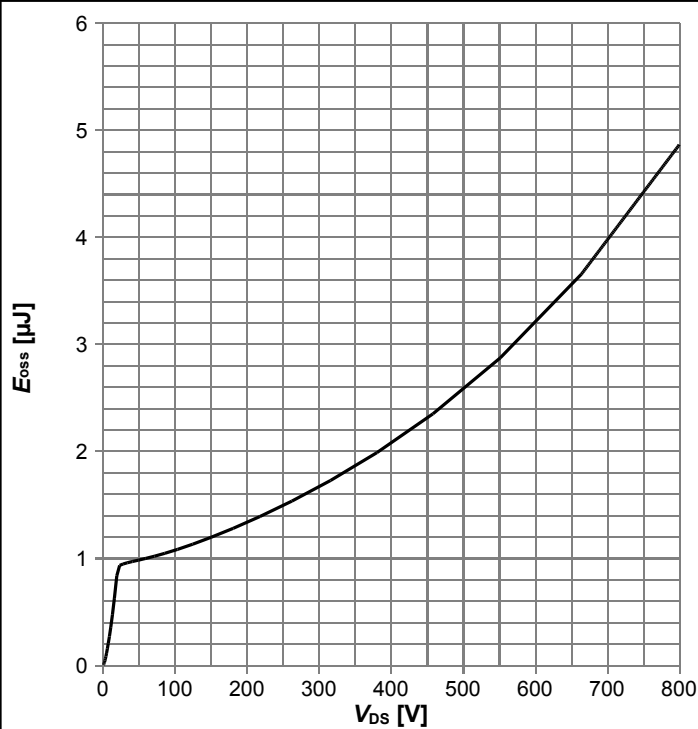
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=250 \text{ kHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

5 Test Circuits

Table 8 Diode characteristics

| Test circuit for diode characteristics | Diode recovery waveform |
|--|-------------------------|
| | |

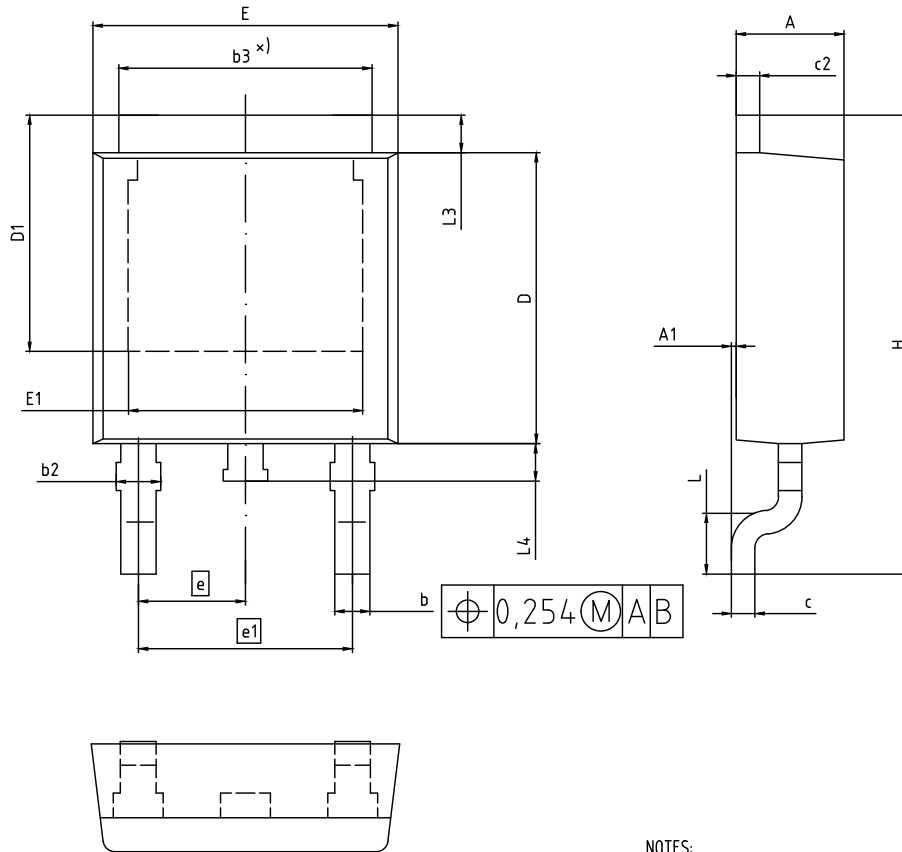
Table 9 Switching times

| Switching times test circuit for inductive load | Switching times waveform |
|---|--------------------------|
| | |

Table 10 Unclamped inductive load

| Unclamped inductive load test circuit | Unclamped inductive waveform |
|---------------------------------------|------------------------------|
| | |

6 Package Outlines



NOTES:

1. INDUSTRIAL QUALITY GRADE
2. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-252 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 2.16 | 2.41 | 0.085 | 0.095 |
| A1 | 0.00 | 0.15 | 0.000 | 0.006 |
| b | 0.64 | 0.89 | 0.025 | 0.035 |
| b2 | 0.65 | 1.15 | 0.026 | 0.045 |
| b3 | 4.95 | 5.50 | 0.195 | 0.217 |
| c | 0.46 | 0.61 | 0.018 | 0.024 |
| c2 | 0.40 | 0.98 | 0.016 | 0.039 |
| D | 5.97 | 6.22 | 0.235 | 0.245 |
| D1 | 5.02 | 5.84 | 0.198 | 0.230 |
| E | 6.35 | 6.73 | 0.250 | 0.265 |
| E1 | 4.32 | 5.21 | 0.185 | 0.205 |
| e | 2.29 (BSC) | | 0.090 (BSC) | |
| e1 | 4.57 (BSC) | | 0.180 (BSC) | |
| N | 3 | | 3 | |
| H | 9.40 | 10.48 | 0.370 | 0.413 |
| L | 1.18 | 1.78 | 0.046 | 0.070 |
| L3 | 0.89 | 1.27 | 0.035 | 0.050 |
| L4 | 0.51 | 1.02 | 0.020 | 0.040 |

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Figure 1 Outline PG-TO 252, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS Webpage:** www.infineon.com
- **IFX Design tools:** www.infineon.com

800V CoolMOS™ P7 Power Transistor

IPD80R450P7

Revision History

IPD80R450P7

Revision: 2016-07-05, Rev. 2.0

Previous Revision

| Revision | Date | Subjects (major changes since last revision) |
|----------|------------|--|
| 2.0 | 2016-07-05 | Release of final version |

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