Highly Efficient 3A Synchronous Buck Regulator

ISL85003, ISL85003A

The ISL85003 and ISL85003A are synchronous buck regulators with integrated high-side and low-side FETs. The regulator can operate from an input voltage range of 4.5V to 18V while delivering a very efficient continuous 3A current. This is all delivered in a very compact 3mmx4mm DFN package.

The ISL85003 is designed on Intersil's proprietary fab process that is designed to deliver very low $r_{DS(ON)}$ FETs with an optimized current mode controller wrapped around it. The high-side NFET is designed to have an $r_{DS(ON)}$ of 65mΩ while the low-side NFET is designed to have an $r_{DS(ON)}$ of 45mΩ. With these two FETs, the device delivers very high efficiency power to the load.

The ISL85003 can automatically switch between DCM and CCM for light-load efficiency in DCM. The switching frequency in CCM is internally set to 500kHz.

The device provides a maximum static regulation tolerance of ±1% over wide line, load and temperature ranges. The output is user adjustable, with external resistors, down to 0.8V. Pulling EN above 0.6V enables the controller. The regulator supports prebiased output.

Fault protection is provided by internal current limiting during positive or negative overcurrent conditions, output and input under and overvoltage detection and an over-temperature monitoring circuit.

Related Literature

- AN1935, "ISL85003DEMO1Z, ISL85003ADEMO1Z Evaluation Board User Guide"
- AN1930, "ISL85003EVAL2Z, ISL85003AEVAL2Z Evaluation Board User Guide"
- AN1965, "Effectively Using the Intersil Small Form Factor Power Management Evaluation Boards"

Features

- Input voltage range 4.5V to 18V
- Output voltage adjustable from 0.8V, ±1%
- Efficiency up to 95%
- Integrated boot diode with undervoltage detection
- Current mode control
  - DCM/CCM
  - Internal or external compensation options
  - 500kHz switching frequency option
  - External synchronization up to 2MHz on ISL85003
- Adjustable soft-start time on the ISL85003A
- Open-drain PG window comparator
  - Built-in protection
  - Positive and negative overcurrent protection
  - Overvoltage and thermal protection
  - Input overvoltage protection
- Small 12 Ld 3mmx4mm Dual Flat No-Lead (DFN) package

Applications

- Network and communication equipment
- Industrial process control
- Multifunction printers
- Point-of-load regulators
- Standard 12V rail supplies
- Embedded computing

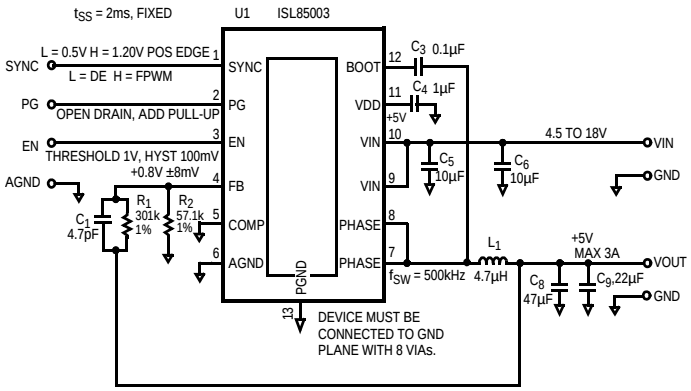


FIGURE 1A. ISL85003 V_{IN} RANGE FROM 4.5V TO 18V, V_{OUT} = 5V AND INTERNAL COMPENSATION WITH EXTERNAL FREQUENCY SYNC

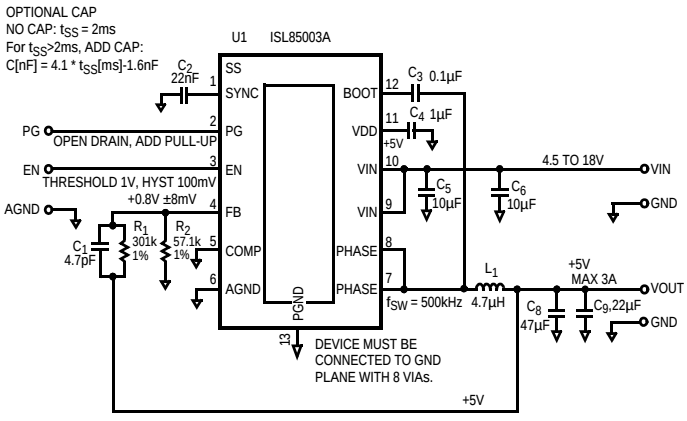


FIGURE 1B. ISL85003A V_{IN} RANGE FROM 4.5V TO 18V, V_{OUT} = 5V AND INTERNAL COMPENSATION WITH EXTERNAL SOFT-START

FIGURE 1. TYPICAL APPLICATION SCHEMATICS

Table of Contents

Functional Block Diagram

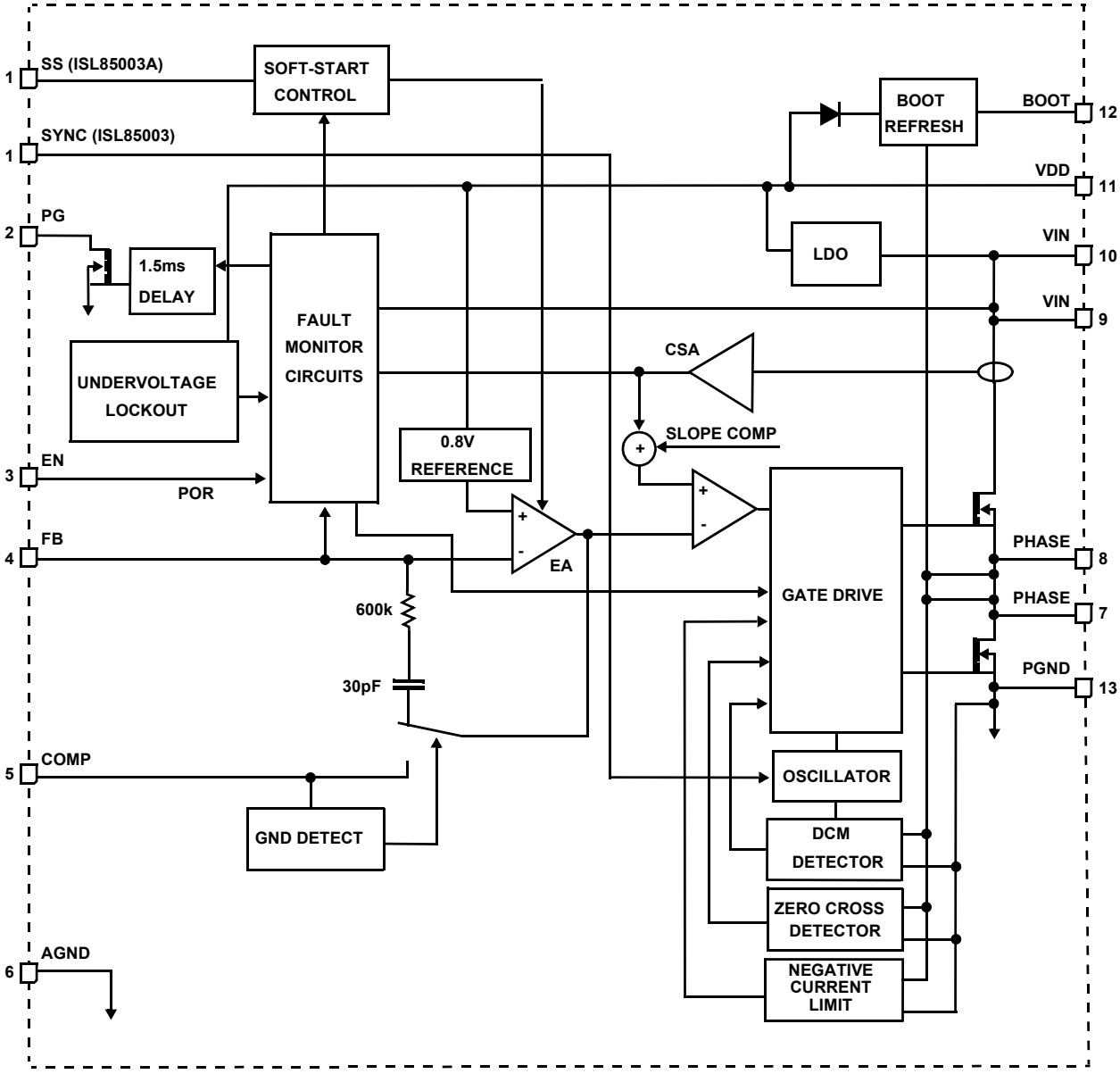
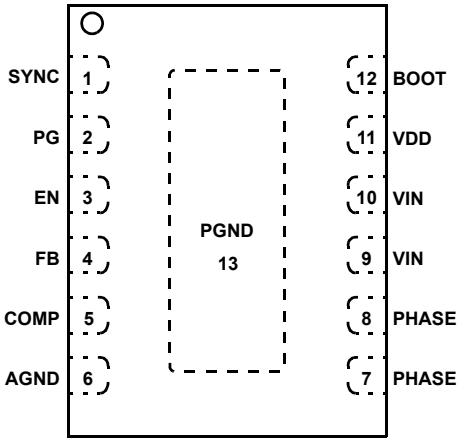


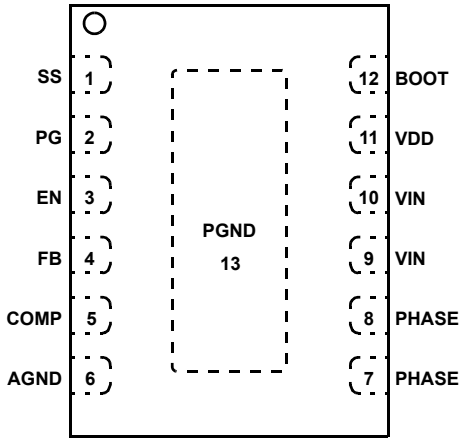
FIGURE 2. FUNCTIONAL BLOCK DIAGRAM

Pin Configurations

ISL85003
(12 ld 3X4 DFN)
TOP VIEW



ISL85003A
(12 LD 3X4 DFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1 (ISL85003)	SYNC	Synchronization and mode selection input. Connect to VDD for CCM mode. Connect to AGND for DCM mode. Connect to an external function generator for synchronization with the positive edge trigger. There is an internal 1MΩ pull-up resistor to VDD, which prevents an undefined logic state in cases where SYNC is floating.
1 (ISL85003A)	SS	Soft-Start input. This pin provides a programmable soft-start. When the chip is enabled, the regulated 4µA pull-up current source charges a capacitor connected from SS to ground. The output voltage of the converter follows the ramping voltage on this pin. Without the external capacitor, the default soft-start is 2ms.
2	PG	Power-good open-drain output. Connect 10kΩ to 100kΩ pull-up resistor between PG and VDD or between PG and a voltage not exceeding 5.5V. PG transitions high about 1ms after the switching regulator's output voltage reaches the regulation threshold, which is 85% of the regulated output voltage typically.
3	EN	Enable input. The regulator is held off when the pin is pulled to ground. The device is enabled when the voltage on this pin rises above 0.6V.
4	FB	Feedback input. The synchronous buck regulator employs a current mode control loop. FB is the negative input to the voltage loop error amplifier. The output voltage is set by an external resistor divider connected to FB. The output voltage can be set to any voltage between the power rail (reduced by converter losses) and the 0.8V reference.
5	COMP	Compensation node. This pin is connected to the output of the error amplifier, and is used to compensate the loop. Internal compensation is used to meet most applications. Connect COMP to AGND to select internal compensation. Connect a compensation network between COMP and FB to use external compensation.
6	AGND	The AGND terminal provides the return path for the core analog control circuitry within the device. Connect AGND to the board ground plane. AGND and PGND are connected internally within the device. Do not operate the device with AGND and PGND connected to dissimilar voltages.
7, 8	PHASE	Phase switch output node. This is the main output of the device. Connect to the external output inductor.
9, 10	VIN	Voltage supply input. The main power input for the IC. Connect to a suitable voltage supply. Place a ceramic capacitor from VIN to PGND, close to the IC for decoupling (typical 10µF).
11	VDD	Low dropout linear regulator decoupling pin. VDD is the internally generated 5V supply voltage and is derived from VIN. The VDD is used to power all the internal core analog control blocks and drivers. Connect a 1µF capacitor from VDD to the board ground plane. If VIN is between 4.5V to 5.5V, then connect VDD directly to VIN to improve efficiency.
12	BOOT	Bootstrap input. Floating bootstrap supply pin for the upper power MOSFET gate driver. Connect a 0.1µF capacitor between BOOT and PHASE.
13 (EPAD)	PGND	Power ground terminal. Provides thermal relief for the package and is connected to the source of the low-side output MOSFET. Connect PGND to the board ground plane using as many vias as possible. AGND and PGND are connected internally within the device. Do not operate the device with AGND and PGND connected to dissimilar voltages.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	OPTION	FREQUENCY (kHz)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL85003FRZ	003F	-40 to +125	SYNC	500	12 Ld DFN	L12.3x4
ISL85003AFRZ	003A	-40 to +125	Soft-Start	500	12 Ld DFN	L12.3x4
ISL85003EVAL2Z	Evaluation Board					
ISL85003AEVAL2Z	Evaluation Board					
ISL85003DEMO1Z	Demo Evaluation Board					
ISL85003ADEMO1Z	Demo Evaluation Board					

NOTES:

1. Add “-T” suffix for 6k unit, “-TK” suffix for 1k unit or “-T7A” suffix for 250 unit Tape and Reel options. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for ISL85003, ISL85003A. For more information on MSL, please see tech brief TB363.
4. The ISL85003 is provided with a frequency synchronization input. The ISL85003A is a version of the part with programmable soft-start.

TABLE 1. COMPONENTS SELECTION (Refer to Figures 1A and 1B)

V_{OUT}	0.8V	1V	1.2V	1.5V	1.8V	2.5V	3.3V	5V
C_5, C_6	10µF	10µF	10µF	10µF	10µF	10µF	10µF	10µF
C_8	22µF	22µF	22µF	47µF	47µF	47µF	47µF	47µF
C_9	22µF	22µF	22µF	22µF	22µF	22µF	22µF	22µF
C_1	Open	Open	Open	4.7pF	4.7pF	4.7pF	4.7pF	4.7pF
L_1	1.8µH	2.2µH	2.2µH	3.3µH	3.3µH	3.3µH	4.7µH	4.7µH
R_1	301kΩ	301kΩ	301kΩ	301kΩ	301kΩ	301kΩ	301kΩ	301kΩ
R_2	Open	1.2MΩ	604kΩ	344kΩ	241kΩ	142kΩ	96.3kΩ	57.1kΩ

NOTE: V_{IN} = 12V, I_{OUT} = 3A; The components selection table is a suggestion for typical application using internal compensation mode. For application that required high output capacitance greater than 200µF, R_1 should be adjusted to maintain loop response bandwidth about 40kHz. See “Loop Compensation Design” on page 19 for more detail.

TABLE 2. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	INTERNAL/EXTERNAL COMPENSATION	EXTERNAL FREQUENCY SYNC	PROGRAMMABLE SOFT-START	SWITCHING FREQUENCY
ISL85003	Yes	Yes	No	300kHz to 2MHz
ISL85003A	Yes	No	Yes	500kHz

Absolute Maximum Ratings

VIN, EN to AGND and PGND . . . . . -0.3V to +24V
PHASE to AGND and PGND . . . . . -0.7V to +24V (DC)
PHASE to AGND and PGND . . . . . -2V to +24V (40ns)
FB to AGND and PGND . . . . . -0.3V to +7V
BOOT to PHASE . . . . . -0.3V to +7V
VDD, COMP, SYNC, PG to AGND and PGND . . . . . -0.3V to +7V
Junction Temperature Range at 0A . . . . . -55°C to +150°C
ESD Rating
- Human Body Model (Tested per JESD22-A114E) 2.5kV
- Machine Model (Tested per JESD22-A115-A) 150V
- Charged Device Model (Tested per JESD22-A115-A) 1kV

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
DFN Package (Notes 5, 6)	49	5

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Junction Temperature Range . . . . . -40°C to +125°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

V_{IN} Supply Voltage Range . . . . . 4.5V to 18V
Load Current Range . . . . . 0A to 3A

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
6. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

All parameter limits are established over the Recommended Operating Conditions with T_J = -40°C to +125°C, and with V_{IN} = 12V unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating junction temperature range, -40°C to +125°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
SUPPLY VOLTAGE						
V_{IN} Voltage Range	V_{IN}		**4.5**		**18**	V
V_{IN} Quiescent Supply Current	I_Q	SYNC = Low, EN > 1V, FB = 0.85V, not switching		3.2	**4.5**	mA
V_{IN} Shutdown Supply Current	I_{SD}	EN = AGND		6	**11**	µA
UNDERVOLTAGE LOCKOUT						
V_{IN} UVLO Threshold		Rising Edge		4.20	**4.35**	V
		Falling Edge	**3.6**	3.8		V
INTERNAL VDD LDO						
V_{DD} Output Voltage		V_{IN} = 6V to 18V, I_{VDD} = 0mA to 30mA	**4.3**	5.00	**5.50**	V
V_{DD} Output Current Limit				50		mA
OSCILLATOR						
Nominal Switching Frequency	f_{SW}		**400**	500	**600**	kHz
Minimum On-Time	t_{ON}	I_{OUT} = 0mA (Note 8)		120	**140**	ns
Minimum Off-Time	t_{OFF}	(Note 8)		140	**180**	ns
Synchronization Range	SYNC	ISL85003	**300**		**2000**	kHz
SYNC High-Time	t_{HI}	ISL85003	**100**			ns
SYNC Low-Time	t_{LO}	ISL85003	**100**			ns
SYNC Logic Input Low		ISL85003			**0.50**	V
SYNC Logic Input High		ISL85003	**1.20**			V
ERROR AMPLIFIER						
FB Regulation Voltage	V_{FB}	V_{IN} = 4.5V to 18V	**0.792**	0.8	**0.808**	V
FB Leakage Current		V_{FB} = 0.8V (Note 8)		0.3	**10**	nA
Open Loop Bandwidth	BW			5.5		MHz
Gain				70		dB

Electrical Specifications All parameter limits are established over the Recommended Operating Conditions with T_J = -40°C to +125°C, and with V_{IN} = 12V unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating junction temperature range, -40°C to +125°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
Output Drive		V_{COMP} = 1.5V		±110		µA
Current Sense Gain	RT			0.2		Ω
Slope Compensation	Se	f_{SW} = 500kHz		550		mV/µs
ENABLE INPUT						
EN Input Threshold		Rising Edge	**0.5**	0.6	**0.7**	V
		Hysteresis	**60**	100	**140**	mV
SOFT-START FUNCTION						
Default Soft-Start Time		ISL85003, ISL85003A with soft-start open	**1**	2.3	**3.6**	ms
SS Internal Soft-Start Charging Current		ISL85003A	**2.5**	3.5	**4.5**	µA
POWER GOOD OPEN DRAIN OUTPUT						
Output Low Voltage		I_{PG} = 5mA sinking		0.25		V
PG Pin Leakage Current		V_{PG} = V_{DD}		0.01		µA
PG Lower Threshold		Percentage of output regulation	**80**	85	**90**	%
PG Upper Threshold		Percentage of output regulation	**110**	115	**120**	%
PG Thresholds Hysteresis				3		%
Delay Time		Rising Edge		1.5		ms
		Falling Edge		18		µs
FAULT PROTECTION						
Positive Overcurrent Protection Threshold	I_{POCP}		**4.0**	5.0	**6.0**	A
Negative Overcurrent Protection Threshold	I_{NOCP}	Current forced into PHASE node, high-side MOSFET is off, SYNC = High	**-3.2**	-2.2	**-1.1**	A
Positive Overcurrent Protection Low-Side MOSFET		Current in low-side MOSFET at end of low-side cycle.		6		A
V_{IN} Overvoltage Threshold			**19**	20		V
		Hysteresis		1		V
Thermal Shutdown Temperature	T_{SD}	Rising Threshold		165		°C
	T_{HYS}	Hysteresis		10		°C
POWER MOSFET						
High-Side MOSFET $r_{DS(ON)}$	R_{HDS}	I_{PHASE} = 100mA		65	**110**	mΩ
Low-Side MOSFET $r_{DS(ON)}$	R_{LDS}	I_{PHASE} = 100mA		45	**75**	mΩ
PHASE Pull-Down Resistor		EN = AGND		10		KΩ
DIODE EMULATION						
Zero Crossing Threshold		ISL85003		150		mA

NOTES:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
8. Compliance to limits is assured by characterization and design.

Typical Performance Curves

Circuit of V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, T_J = -40°C to +125°C unless otherwise noted. Typical values are at T_A = +25°C.

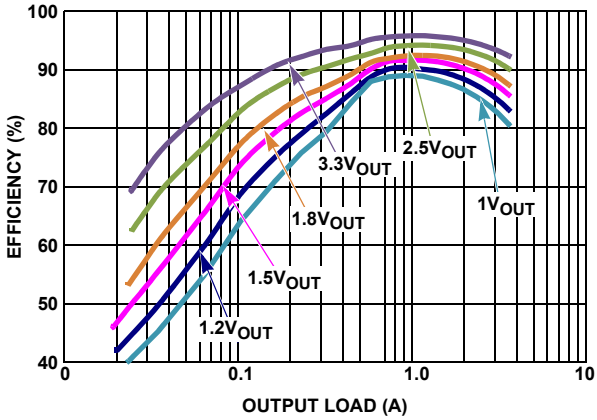


FIGURE 3. EFFICIENCY vs LOAD, $5V_{IN}$ DCM

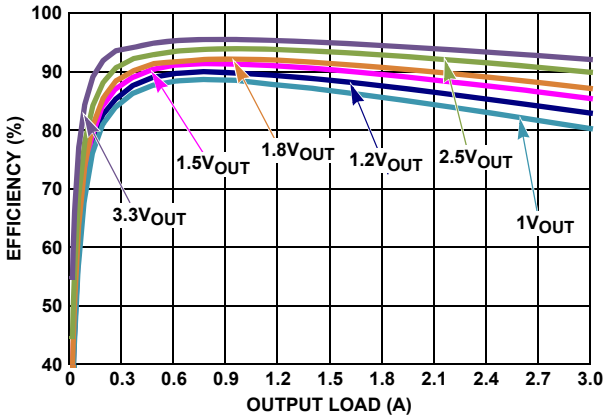


FIGURE 4. EFFICIENCY vs LOAD, $5V_{IN}$ CCM

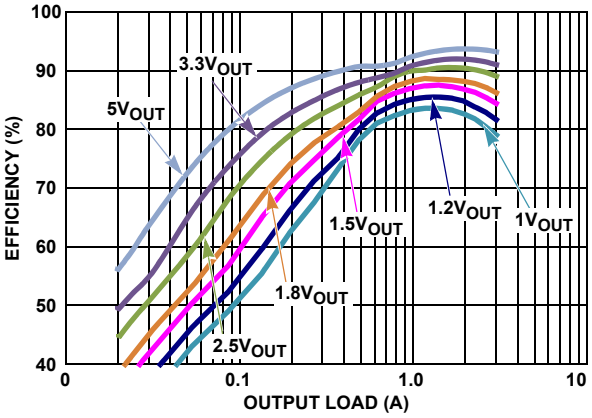


FIGURE 5. EFFICIENCY vs LOAD, $12V_{IN}$ DCM

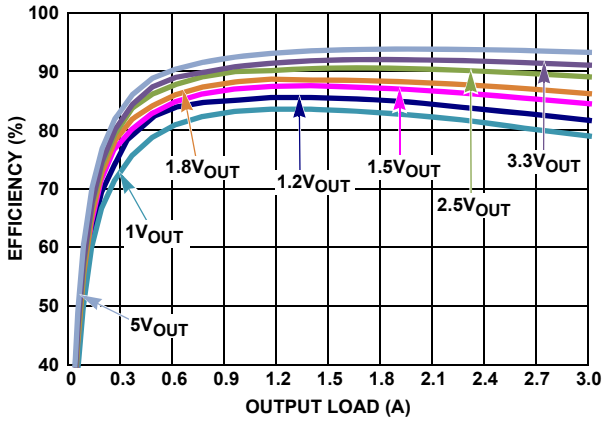


FIGURE 6. EFFICIENCY vs LOAD, $12V_{IN}$ CCM

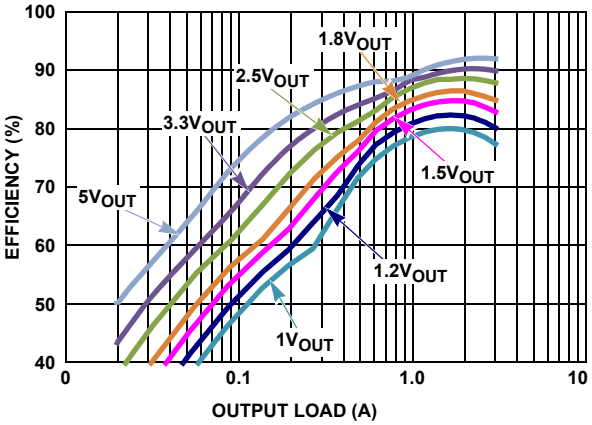


FIGURE 7. EFFICIENCY vs LOAD, $18V_{IN}$ DCM

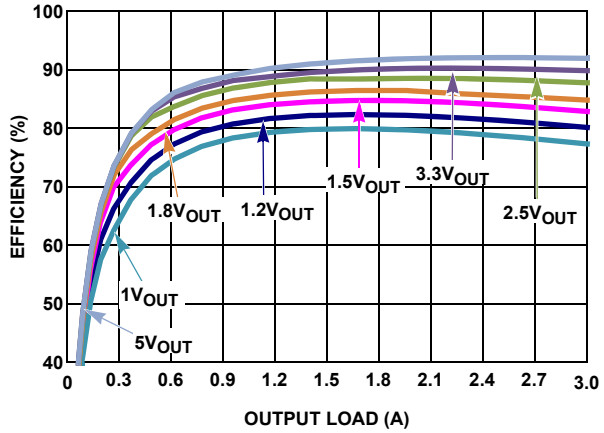


FIGURE 8. EFFICIENCY vs LOAD, $18V_{IN}$ CCM

Typical Performance Curves

Circuit of V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, T_J = -40°C to +125°C unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

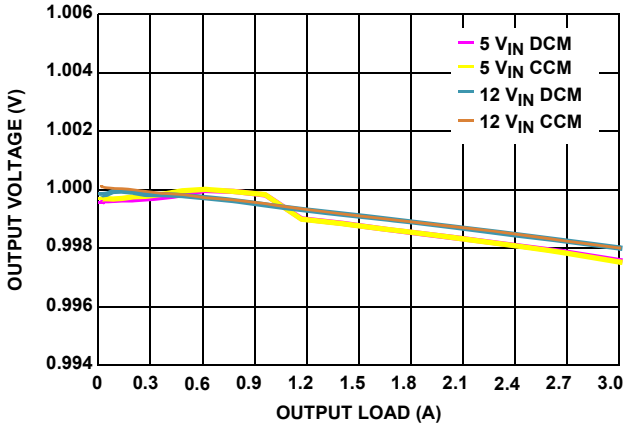


FIGURE 9. V_{OUT} REGULATION vs LOAD, 1V

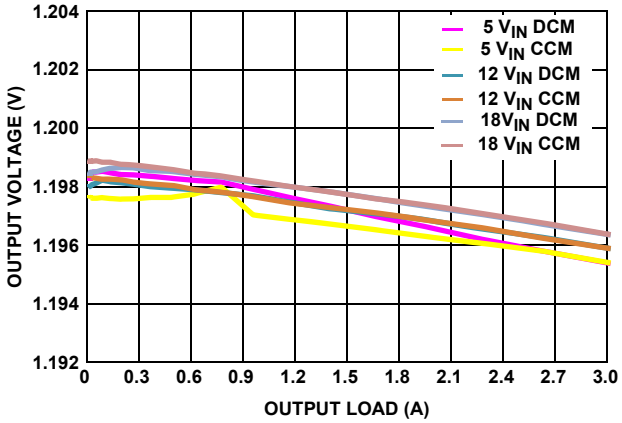


FIGURE 10. V_{OUT} REGULATION vs LOAD, 1.2V

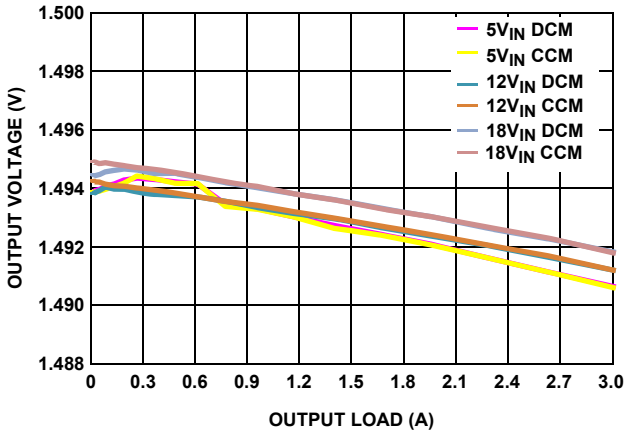


FIGURE 11. V_{OUT} REGULATION vs LOAD, 1.5V

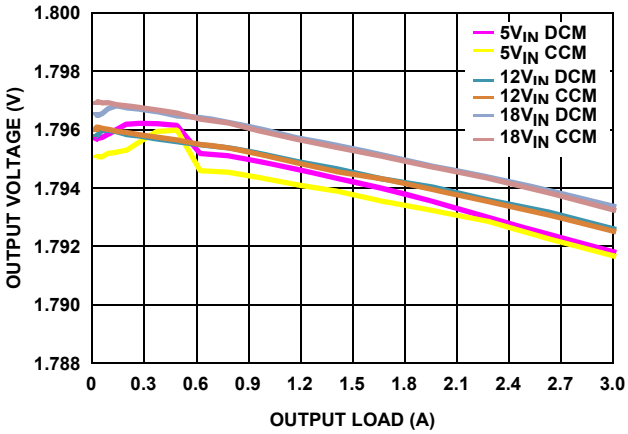


FIGURE 12. V_{OUT} REGULATION vs LOAD, 1.8V

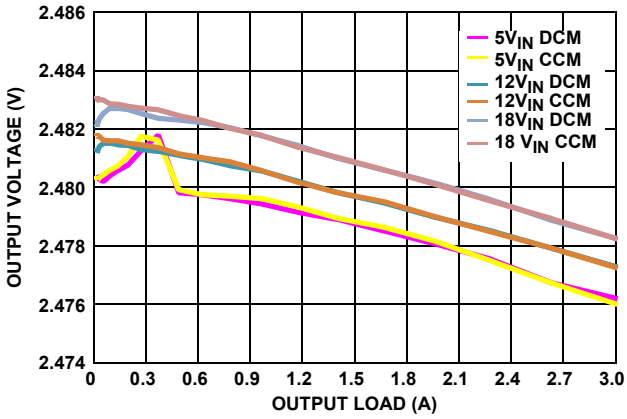


FIGURE 13. V_{OUT} REGULATION vs LOAD, 2.5V

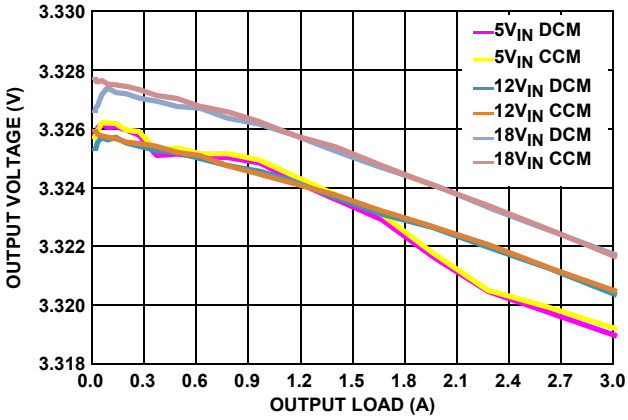


FIGURE 14. V_{OUT} REGULATION vs LOAD, 3.3V

Typical Performance Curves

Circuit of V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, T_J = -40°C to +125°C unless otherwise noted.
Typical values are at T_A = +25°C. **(Continued)**

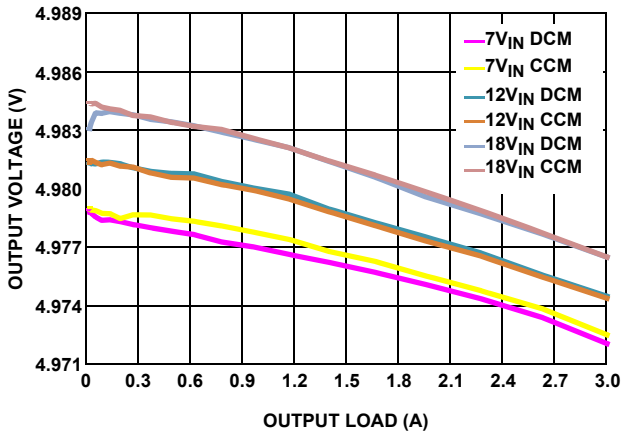


FIGURE 15. V_{OUT} REGULATION vs LOAD 5V

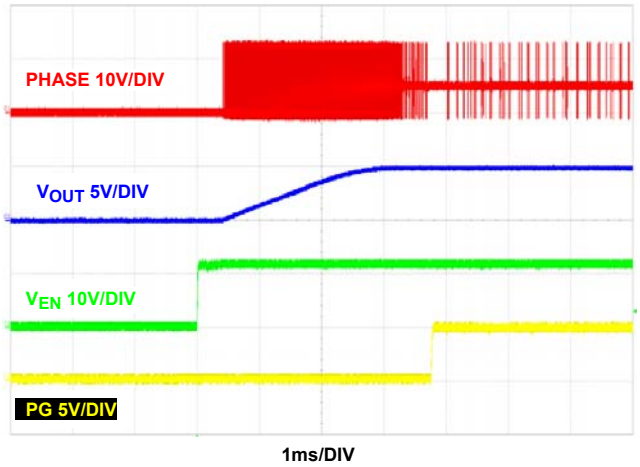


FIGURE 16. START-UP V_{EN} AT NO LOAD (DCM)

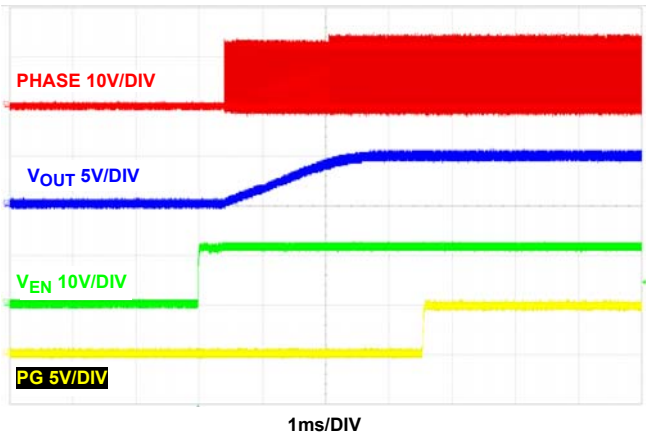


FIGURE 17. START-UP V_{EN} AT NO LOAD (CCM)

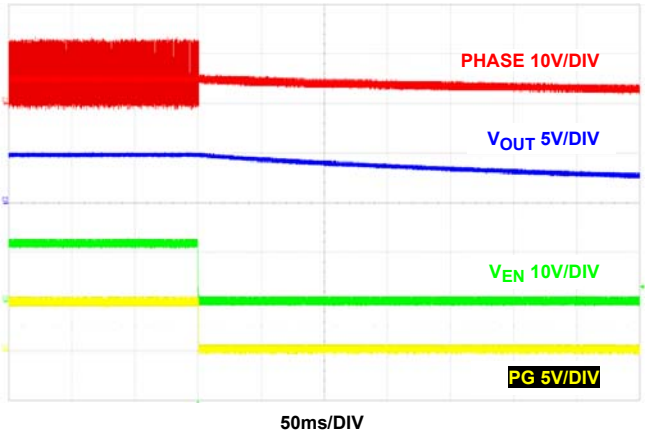


FIGURE 18. SHUTDOWN V_{EN} AT NO LOAD (DCM)

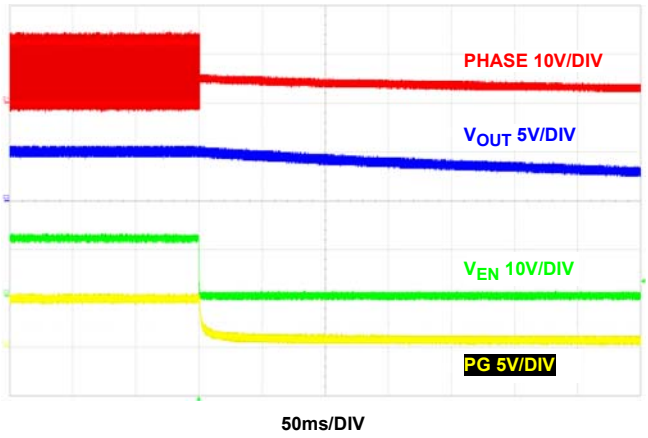


FIGURE 19. SHUTDOWN V_{EN} AT NO LOAD (CCM)

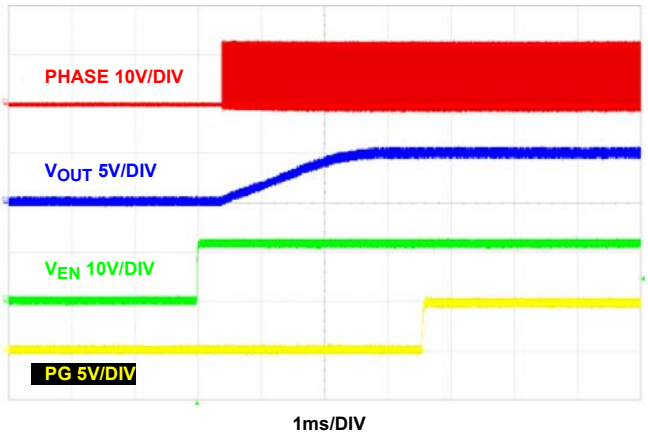


FIGURE 20. START-UP V_{EN} AT 3A LOAD

Typical Performance Curves

Circuit of V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, T_J = -40°C to +125°C unless otherwise noted.
Typical values are at T_A = +25°C. **(Continued)**

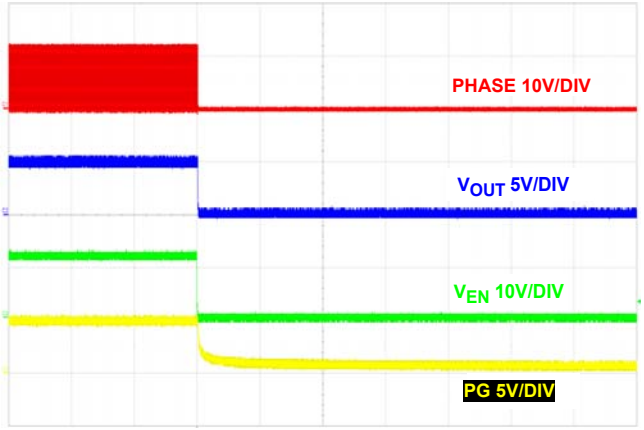


FIGURE 21. SHUTDOWN V_{EN} AT 3A LOAD

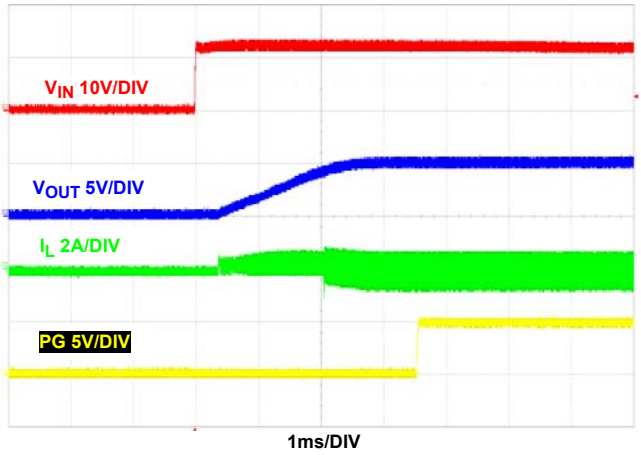


FIGURE 22. START-UP V_{IN} AT NO LOAD (CCM)

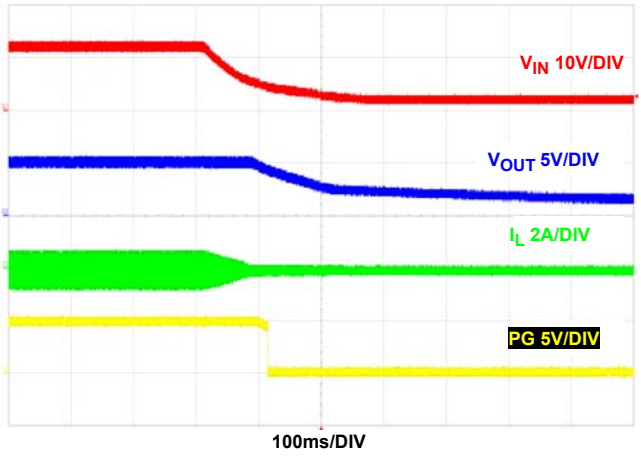


FIGURE 23. SHUTDOWN V_{IN} AT NO LOAD (CCM)

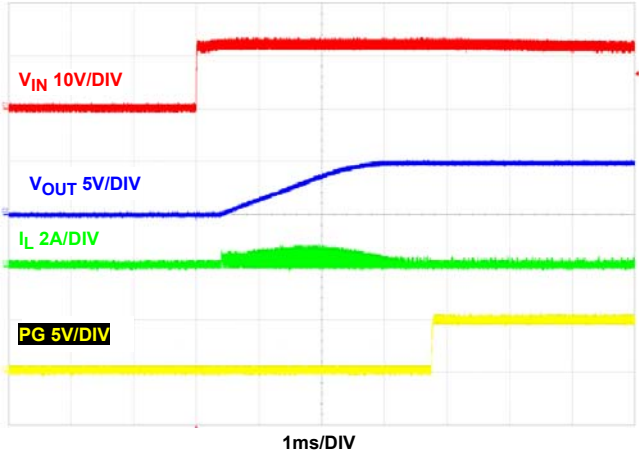


FIGURE 24. START-UP V_{IN} AT NO LOAD (DCM)

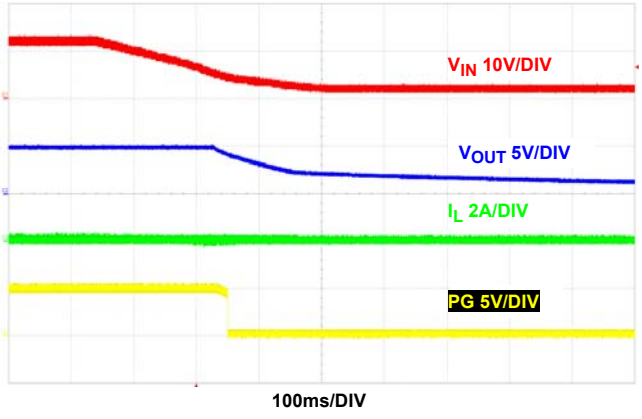


FIGURE 25. SHUTDOWN V_{IN} AT NO LOAD (DCM)

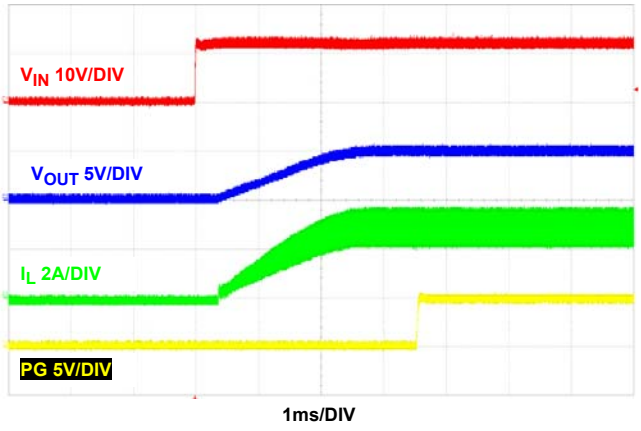


FIGURE 26. STAR-TUP V_{IN} AT 3A LOAD

Typical Performance Curves

Circuit of V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, T_J = -40°C to +125°C unless otherwise noted.
Typical values are at T_A = +25°C. **(Continued)**

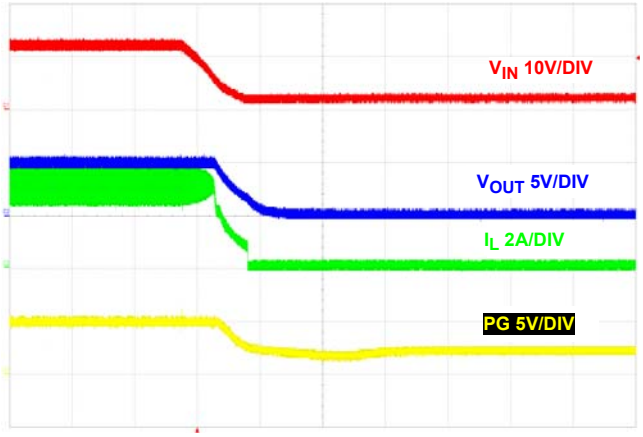


FIGURE 27. SHUTDOWN V_{IN} AT 3A LOAD

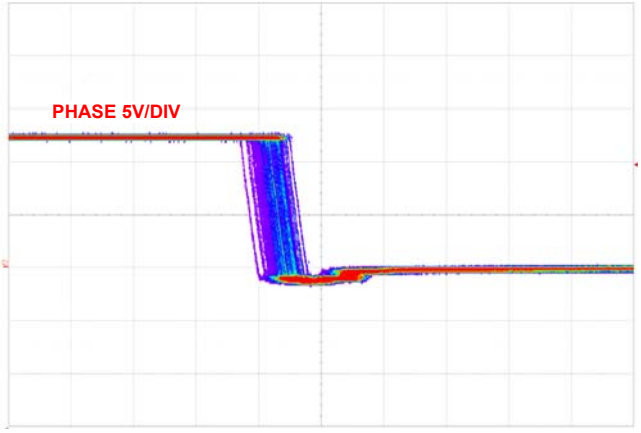


FIGURE 28. JITTER AT NO LOAD (CCM)

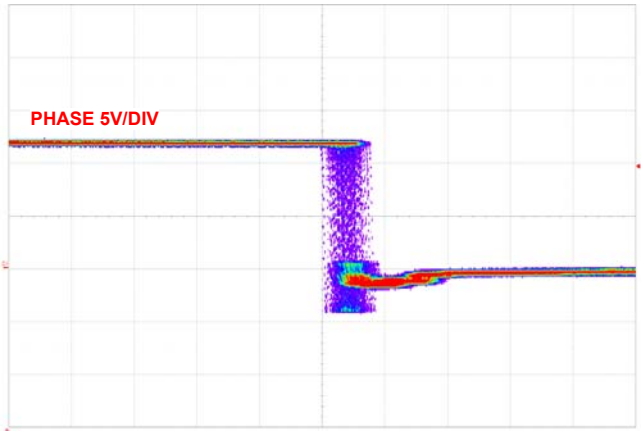


FIGURE 29. JITTER AT FULL LOAD 3A (CCM)

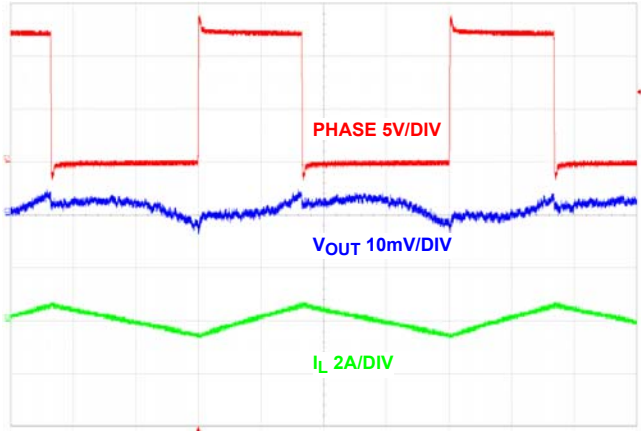


FIGURE 30. STEADY STATE AT NO LOAD CCM

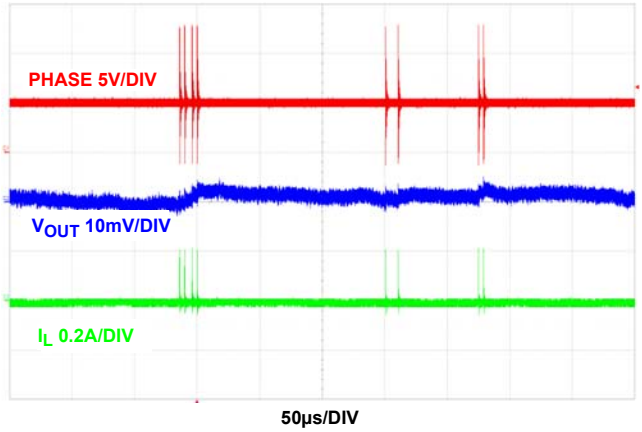


FIGURE 31. STEADY STATE AT NO LOAD DCM

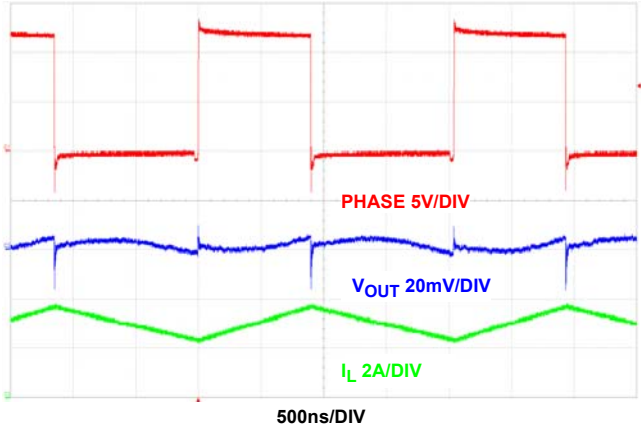


FIGURE 32. STEADY STATE AT 3A LOAD DCM

Typical Performance Curves

Circuit of V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, T_J = -40°C to +125°C unless otherwise noted.
Typical values are at T_A = +25°C. **(Continued)**

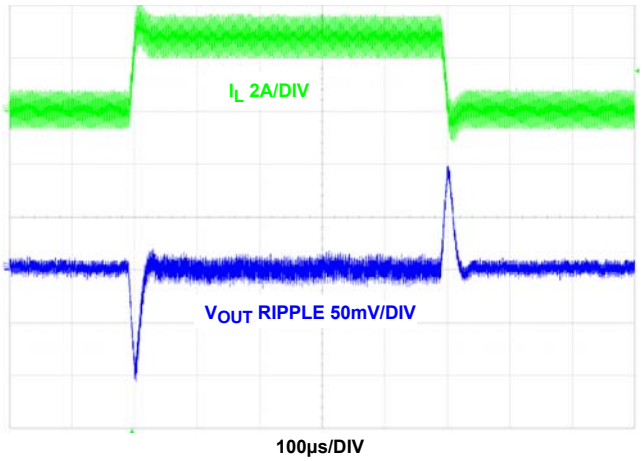


FIGURE 33. LOAD TRANSIENT (CCM)

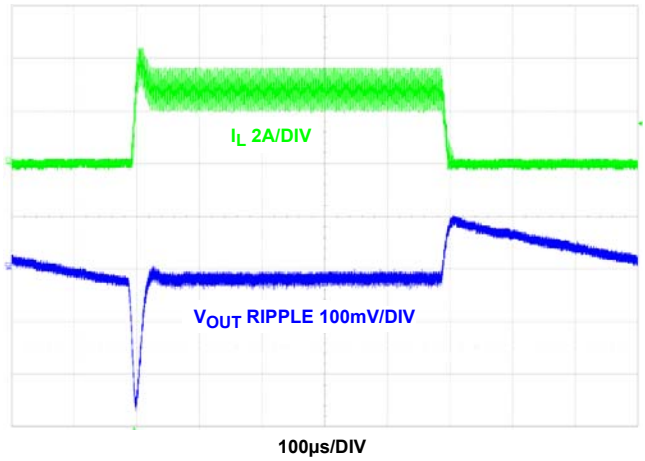


FIGURE 34. LOAD TRANSIENT (DCM)

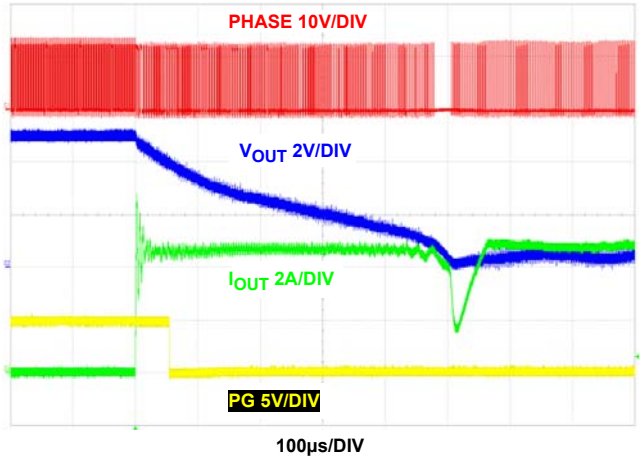


FIGURE 35. OUTPUT SHORT-CIRCUIT

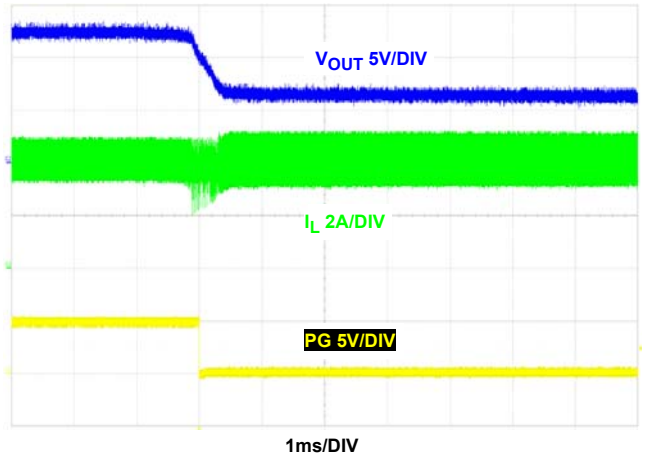


FIGURE 36. OVERCURRENT PROTECTION

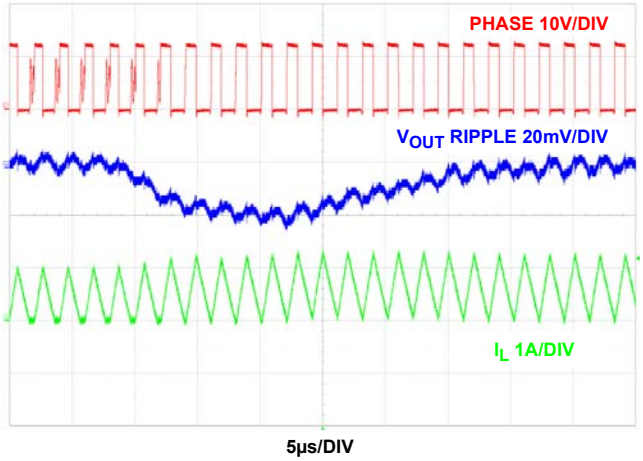


FIGURE 37. DCM TO CCM TRANSITION

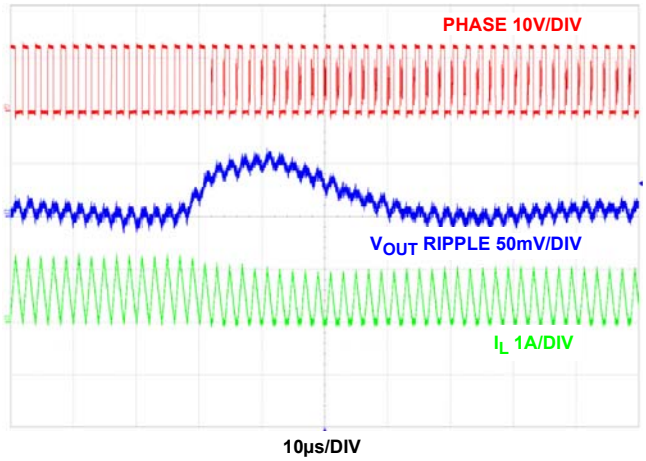


FIGURE 38. CCM TO DCM TRANSITION

Typical Performance Curves

Circuit of V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, T_J = -40°C to +125°C unless otherwise noted.

Typical values are at T_A = +25°C. **(Continued)**

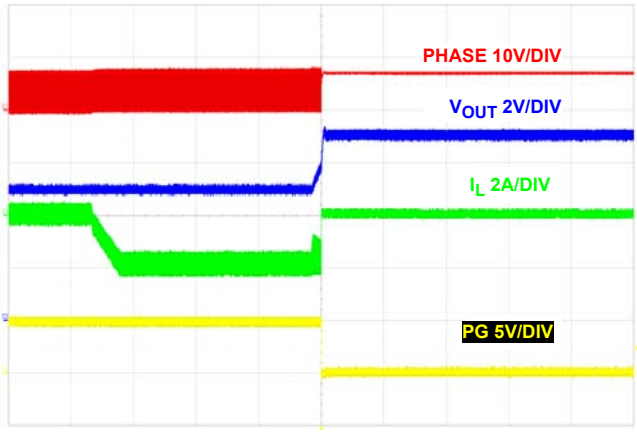


FIGURE 39. 0VERVOLTAGE PROTECTION

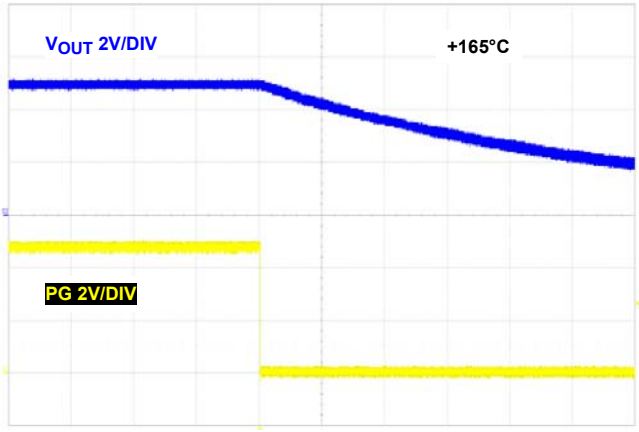


FIGURE 40. OVER-TEMPERATURE PROTECTION

Detailed Description

The ISL85003 and ISL85003A combine a synchronous buck controller with a pair of integrated switching MOSFETs. The buck controller drives the internal high-side and low-side N-channel MOSFETs to deliver load currents up to 3A. The buck regulator can operate from an unregulated DC source, such as a battery, with a voltage ranging from +4.5V to +18V. An internal 5V LDO voltage regulator is used to bias the controller. The converter output voltage is programmed using an external resistor divider and will generate regulated voltages down to 0.8V. These features make the regulator suited for a wide range of applications.

The controller uses a current mode loop, which simplifies the loop compensation and permits fixed frequency operation over a wide range of input and output voltages. The internal feedback loop compensation option allows for simple circuit design. The regulator switches at a default of 500kHz or it can be synchronized from 300kHz to 2MHz on an ISL85003.

The buck regulator is equipped with a lossless current limit scheme. The current in the output stage is derived from temperature compensated measurements of the drain-to-source voltage of the internal power MOSFETs. The current limit threshold is internally set at 5A.

Operation Initialization

Pull EN high to start operation. The power-on reset circuitry will prevent operation if the input voltage is below 4.2V. Once the power-on reset requirement is met, the controller will soft-start with a 2ms ramp on an ISL85003 or at a rate determined by the value of a capacitor connected between SS and AGND on an ISL85003A.

CCM Control Scheme

The regulator employs a current-mode pulse-width modulation control scheme for fast transient response and pulse-by-pulse current limiting. The current loop consists of the oscillator, the PWM comparator, current sensing circuit, and a slope compensation circuit. The gain of the current sensing circuit is typically 200mV/A and the slope compensation is 1.1V/T. The reference for the current loop is in turn provided by the output of an Error Amplifier (EA), which compares the feedback signal at the FB pin to the integrated 0.8V reference. Thus, the output voltage is regulated by using the error amplifier to control the reference for the current loop.

The error amplifier is an operational amplifier that converts the voltage error signal to a voltage output. The voltage loop is internally compensated with the 30pF and 600kΩ RC network that can support most applications.

PWM operation is initialized by the clock from the oscillator. The upper MOSFET is turned on at the beginning of a cycle and the current in the MOSFET starts to ramp up. When the sum of the current amplifier CSA signal and the slope compensation reaches the control reference of the current loop, the PWM comparator sends a signal to the logic to turn off the upper MOSFET and turn on the lower MOSFET. The lower MOSFET stays on until the end of the cycle. Figure 41 shows the typical operating waveforms during Continuous Conduction Mode (CCM) operation. The dotted lines illustrate the sum of the compensation ramp and the current-sense amplifier's output.

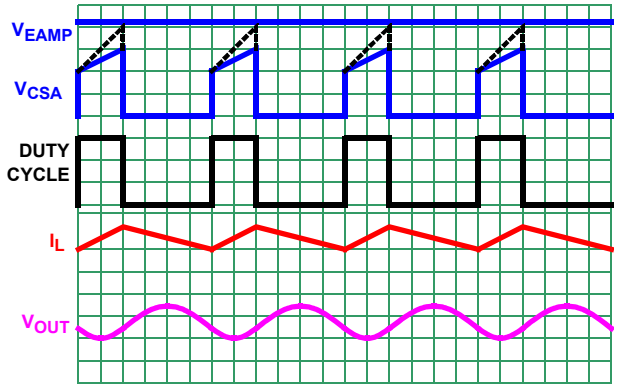


FIGURE 41. CCM OPERATION WAVEFORMS

Light-Load Operation

The ISL85003 monitors both the current in the low-side MOSFET and the voltage of the FB node for regulation. Pulling the SYNC pin low allows the ISL85003 to enter discontinuous operation when lightly loaded by operating the low-side MOSFET in Diode Emulation Mode (DEM). In this mode, reverse current is not allowed in the inductor, and the output falls naturally to the regulation voltage before the high-side MOSFET is switched for the next cycle. Figure 42 shows the transition from CCM to DCM operation. In CCM mode, the boundary is set by Equation 1:

$$I_{OUT} = \frac{V_{OUT}(1-D)}{2Lf_{SW}} \quad \text{(EQ. 1)}$$

Where D = duty cycle, f_{SW} = switching frequency, L = inductor value, I_{OUT} = output loading current, V_{OUT} = output voltage.

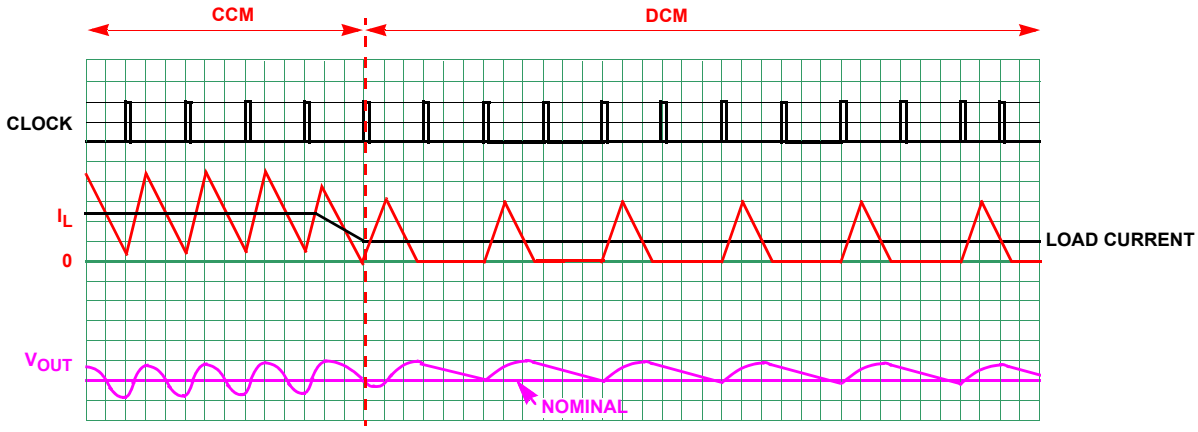


FIGURE 42. DCM MODE OPERATION WAVEFORMS

Synchronization Control

The ISL85003 can be synchronized from 300kHz to 2MHz by an external signal applied to the SYNC pin. The rising edge on the SYNC triggers the rising edge of the PHASE pulse. Make sure that the on-time of the SYNC pulse is greater than 100ns. Although the maximum synchronized frequency can be as high as 2MHz, the ISL85003 is a current mode regulator that requires a minimum of 140ns on-time to regulate properly. As an example, the maximum recommended synchronized frequency will be about 600kHz with $12V_{IN}$ and $1V_{OUT}$.

Enable, Soft-Start and Disable

Chip operation begins after V_{IN} exceeds its rising POR trip point (nominal 4.2V). If EN is held low externally, nothing happens until this pin is released. Once the voltage on the EN pin is above 0.6V, the LDO powers up and soft-start control begins. The default soft-start time is 2ms.

On the ISL85003A, let SS float to select the internal soft-start time with a default of 2ms. The soft-start time is extended by connecting an external capacitor between SS and AGND. A 3.5µA current source charges up the capacitor. The soft-start capacitor is charged until the voltage on the SS pin reaches a 2.0V clamp level. However, the output voltage reaches its regulation value when the voltage on the SS pin reaches approximately 0.9V. The capacitor, along with an internal 3.5µA current source, sets the soft-start interval of the converter, t_{SS}, according to Equation 2:

$$C_{SS}[nF] = 4.1 \cdot t_{SS}[mS] - 1.6nF \quad \text{(EQ. 2)}$$

Output Voltage Selection

The regulator output voltage is programmed using an external resistor divider that scales the feedback relative to the internal reference voltage. The scaled voltage is fed back to the inverting input of the error amplifier; refer to Figure 43.

The output voltage programming resistor, R_2, will depend on the value chosen for the feedback resistor, R_1, and the desired regulator output voltage, V_{OUT}; (see Equation 3). The R_1 value will determine the gain of the feedback loop. (See "Loop Compensation Design" on page 19) for more details. The value for the feedback resistor is typically between 10kΩ and 400kΩ.

$$R_2 = \frac{R_1 \cdot 0.8V}{V_{OUT} - 0.8V} \quad \text{(EQ. 3)}$$

If the output voltage desired is 0.8V, then R_2 is left unpopulated. R_1 is still required to set the low frequency pole of the modulator compensation.

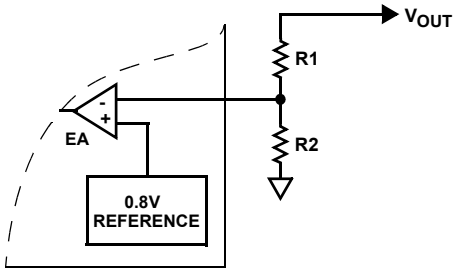


FIGURE 43. EXTERNAL RESISTOR DIVIDER

Protection Features

The regulator limits current in all on-chip power devices. Overcurrent limits are applied to the two output switching MOSFETs as well as to the LDO linear regulator that feeds VDD. Input and output overvoltage protection circuitry on the switching regulator provides a second layer of protection.

Switching Regulator Overcurrent Protection

Current flowing through the internal high-side switching MOSFET is monitored during the on-time. The current is compared to a nominal 5A overcurrent limit. If the measured current exceeds the overcurrent limit reference level, the high-side MOSFET is immediately turned off and will not turn on again until the next switching cycle. Current through the low-side switching MOSFET is sampled during off time. If the low-side MOSFET current exceeds 6A at the end of the low-side cycle, then the high-side MOSFET will skip the next cycle, allowing the inductor current to decay to a safe level before resuming switching.

Once an output overload condition is removed, the output voltage will rise into regulation at the internal SS rate.

Negative Current Protection

Similar to the overcurrent, the negative current protection is realized by monitoring the current across the low-side MOSFET, as shown in "Functional Block Diagram" on page 3. When the inductor current reaches -2.2A, the synchronous rectifier is turned off. This limits the ability of the regulator to actively pull down on the output and prevents large reverse currents that may fall outside the range of the high-side current sense amp.

Output Overvoltage Protection

The output overvoltage protection is triggered when the output voltage exceeds 115% of the set voltage. In this condition, high-side and low-side MOSFETs are tri-stated until the output drops to within the regulation band. Once the output is in regulation, the controller will restart under internal SS control.

Input Overvoltage Protection

The input overvoltage protection system prevents operation of the switching regulator whenever the input voltage is higher than 20V. The high-side and low-side MOSFETs are tri-stated and the converter will restart under internal SS control when the input voltage returns to normal.

Thermal Overload Protection

Thermal overload protection limits the maximum die temperature, thus the total power dissipation in the regulator. A sensor on the chip monitors the junction temperature. A signal is sent to the fault monitor circuits whenever the junction temperature (T_J) exceeds +165°C and this causes the switching regulator and LDO to shut down.

The switching regulator turns on again and soft-starts after the IC's junction temperature cool by 10°C. The switching regulator exhibits hiccup mode operation during continuous thermal overload conditions. For continuous operation, do not exceed the +125°C junction temperature rating.

Power Derating Characteristics

To prevent the regulator from exceeding the maximum junction temperature, some thermal analysis is required. The temperature rise is given by Equation 4:

$$T_{RISE} = (PD)(\theta_{JA}) \quad \text{(EQ. 4)}$$

Where PD is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature. The junction temperature, T_J, is given by Equation 5:

$$T_J = (T_A + T_{RISE}) \quad \text{(EQ. 5)}$$

Where T_A is the ambient temperature. For the DFN package, the θ_{JA} is 49 (°C/W).

The actual junction temperature should not exceed the absolute maximum junction temperature of +125°C when considering the thermal design.

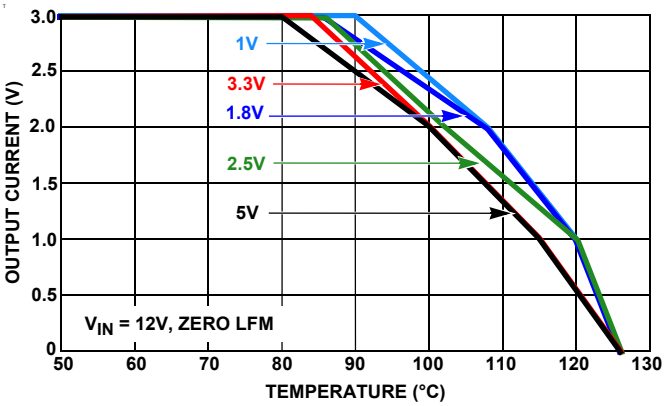


FIGURE 44. DERATING CURVE vs TEMPERATURE

Application Guidelines

BOOT Undervoltage Detection

The internal driver of the high-side FET is equipped with a BOOT Undervoltage (UV) detection circuit. In the event the voltage difference between BOOT and PHASE falls below 2.5V, the UV detection circuit allows the low-side MOSFET on for 300ns, to recharge the bootstrap capacitor.

While the ISL85003 includes an internal bootstrap diode, efficiency can be improved by using an external supply voltage and bootstrap Schottky diode. The external diode is then sourced from a fixed external 5V supply or from the output of the switching regulator if this is at 5V. The bootstrap diode can be a low cost type, such as the BAT54.

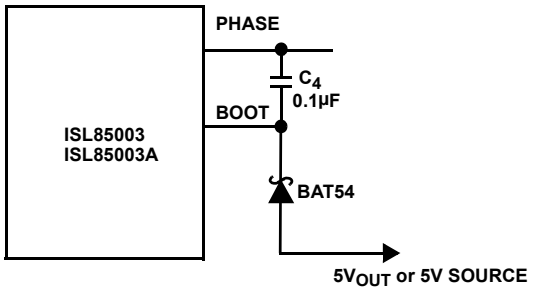


FIGURE 45. EXTERNAL BOOTSTRAP DIODE

Switching Regulator Output Capacitor Selection

An output capacitor is required to filter the inductor current and supply the load transient current. The filtering requirements are a function of the switching frequency, the ripple current and the required output ripple. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitor types and careful layout.

High frequency ceramic capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the (Equivalent Series Resistance) ESR and voltage rating requirements rather than actual capacitance requirements.

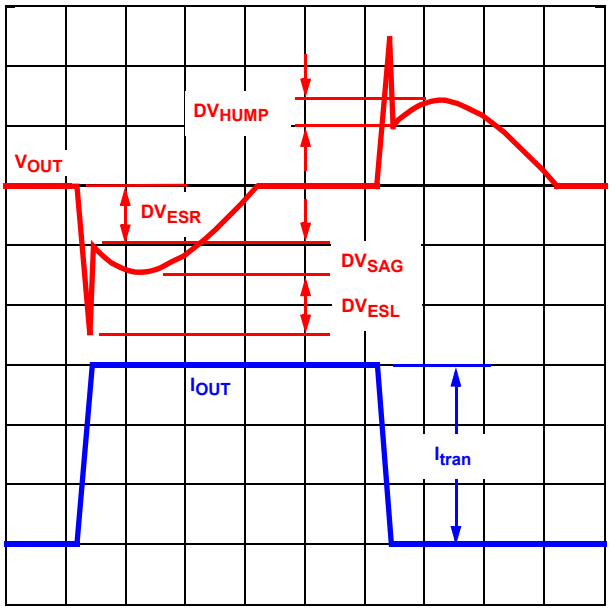


FIGURE 46. TYPICAL TRANSIENT RESPONSE

The high frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

The shape of the output voltage waveform during a load transient that represents the worst case loading conditions will ultimately determine the number of output capacitors and their type. When this load transient is applied to the converter, most of the energy required by the load is initially delivered from the output capacitors. This is due to the finite amount of time required for the inductor current to slew up to the level of the output current required by the load. This phenomenon results in a temporary dip in the output voltage. At the very edge of the transient, the Equivalent Series Inductance (ESL) of each capacitor induces a spike that adds on top of the existing voltage drop due to the ESR.

After the initial spike, attributable to the ESR and ESL of the capacitors, the output voltage experiences sag. This sag is a direct consequence of the amount of capacitance on the output.

During the removal of the same output load, the energy stored in the inductor is dumped into the output capacitors. This energy dumping creates a temporary hump in the output voltage. This hump, as with the sag, can be attributed to the total amount of capacitance on the output. Figure 46 shows a typical response to a load transient.

The amplitudes of the different types of voltage excursions can be approximated using Equations 6, 7, 8 and 9.

$$\Delta V_{ESR} = ESR \bullet I_{tran} \quad \text{(EQ. 6)}$$

$$\Delta V_{ESL} = ESL \bullet \frac{dI_{tran}}{dt} \quad \text{(EQ. 7)}$$

$$\Delta V_{SAG} = \frac{L_{out} \bullet I_{tran}^{2}}{C_{out} \bullet (V_{in} - V_{out})} \quad \text{(EQ. 8)}$$

$$\Delta V_{HUMP} = \frac{L_{out} \bullet I_{tran}^{2}}{C_{out} \bullet V_{out}} \quad \text{(EQ. 9)}$$

Where: I_{tran} = Output Load Current Transient and C_{out} = Total Output Capacitance.

In a typical converter design, the ESR of the output capacitor bank dominates the transient response. The ESR and the ESL are typically the major contributing factors in determining the output capacitance. The number of output capacitors can be determined by using Equation 10, which relates the ESR and ESL of the capacitors to the transient load step and the voltage limit (ΔVo):

$$\text{Number of Caps} = \frac{\frac{ESL \bullet I_{tran}}{dt} + ESR \bullet I_{tran}}{\Delta V_{o}} \quad \text{(EQ. 10)}$$

If ΔV_{SAG} or ΔV_{HUMP} are found to be too large for the output voltage limits, then the amount of capacitance may need to be increased. In this situation, a trade-off between output inductance and output capacitance may be necessary.

The ESL of the capacitors, which is an important parameter in the above equations, is not usually listed in specification. Practically, it can be approximated using Equation 11 if an Impedance vs Frequency curve is given for a specific capacitor:

$$ESL = \frac{1}{C(2 \bullet \pi \bullet f_{res})^{2}} \quad \text{(EQ. 11)}$$

Where: f_{res} is the resonant frequency where the lowest impedance is achieved.

The ESL of the capacitors becomes a concern when designing circuits that supply power to loads with high rates of change in the current.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the output ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by Equations 12 and 13:

$$\Delta I = \frac{(V_{IN} - V_{OUT})}{Fs \bullet L} \bullet \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 12)}$$

$$\Delta V_{OUT} = \Delta I \times ESR \quad \text{(EQ. 13)}$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient. Furthermore, the ripple current is an important signed in current mode control. Therefore, set the ripple inductor current to approximately 30% of the maximum output current or about 1A for optimized performance.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the regulator will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval, the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. Equations 14 and 15 give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L \times I_{TRAN}}{V_{IN} - V_{OUT}} \quad \text{(EQ. 14)}$$

$$t_{FALL} = \frac{L \times I_{TRAN}}{V_{OUT}} \quad \text{(EQ. 15)}$$

Where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. The worst case response time can be either at the application or removal of load. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the input voltage ripple. Use ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time the switching MOSFET turns on. Place the ceramic capacitors physically close to the MOSFET VIN pins (switching MOSFET drain) and PGND.

The important parameters for the bulk input capacitance are the voltage rating and the RMS current rating. For reliable operation, select bulk capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. Their voltage rating should be at least 1.25x greater than the maximum input voltage, while a voltage rating of 1.5x is a conservative guideline. For most cases, the RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

The maximum RMS current required by the regulator may be more closely approximated through Equation 16:

$$I_{RMS_{(MAX)}} = \sqrt{\frac{V_{OUT}}{V_{IN}} \bullet \left(I_{OUT_{(MAX)}}{}^2 + \frac{1}{12} \bullet \left(\frac{V_{IN} - V_{OUT}}{L \bullet f_s} \bullet \frac{V_{OUT}}{V_{IN}} \right)^2 \right)} \quad \text{(EQ. 16)}$$

For a through-hole design, several electrolytic capacitors may be needed, especially at temperature less than -25°C. The electrolytic's ESR can increase ten times higher than at room temperature and cause input line oscillation. In this case, a more thermally stable capacitor such as X7R ceramic should be used. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. Some capacitor series available from reputable manufacturers are surge current tested.

Loop Compensation Design

When COMP is not connected to GND, the COMP pin is active for external loop compensation. In an application where extreme temperature such as less than -10°C or greater than +85°C, external compensation mode should be used. The regulator uses constant frequency peak current mode control architecture to achieve a fast loop transient response. An accurate current sensing pilot device in parallel with the upper MOSFET is used for peak current control signal and overcurrent protection. The inductor is not considered as a state variable since its peak current is constant, and the system becomes a single order system. It is much easier to design a type II compensator to stabilize the loop than to implement voltage mode control. Peak current mode control has an inherent input voltage feed-forward function to achieve good line regulation. Figure 47 shows the small signal model of the synchronous buck regulator.

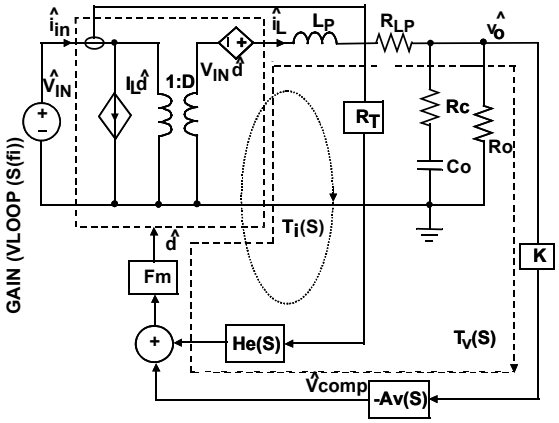


FIGURE 47. SMALL SIGNAL MODEL OF SYNCHRONOUS BUCK REGULATOR

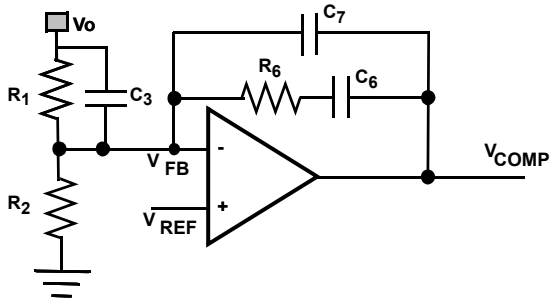


FIGURE 48. TYPE II COMPENSATOR

Figure 48 shows the type II compensator and its transfer function is expressed, as shown in Equation 17:

$$A_V(S) = \frac{\hat{v}_{comp}}{\hat{v}_o} = \frac{1}{(C_6 + C_7) \cdot R_1} \frac{\left(1 + \frac{S}{\omega_{cz1}}\right)\left(1 + \frac{S}{\omega_{cz2}}\right)}{S\left(1 + \frac{S}{\omega_{cp1}}\right)\left(1 + \frac{S}{\omega_{cp2}}\right)} \quad \text{(EQ. 17)}$$

Where,

$$\omega_{cz1} = \frac{1}{R_6 C_6}, \quad \omega_{cz2} = \frac{1}{R_1 C_3}, \omega_{cp1} = \frac{C_6 + C_7}{R_6 C_6 C_7}, \omega_{cp2} \approx 350kHz$$

Compensator Design Goal

High DC Gain

Choose Loop bandwidth f_c of approximately 50kHz or 1/10 of the switching frequency.

Gain margin: >10dB

Phase margin: >40°

The compensator design procedure is as follows:

The loop gain at crossover frequency of f_c has a unity gain. Therefore, the compensator resistance R_6 is determined by Equation 18.

$$R_6 = 2\pi f_c C_o R_t R_1 \approx f_c \cdot C_o R_1 \quad \text{(EQ. 18)}$$

Note that C_o is the actual capacitance seen by the regulator, which may include ceramic high frequency decoupling and bulk output capacitors. Ceramic may have to be derated by approximately 40% depending on dielectric, voltage stress and temperature. Compensator capacitor C_6 is then given by Equations 19 and 20.

$$C_6 = \frac{R_o C_o}{10 R_6} = \frac{V_o C_o}{10 I_o R_6} \quad \text{(EQ. 19)}$$

$$C_7 = \max\left[\frac{R_c C_o}{10 R_6}, \frac{1}{\pi f_s R_6}\right] \quad \text{(EQ. 20)}$$

An optional zero can boost the phase margin. ω_{CZ2} is a zero due to R_1 and C_3.

Put compensator zero, ω_{CZ2} from $1/2f_c$ to f_c.

$$C_3 = \frac{1}{2\pi f_c R_2} \quad \text{(EQ. 21)}$$

For internal compensation mode, R_6 is equal 600kΩ and C_6 is 30pF. Equation 18 can be rearranged to solve for R_1.

Example: V_{IN} = 12V, V_O = 5V, I_O = 3A, f_{SW} = 500kHz, R_1 = 51kΩ, R_2 = 9.7kΩ, C_o = 2x47µF/3mΩ 6.3V ceramic (~60µF with derating), L = 4.7µH, f_c = 50kHz, then compensator resistance R_6:

$$R_6 = 50k \cdot 60\mu F \cdot 51k\Omega = 153k\Omega \quad \text{(EQ. 22)}$$

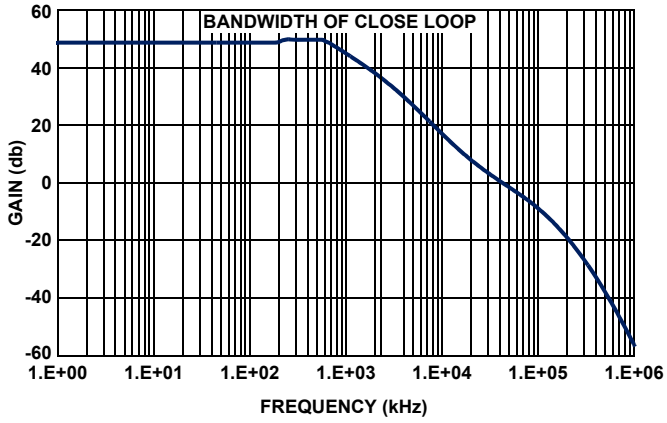
$$C_6 = \frac{5V \cdot 60\mu F}{10 \cdot 3A \cdot 153k\Omega} = 65pF \quad \text{(EQ. 23)}$$

$$C_7 = \max\left[\frac{1.5m\Omega \cdot 60\mu F}{10 \cdot 153k\Omega}, \frac{1}{\pi \cdot 500kHz \cdot 153k\Omega}\right] = (0.06pF, 4.2pF) \quad \text{(EQ. 24)}$$

Use the closest standard values for R_6, C_6 and C_7. There is approximately 3pF parasitic capacitance from V_{COMP} to GND; therefore, C_7 is optional. Use R_6 = 150kΩ, C_6 = 62pF, and C_7 = OPEN.

$$C_3 = \frac{1}{2\pi 50kHz \cdot 51k\Omega} = 62pF \quad \text{(EQ. 25)}$$

Use C_3 = 68pF. Note that C_3 may increase the loop bandwidth from the previous estimated value. Figure 49 shows the simulated voltage loop gain. It has a 42kHz loop bandwidth with 54° of phase margin and 17dB of gain margin. It may be more desirable to achieve an increased phase margin. This can be accomplished by lowering R_6 or increasing C_3 by 20% to 30%.



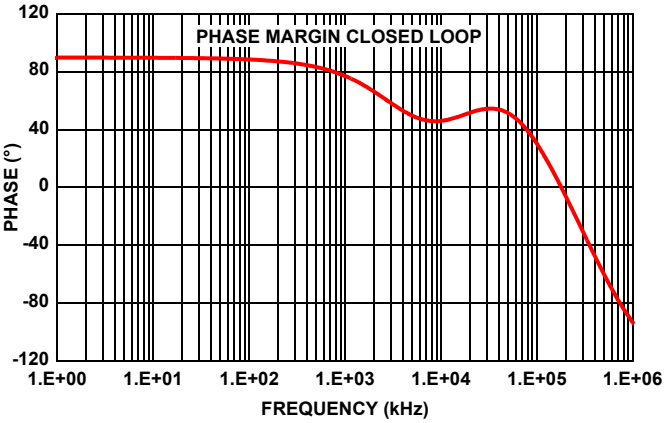


FIGURE 49. SIMULATED LOOP GAIN

Layout Considerations

The layout is very important in high frequency switching converter design. With power devices switching efficiently at 500kHz, the resulting current transitions from one device to another cause voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device overvoltage stress. Careful component layout and printed circuit board design minimizes these voltage spikes.

As an example, consider the turn-off transition of the upper MOSFET. Prior to turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is picked up by the internal body diode. Any parasitic inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components and short, wide traces minimize the magnitude of voltage spikes.

There are two sets of critical components in the regulator switching converter. The switching components are the most critical because they switch large amounts of energy and therefore tend to generate large amounts of noise. Next are the small signal components, which connect to sensitive nodes or supply critical bypass current and signal coupling.

A multi-layer printed circuit board is recommended. Figure 50 shows the connections of the critical components in the converter. Note that capacitors C_{IN} and C_{OUT} could each represent numerous physical capacitors. Dedicate one solid layer, usually a middle layer of the PC board, for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the PHASE terminals to the output inductor short. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase nodes. Use the remaining printed circuit layers for small signal wiring.

In order to dissipate heat generated by the internal LDO and MOSFETs, the ground pad should be connected to the internal ground plane through at least five vias. This allows the heat to move away from the IC and also ties the pad to the ground plane through a low impedance path.

The switching components should be placed close to the regulator first. Minimize the length of the connections between the input capacitors, C_{IN}, and the power switches by placing them nearby. Position both the ceramic and bulk input capacitors as close to the upper MOSFET drain as possible.

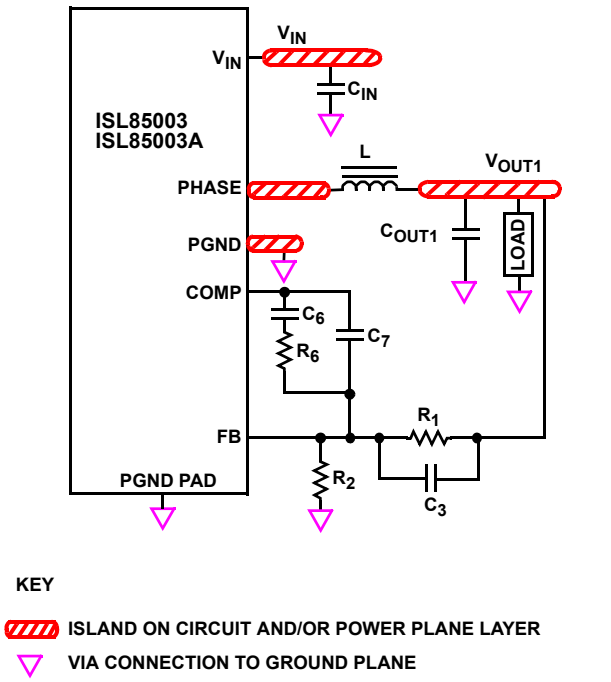


FIGURE 50. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

The critical small signal components include any bypass capacitors, feedback components and compensation components. Place the compensation components close to the FB and COMP pins. The feedback resistors should be located as close as possible to the FB pin with vias tied straight to the ground plane.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
January 15, 2016	FN7968.2	Added the Related Literature section on page 1. On page 4, updated VDD pin description by changing VIN range from “3V to 5.5V” to “4.5V to 5.5V”. Updated Note 1 in the ordering information table to include all tape and reel options. Added Table 2 on page 5. Updated POD L12.3x4 to the latest revision the changes are as follows: Tiebar Note 5 updated From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
July 17, 2014	FN7968.1	Detailed Description on page 15 changed from 4.5A to 5A. “Switching Regulator Overcurrent Protection” on page 16: Changed 4.5A to 5A. Equation 12 on page 18, updated from “dI=/(Fs*L)*Vout/Vin” to “dI=(Vin-Vout)/(Fs*L)*Vout/Vin” “Input Capacitor Selection” on page 19 : Change RESR to ESR “Negative Current Protection” on page 17: Changed -2.5A to -2.2A. Updated Package information from 4x3 to 3x4 on page 1, Pin Configuration on page 4, Ordering Information on page 5, and replaced the “Package Outline Drawing” on page 23. Updated the Ordering Information on page 5 to include the new Evaluation Boards that are now available.
March 21, 2014	FN7968.0	Initial Release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

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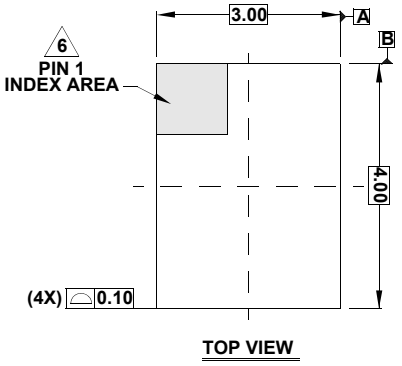
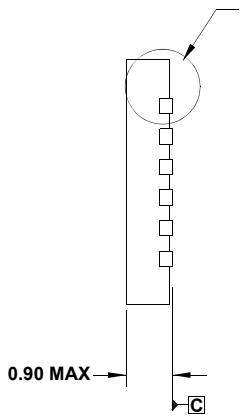
Package Outline Drawing

L12.3x4

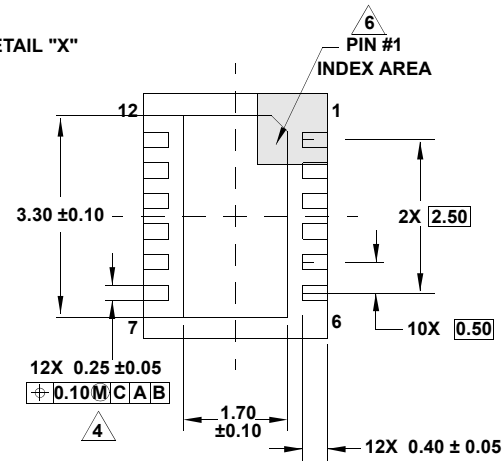
12 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 3/15



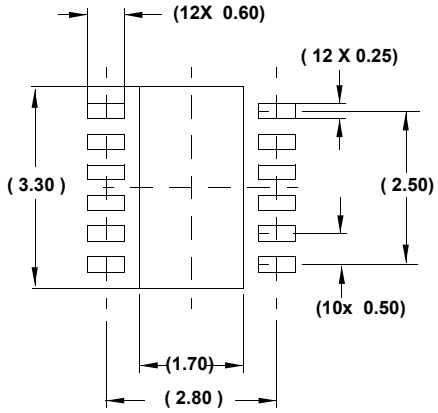
TOP VIEW



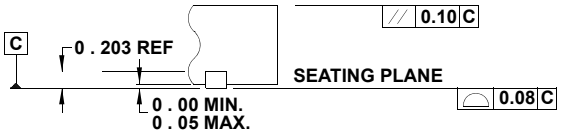
SIDE VIEW



BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Reference document JEDEC MO-229.

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ISL85003AFRZ-T7A ISL85003FRZ-T7A ISL85003EVAL2Z ISL85003DEMO1Z ISL85003AFRZ-T ISL85003FRZ ISL85003FRZ-T ISL85003AFRZ-TK ISL85003FRZ-TK ISL85003AFRZ ISL85003ADEMO1Z