USB5533B

3-Port SS/HS USB Hub Controller

PRODUCT FEATURES

Datasheet

General Description

The USB5533B hub is a 3-port SuperSpeed/Hi-Speed, low-power, configurable hub controller family fully compliant with the *USB 3.0 Specification*. The USB5533B supports 5 Gbps SuperSpeed (SS), 480 Mbps Hi-Speed (HS), 12 Mbps Full-Speed (FS) and 1.5 Mbps Low-Speed (LS) USB signaling for complete coverage of all defined USB operating speeds.

The USB5533B supports non-USB 1.2 speeds through its USB 2.0 hub controller. The new SuperSpeed hub controller operates in parallel with the USB 2.0 controller, so the 5 Gbps SuperSpeed data transfers are not affected by the slower USB 2.0 traffic.

The USB5533B supports battery charging on a per port basis. On battery charging enabled ports, the devices provide automatic USB data line handshaking. The handshaking supports USB 1.2 Charging Downstream Port (CDP), Dedicated Charging Port (DCP) and non-USB 1.2 devices.

The USB5533B is configured for operation through internal default settings, where custom configurations are supported through an on-chip OTP ROM, an external SPI ROM, or SMBus.

Features

- USB 3.0 compliant 5 Gbps, 480 Mbps, 12 Mbps and 1.5 Mbps operation, USB pins are 5 V tolerant
  - Integrated termination and pull-up/pull-down resistors
- Three downstream USB 3.0 ports
- Supports battery charging of most popular battery powered devices
  - USB-IF Battery Charging rev. 1.2 support (DCP & CDP)
  - Apple Portable product charger emulation
  - Blackberry charger emulation
  - Chinese YD/T 1591-2006 charger emulation
  - Chinese YD/T 1591-2009 charger emulation
  - Supports additional portable devices
- Emulates portable/handheld native wall chargers
  - Charging profiles emulate a handheld device's wall charger to enable fast charging (minutes vs. hours)
- Enables charging from a mobile platform that is off
- Support tablets' high current requirements
- Optimized for low-power operation and low thermal dissipation
- Vendor Specific Messaging (VSM) support for firmware upload over USB
- Configuration via OTP ROM, SPI ROM, or SMBus
- On-chip 8051 µC manages VBUS, and other hub signals
- 8 K RAM, 32 K ROM
- One Time programmable (OTP) ROM: 8 kbit
  - Includes on-chip charge pump
- Single 25 MHz XTAL or clock input for all on-chip PLL and clocking requirements
- Supports JTAG boundary scan
- PHYBoost (USB 2.0)
  - Selectable drive strength for improved signal integrity
- VariSense (USB 2.0)
  - controls the receiver sensitivity enabling four programmable levels of USB signal receive sensitivity
- IETF RFC 4122 compliant 128-bit UUID

Software Features

- Compatible with Microsoft Windows 7, Vista, XP, Mac OSX10.4+, and Linux Hub Drivers

Order Numbers:

ORDER NUMBERS*	DESCRIPTION	ROHS COMPLIANT PACKAGE	TEMPERATURE RANGE
USB5533B-5000JZX	USB 3.0 3-Port Hub with VSM, Apple/BC 1.2 Charging & UCS1002 Control	64QFN 9 x 9mm 6.0 mm exposed pad	0ºC to 70ºC
USB5533B-6080JZX	USB 3.0 3-Port Hub with VSM, Apple/BC 1.2 Charging & UCS1002 Control	64QFN 9 x 9mm 6.0 mm exposed pad	0ºC to 70ºC

* Add “TR” to the end of any order number to order tape and reel. Reel size is 3000 pieces.

This product meets the halogen maximum concentration values per IEC61249-2-21

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Conventions

Within this manual, the following abbreviations and symbols are used to improve readability.

Example	Description
BIT	Name of a single bit within a field
FIELD.BIT	Name of a single bit (BIT) in FIELD
x…y	Range from x to y, inclusive
BITS[m:n]	Groups of bits from m to n, inclusive
PIN	Pin Name
zzzzb	Binary number (value zzzz)
0xzzz	Hexadecimal number (value zzz)
zzh	Hexadecimal number (value zz)
rsvd	Reserved memory location. Must write 0, read value indeterminate
`code`	Instruction code, or API function or parameter
Section Name	Section or Document name
x	Don't care
<Parameter>	<> indicate a Parameter is optional or is only used under some conditions
{,Parameter}	Braces indicate Parameter(s) that repeat one or more times
[Parameter]	Brackets indicate a nested Parameter. This Parameter is not real and actually decodes into one or more real parameters.

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Chapter 1 Block Diagram

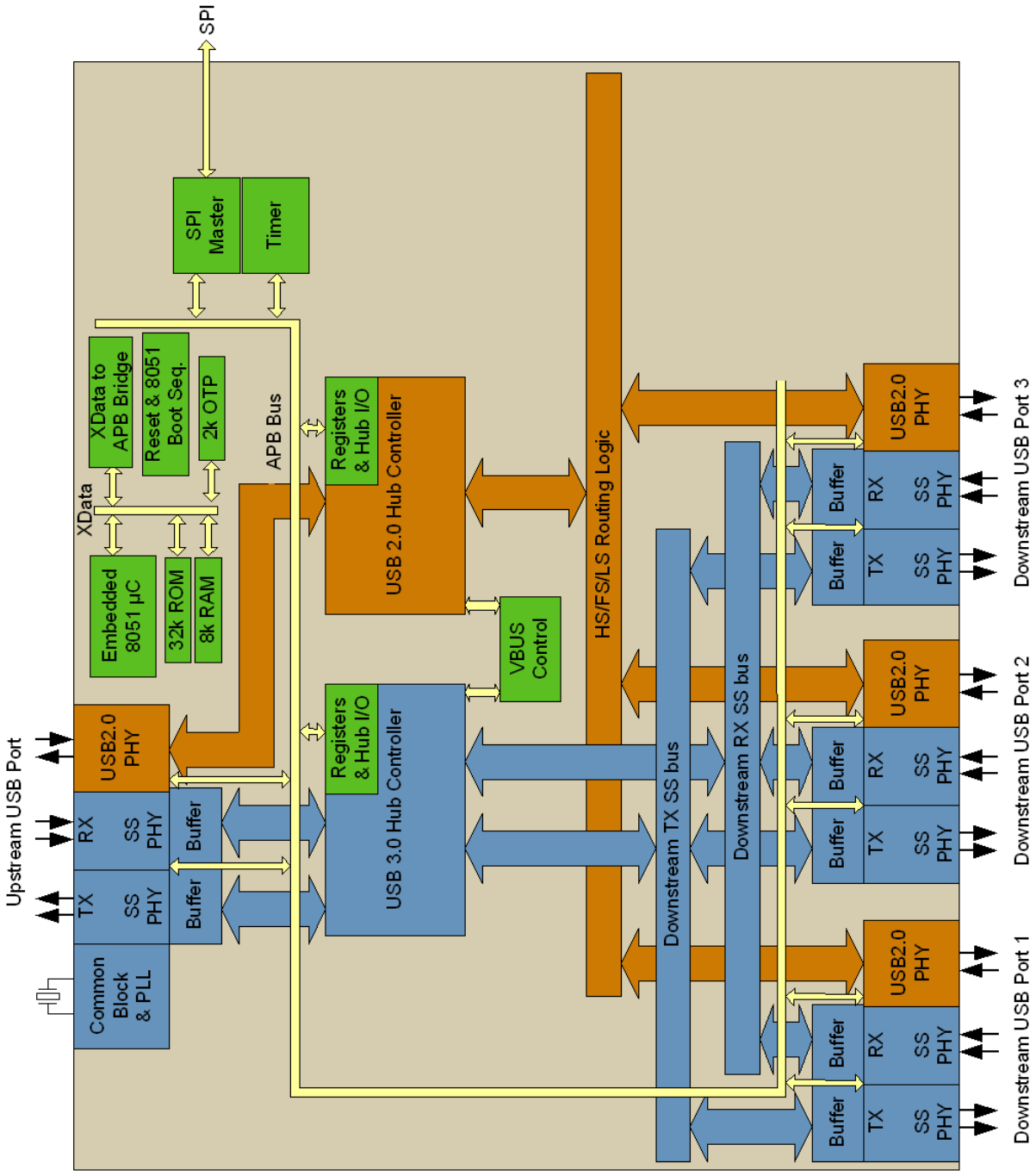

Figure 1.1 USB5533B Block Diagram

Chapter 2 Overview

The USB5533B hub is a 3-port, low-power, configurable Hub Controller fully compliant with the *USB 3.0 Specification* [2]. The USB5533B supports 5 Gbps SuperSpeed (SS), 480 Mbps Hi-Speed (HS), 12 Mbps Full-Speed (FS) and 1.5 Mbps Low-Speed (LS) USB signalling for complete coverage of all defined USB operating speeds.

All required resistors on the USB ports are integrated into the hub. This includes all series termination resistors and all required pull-down and pull-up resistors on D+ and D- pins. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

The USB5533B hub includes programmable features such as:

- **MultiTRAK™ Technology**: implements a dedicated Transaction Translator (TT) for each port. Dedicated TTs help maintain consistent full-speed data throughput regardless of the number of active downstream connections.
- **PortSwap**: allows direct alignment of USB signals (D+/D-) to connectors to avoid uneven trace length or crossing of the USB differential signals on the PCB.
- **PHYBoost**: enables 4 programmable levels of USB signal drive strength in downstream port transceivers. PHYBoost will also attempt to restore USB signal integrity.

As shown in the ordering code matrix, two USB5533B firmware versions are available: “-5000” and “-6080”. These options differ in the following ways:

- The Dynamic Charging Port feature and related DYNCPDIS_N pin function are only available on the -6080 device. Refer to Section 5.1.3: *Dynamic Charging Port (6080 Only)* for additional details.
- The TRST/DYNCPDIS_N/UCS_SMBALERT_N pin buffer type is “IPU” in the -6080 device and “I” in the -5000 device. Refer to Chapter 3: *Pin Information* on page 13 for additional details.
- The Global Suspend power consumption has been significantly lowered in the -6080 device. Refer to Section 6.3: *Power Consumption* for additional details.

2.1 Configurable Features

The USB5533B hub controller provides a default configuration that is sufficient for most applications. When initialized in the default configuration, the following features may be configured:

- Downstream non-removable ports, where the hub will automatically report as a compound device
- Downstream disabled ports
- Downstream port power control and over-current detection on a ganged or individual basis
- USB signal drive strength
- USB differential pair pin location

The USB5533B hub controllers can alternatively be configured by OTP or as an SMBus slave device. When configured by an OTP or over SMBus, the following configurable features are provided:

- Support for compound devices on a port-by-port basis
- Selectable over-current sensing and port power control on an individual or ganged basis to match the circuit board component selection
- Customizable vendor ID, product ID, and device ID
- Configurable delay time for filtering the over-current sense inputs

- Indication of the maximum current that the hub consumes from the USB upstream port
- Indication of the maximum current required for the hub controller
- Custom string descriptors (up to 30 characters): Product, manufacturer, and serial number

Chapter 3 Pin Information

This chapter outlines the pinning configurations for each chip. The detailed pin descriptions are listed by function in Section 3.2: *Pin Descriptions (Grouped by Function)* on page 14.

3.1 Pin Configurations

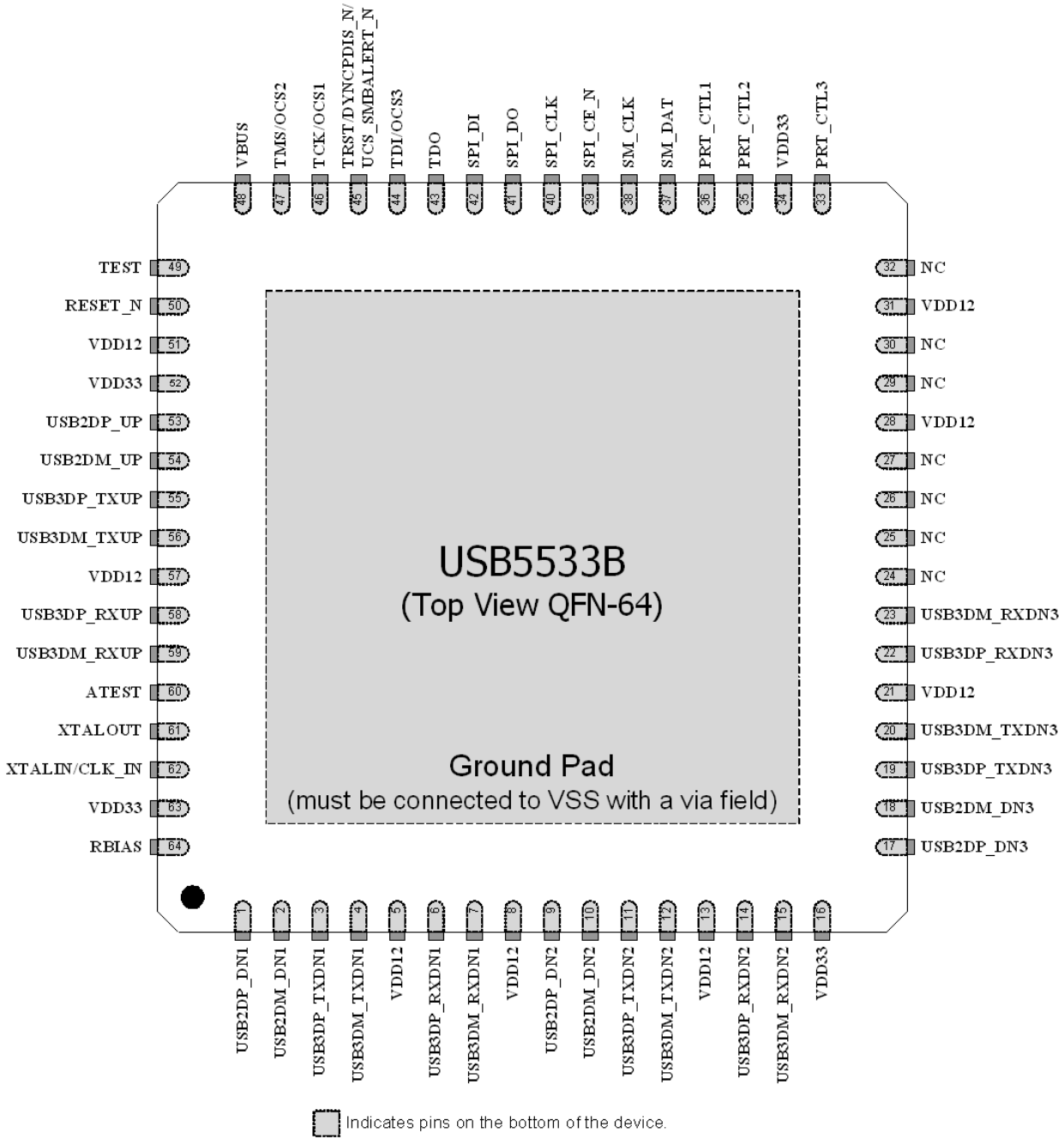

Figure 3.1 USB5533B 64-Pin QFN

3.2 Pin Descriptions (Grouped by Function)

An *N* at the end of a signal name indicates that the active (asserted) state occurs when the signal is at a low voltage level. When the *N* is not present, the signal is asserted when it is at a high voltage level. The terms assertion and negation are used exclusively in order to avoid confusion when working with a mixture of active low and active high signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

Table 3.1 USB5533B Pin Descriptions

SYMBOL	BUFFER TYPE	DESCRIPTION
USB 3.0 INTERFACE		
USB3DP_TXUP	IO-U	USB 3 Upstream Upstream SuperSpeed transmit data plus
USB3DM_TXUP	IO-U	USB 3 Upstream Upstream SuperSpeed transmit data minus
USB3DP_RXUP	IO-U	USB 3 Upstream Upstream SuperSpeed receive data plus
USB3DM_RXUP	IO-U	USB 3 Upstream Upstream SuperSpeed receive data minus
USB3DP_TXDN[3:1]	IO-U	USB 3 Downstream Downstream SuperSpeed transmit data plus for ports 1 through 3.
USB3DM_TXDN[3:1]	IO-U	USB 3 Downstream Downstream SuperSpeed transmit data minus for ports 1 through 3.
USB3DP_RXDN[3:1]	IO-U	USB 3 Downstream Downstream SuperSpeed receive data plus for ports 1 through 3.
USB3DM_RXDN[3:1]	IO-U	USB 3 Downstream Downstream SuperSpeed receive data minus for ports 1 through 3.
USB 2.0 INTERFACE		
USB2DP_UP	IO-U	USB Bus Data These pins connect to the upstream USB bus data signals.
USB2DM_UP	IO-U	USB Bus Data These pins connect to the upstream USB bus data signals.
USB2DP_DN[3:1]	IO-U	USB Downstream Downstream Hi-Speed data plus for ports 1 through 3.
USB2DM_DN[3:1]	IO-U	USB Downstream Downstream Hi-Speed data minus for ports 1 through 3.

Table 3.1 USB5533B Pin Descriptions (continued)

SYMBOL	BUFFER TYPE	DESCRIPTION
USB PORT CONTROL		
PRT_PWR[3:1]/ PRT_CTL[3:1]	O12	USB Power Enable Enables power to USB peripheral devices downstream. **Note:** This pin also provides configuration strap functions. See .
VBUS	I	Upstream VBUS Power Detect This pin can be used to detect the state of the upstream bus power.
SPI INTERFACE (4 PINS)		
SPI_CE_N	O12	SPI Enable
SPI_CLK	O12	SPI Clock
SPI_DO	O12	SPI Serial Data Out The output for the SPI port. **Note:** This pin also provides configuration strap functions. See Note 3.1.
SPI_DI	I	SPI Serial Data In The SPI data in to the controller from the ROM. This pin has a weak internal pull-down applied at all times to prevent floating.
JTAG/OCS INTERFACE		
TRST	IPU (Note 3.3)	JTAG Asynchronous Reset **Note:** If using the SMBus interface, a pull-up on this signal will enable Legacy Mode, while leaving it unconnected or pulled-down will enable Advanced Mode. **Note:** Only available in test mode.
DYNCPDIS_N		Dynamic Charging Port Disable This active-low signal is used to globally disable Battery Charging support on all USB downstream ports configured as Charging Ports. **Note:** This signal available in -6080 versions only
UCS_SMBALERT_N		UCS1002 SMBus Alert When charging port is enabled and SMBus devices are used, this signal acts as an active-low SMBus alert.

Table 3.1 USB5533B Pin Descriptions (continued)

SYMBOL	BUFFER TYPE	DESCRIPTION
TCK	I	JTAG Clock This input is used for JTAG boundary scan and has a weak pull-down. It can be left floating or grounded when not used. If the JTAG is connected, then this signal will be detected high, and the software disables the pull up after reset. **Note:** Only available in test mode.
OCS1		Over-Current Sense 1 Input from external current monitor indicating an over-current condition. **Note:** This pin also provides configuration strap functions. See Note 3.2.
TMS	I	JTAG TMS Used for JTAG boundary scan. **Note:** Only available in test mode.
OCS2		Over-Current Sense 2 Input from external current monitor indicating an over-current condition. **Note:** This pin also provides configuration strap functions. See Note 3.2.
TDI	I	JTAG TDI Used for JTAG boundary scan. **Note:** Only available in test mode.
OCS3		Over-Current Sense 3 Input from external current monitor indicating an over-current condition. **Note:** This pin also provides configuration strap functions. See Note 3.2.
TDO	O12	JTAG TDO Used for JTAG boundary scan. **Note:** Only available in test mode.
MISC		
RESET_N	IS	Reset Input The system uses this active low signal to reset the chip. The active low pulse should be at least 1 µs wide.
XTALIN	ICLKx	Crystal Input: 25 MHz crystal. This pin connects to either one terminal of the crystal or to an external 25 MHz clock when a crystal is not used.
CLK_IN		External Clock Input This pin connects to either one terminal of the crystal or to an external 25 MHz clock when a crystal is not used.

Table 3.1 USB5533B Pin Descriptions (continued)

SYMBOL	BUFFER TYPE	DESCRIPTION
XTALOUT	OCLKx	Crystal Output The clock output, providing a crystal 25 MHz. When an external clock source is used to drive **XTALIN/CLK_IN**, this pin becomes a no connect.
TEST	IPD	Test Pin Treat as a no connect pin or connect to ground. No trace or signal should be routed or attached to this pin.
RBIAS	I-R	USB Transceiver Bias A12.0 kΩ (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings.
ATEST	A	Analog Test Pin This signal is used for testing the chip and must always be connected to ground.
SM_CLK	I/O12	SMBus Clock
SM_DAT	I/O12	SMBus Data Pin
(7) **NC**	-	No connect pins
DIGITAL AND POWER		
(4) **VDD33**		3.3 V Power
(8) **VDD12**		1.25 V Power
VSS		Ground Pad This exposed pad is the device's only connection to VSS and the primary thermal conduction path. Connect to an appropriate via field.

The PRT_PWR[3:1] pins can optionally provide additional configuration strap functions to enable/disable the associated port and configure its battery charging capabilities. Configuration strap values are latched on device reset. Table 3.2 details the functions associated with the various strap settings.

Strapping features are enabled by default and can be optionally disabled via the Pro-Touch software programming tool. For additional information on the Pro-Touch programming tool, contact your local sales representative.

Strapping functions are not supported for designs that support OCS but not power switching.

Table 3.2 PRT_PWR[3:1] Configuration Strap States

PRT_PWR[3:1] STRAP SETTING	PORT STATE	BATTERY CHARGING
No Pull-Up or Pull-Down	Enabled	Disabled
Pull-Down: <10 kΩ to VSS	Disabled	N/A
Pull-Up: <10 kΩ and >1 kΩ to VDD33	Enabled	Enabled

Note 3.1 The SPI_DO pin provides an additional SPI_SPD_SEL configuration strap function. SPI_SPD_SEL selects between the 30MHz SPI Mode when pulled-down to ground (default) and the 60MHz SPI Mode when pulled-up to VDD33. The SPI_SPD_SEL strap value is latched on Power-On Reset (POR) or RESET_N deassertion.

Note 3.2 The OCS[3:1] pins can optionally provide additional configuration strap functions. To set the associated port into the non-removable state, the OCS pin must be configured with a pull-down (<10 kΩ to VSS). Otherwise, the port will be configured in the removable state. Configuration strap values are latched on device reset.

Strapping features are enabled by default and can be optionally disabled via the Pro-Touch software programming tool. For additional information on the Pro-Touch programming tool, contact your local sales representative.

Strapping functions are not supported for designs that support OCS but not power switching.

Note 3.3 This pin has an internal pull-up only in the -6080 version. The internal pull-up is only active after the SMBus mode (Legacy/Advanced) configuration strap has been sampled at POR or reset. The -5000 version is an “I” type buffer.

3.3 Buffer Type Descriptions

Table 3.3 Buffer Type Descriptions

BUFFER TYPE	DESCRIPTION
I	Input
I/O	Input/output
IPD	Input with internal weak pull-down resistor
IPU	Input with internal weak pull-up resistor
IS	Input with Schmitt trigger
O12	Output 12 mA
I/O12	Input/output buffer with 12 mA sink and 12 mA source
I/OSD12	Open drain with Schmitt trigger and 12 mA sink.
ICLKx	XTAL clock input
OCLKx	XTAL clock output
I-R	RBIAS
I/O-U	Analog input/output defined in USB specification

Chapter 4 Standard Interface Connections

4.1 SPI Interface

The hub will interface to external memory depending on configuration of the USB5533B pins associated with each interface type. The USB5533B will first check to see whether an external SPI Flash is present. If not, the USB5533B will operate from internal ROM. If SPI Flash is present, the chip will operate from the external ROM.

The USB5533B is capable of code execution from an external SPI ROM. On power up, the firmware looks for an external SPI flash device that contains a valid signature of `2DFU` (device firmware upgrade) beginning at address 0xFFFA. If a valid signature is found, then the external ROM is enabled and the code execution begins at address 0x0000 in the external SPI device. If a valid signature is not found, then execution continues from internal ROM. The following sections describe the interface options to the external SPI ROM.

4.1.1 Operation of the Hi-Speed Read Sequence

The SPI controller will automatically handle code reads going out to the SPI ROM Address. When the controller detects a read, the controller drops the **SPI_CE**, and puts out a 0x0B, followed by the 24-bit address. The SPI controller then puts out a DUMMY byte. The next eight clocks clock in the first byte. When the first byte is clocked in a ready signal is sent back to the processor, and the processor gets one byte.

After the processor gets the first byte, its address will change. If the address is one more than the last address, the SPI controller will clock out one more byte. If the address in anything other than one more than the last address, the SPI controller will terminate the transaction by taking **SPI_CE** high. As long as the addresses are sequential, the SPI Controller will keep clocking in data.

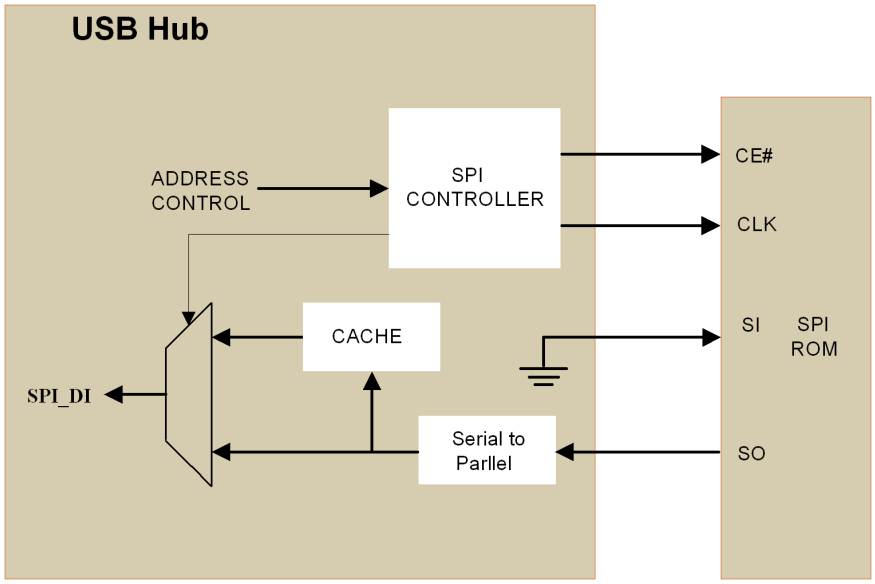

Figure 4.1 SPI Hi-Speed Read Operation

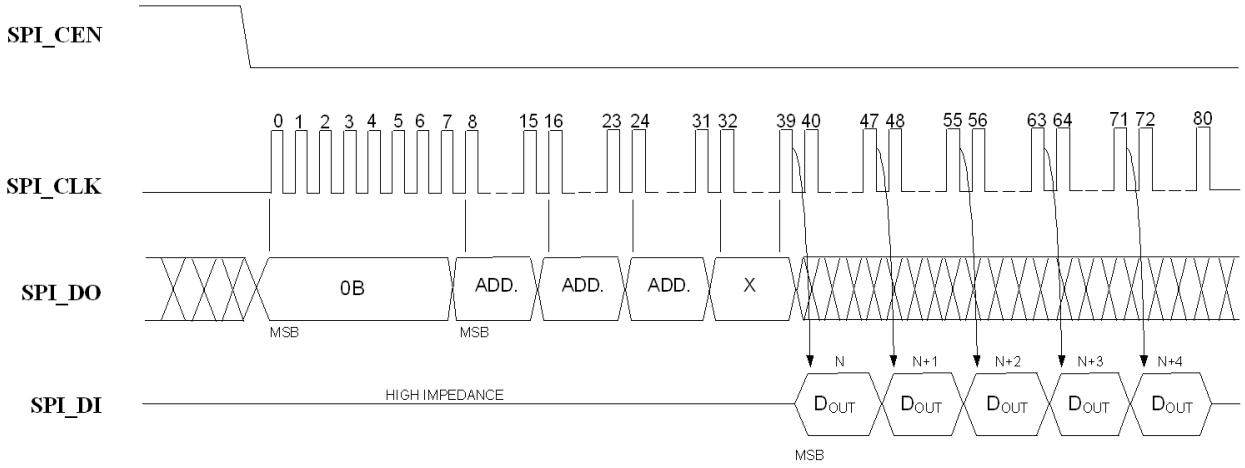

Figure 4.2 SPI Hi-Speed Read Sequence

4.1.2 Operation of the Dual Hi-Speed Read Sequence

The SPI controller also supports dual data mode (at 30 MHz SPI speed only). When configured in dual mode, the SPI controller will automatically handle reads going out to the SPI ROM. When the controller detects a read, the controller drops the **SPI_CE_N**, and puts out a 0x3B, followed by the 24-bit address. The SPI controller then puts out a DUMMY byte. The next four clocks clock in the first byte. The data appears two bits at a time on data out and data in. When the first byte is clocked in a ready signal is sent back to the processor, and the processor gets one byte.

After the processor gets the first byte, the address will change. If the address is one more than the last address, the SPI controller will clock out one more byte. If the address in anything other than one more than the last address, the SPI controller will terminate the transaction by taking **SPI_CE_N** high. As long as the addresses are sequential, the SPI Controller will keep clocking in data.

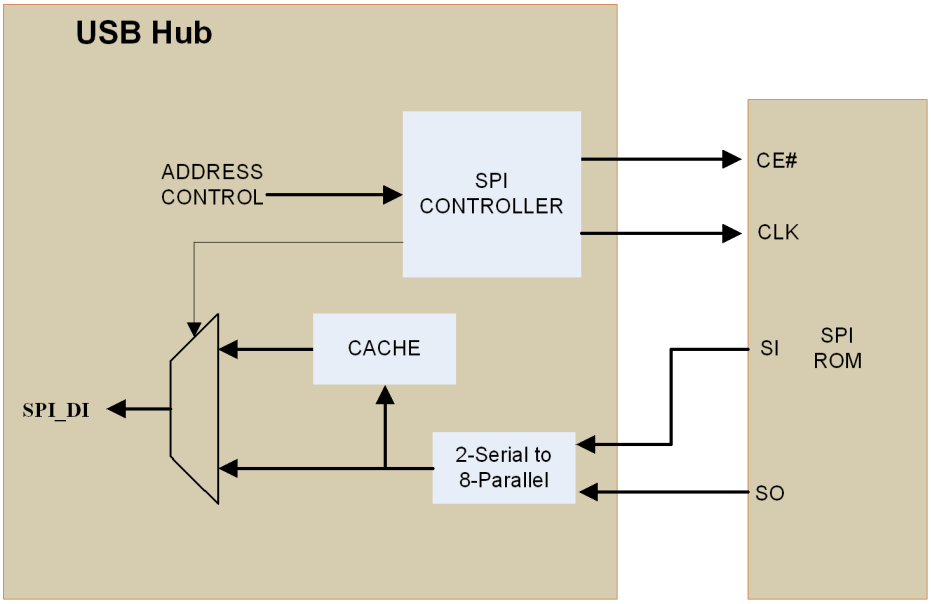

Figure 4.3 SPI Dual Hi-Speed Read Operation

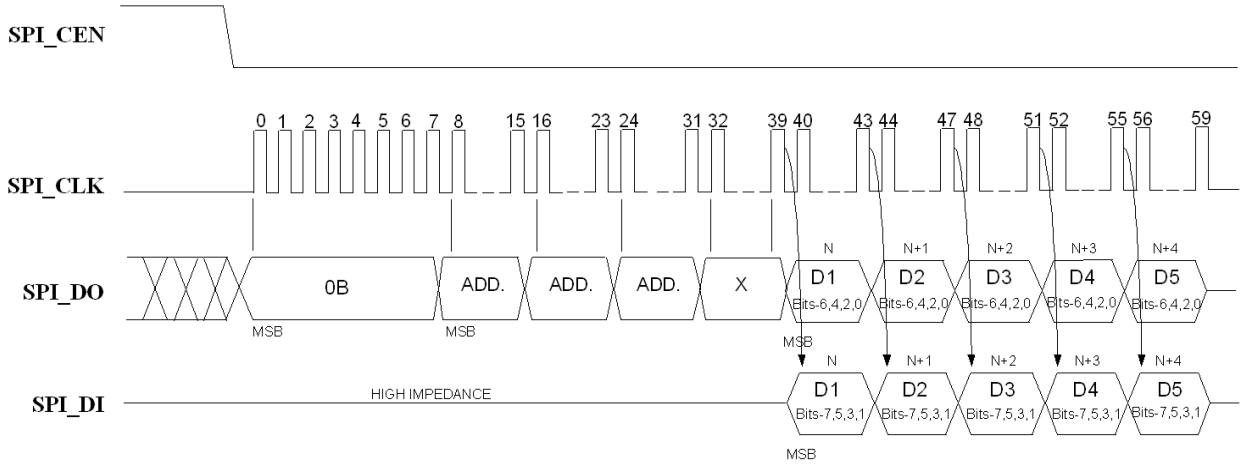

Figure 4.4 SPI Dual Hi-Speed Read Sequence

4.1.3 32-Byte Cache

There is a 32-byte pipeline cache, and associated with the cache is a base address pointer and a length pointer. Once the SPI controller detects a jump, the base address pointer is initialized to that address. As each new sequential data byte is fetched, the data is written into the cache, and the length is incremented. If the sequential run exceeds 32 bytes, the base address pointer is incremented to indicate the last 32 bytes fetched. If the USB5533B does a jump, and the jump is in the cache address range, the fetch is done in 1 clock from the internal cache instead of an external access.

4.1.4 Interface Operation to SPI Port When Not Doing Fast Reads

There is an 8-byte command buffer: SPI_CMD_BUF[7:0]; an 8-byte response buffer: SPI_RESP_BUF[7:0]; and a length register that counts out the number of bytes: SPI_CMD_LEN. Additionally, there is a self-clearing **GO** bit in the SPI_CTL Register. Once the **GO** bit is set, the device drops **SPI_CE_N**, and starts clocking. It will put out SPI_CMD_LEN X 8 number of clocks. After the first byte, the COMMAND, has been sent out, and the **SPI_DI** is stored in the SPI_RESP buffer. If the SPI_CMD_LEN is longer than the SPI_CMD_BUF, don't cares are sent out on the **SPI_DO** line. This mode is used for program execution out of internal RAM or ROM.

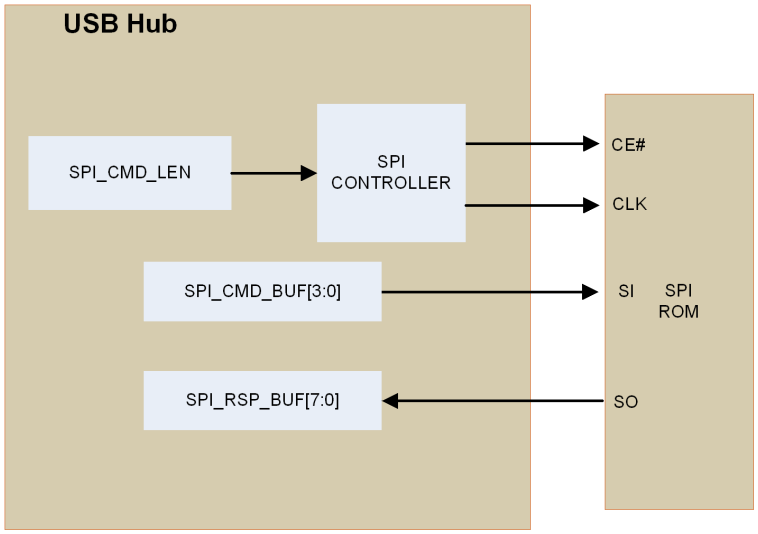

Figure 4.5 SPI Internally-Controlled Operation

4.1.4.1 ERASE EXAMPLE

To perform a SCTR_ERASE, 32BLK_ERASE, or 64BLK_ERASE, the device writes 0x20, 0x52, or 0xD8, respectively to the first byte of the command buffer, followed by a 3-byte address. The length of the transfer is set to 4 bytes. To do this, the device first drops **SPI_CE_N**, then counts out 8 clocks. It then puts out the 8 bits of command, followed by 24 bits of address of the location to be erased on the **SPI_DO** pin. When the transfer is complete, the **SPI_CE_N** goes high, while the **SPI_DI** line is ignored in this example.

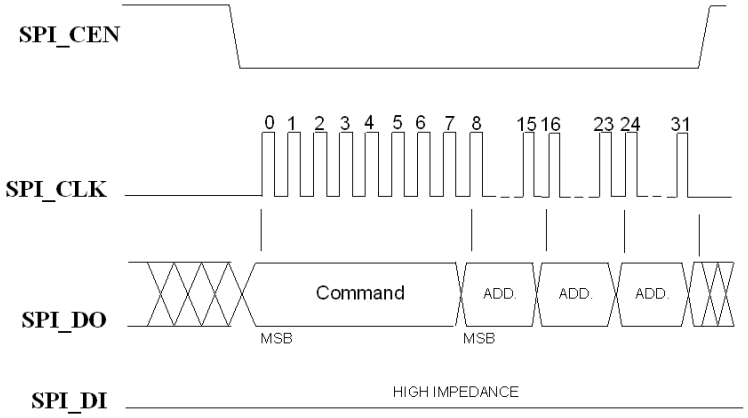

Figure 4.6 SPI Erase Sequence

4.1.4.2 BYTE PROGRAM EXAMPLE

To perform a Byte Program, the device writes 0x02 to the first byte of the command buffer, followed by a 3-byte address of the location that will be written to, and one data byte. The length of the transfer is set to 5 bytes. The device first drops **SPI_CE_N**, 8 bits of command are clocked out, followed by 24 bits of address, and one byte of data on the **SPI_DO** pin. The **SPI_DI** line is not used in this example.

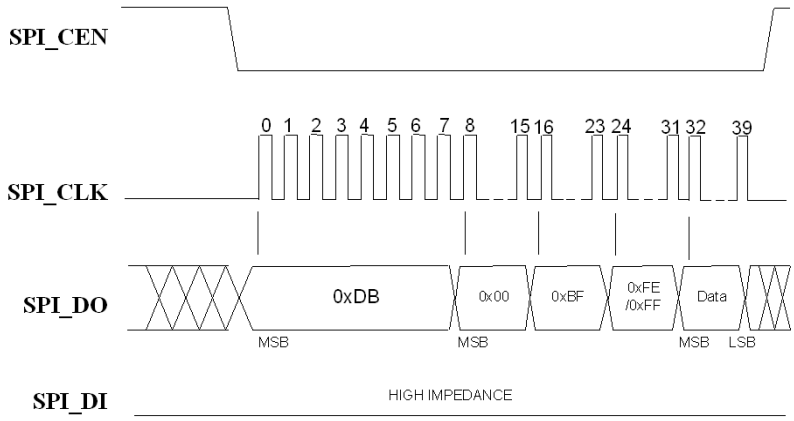

Figure 4.7 SPI Byte Program

4.1.4.3 COMMAND ONLY PROGRAM EXAMPLE

To perform a single byte command such as the following:

- WRDI
- WREN
- EWSR
- CHIP_ERASE
- EBSY
- DBSY

The device writes the opcode into the first byte of the SPI_CMD_BUF and the SPI_CMD_LEN is set to one. The device first drops **SPI_CE**, then 8 bits of the command are clocked out on the **SPI_DO** pin. The **SPI_DI** is not used in this example.

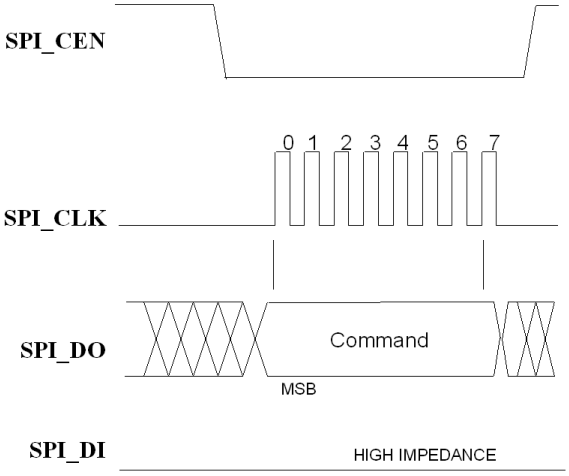

Figure 4.8 SPI Command Only Sequence

4.1.4.4 JEDEC-ID READ EXAMPLE

To perform a JEDEC-ID command, the device writes 0x9F into the first byte of the SPI_CMD_BUF and the length of the transfer is 4 bytes. The device first drops **SPI_CE_N**, then 8 bits of the command are clocked out, followed by the 24 bits of dummy bytes (due to the length being set to 4) on the **SPI_DO** pin. When the transfer is complete, the **SPI_CE_N** goes high. After the first byte, the data on **SPI_DI** is clocked into the SPI_RSP_BUF. At the end of the command, there are three valid bytes in the SPI_RSP_BUF. In this example, 0xBF, 0x25, 0x8E.

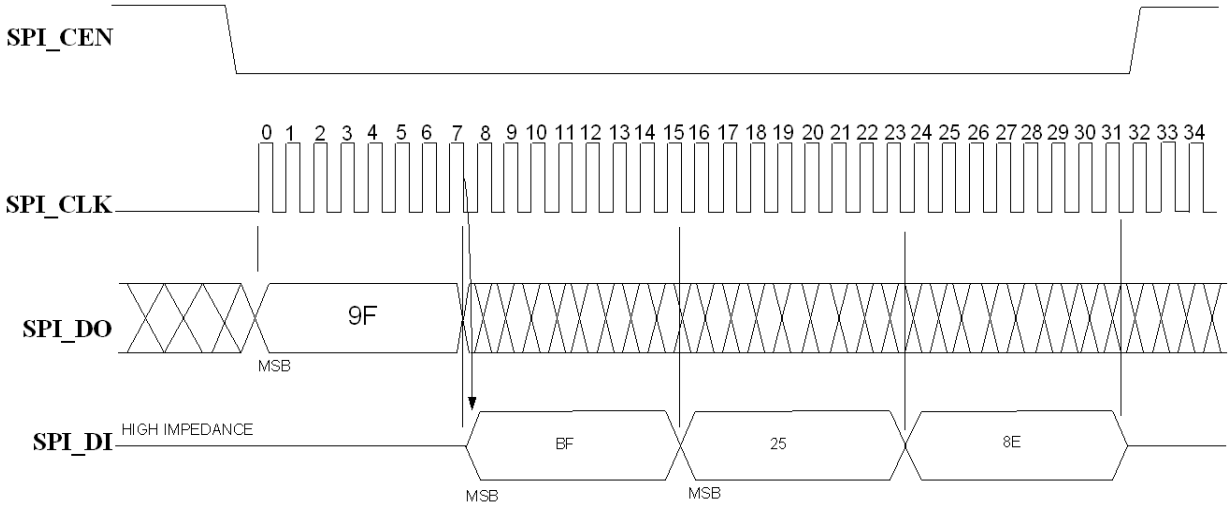

Figure 4.9 SPI JEDEC-ID Sequence

4.2 SMBus Slave Interface

Next, the USB5533B will look to receive configuration and commands from an optional SMBus master (if present). When SMBus is enabled, the SMBus can operate in either legacy (USB 2.0 only) or advanced mode (access to both USB 2.0 and 3.0 registers). Next, the USB5533B will look for (optional) configuration present in the internal OTP memory. Any register settings that are modified via the SMBus interface will overwrite the internal OTP settings.

The SMBus slave interface is enabled when pull-up resistors are detected on both **SM_DAT** and **SM_CLK** for the first millisecond after reset. For operation in SMBus Legacy Mode, an additional pull-up resistor is required on **TRST**. If the SMBus interface is enabled, then the USB5533B will wait indefinitely for the SMBus host to configure the device. Once SMBus configuration is complete, device initialization will proceed. To disable the SMBus, a pull-down resistor of 10 KΩ must be applied to **SM_DAT**. If SMBus is disabled, the device proceeds directly to device initialization using the internal OTP ROM.

4.2.1 Pull-Up Resistor for SMBus

External pull-up resistors (10 kΩ recommended) are required on the **SM_DAT** and **SM_CLK** pins when implementing either SMBus mode.

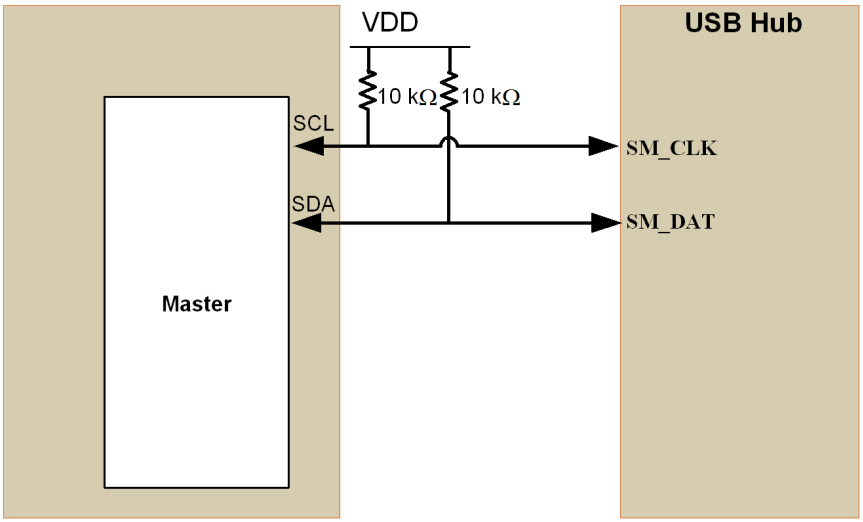

Figure 4.10 SMBus Slave Connection

4.2.1.1 Invalid Protocol Response Behavior

Note that any attempt to update registers with an invalid protocol will not be updated. The only valid protocols are write block and read block (described Section 5.5: *SMBus Slave Interface* on page 37), where the hub only responds to the 7-bit hardware selected slave addresses (0101100b or 0101101b). Additionally, the only valid registers for the hub are outlined in the *USB5533B Configuration Release Notes* documentation.

4.2.2 Slave Device Timeout

Devices in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds 25 ms ($T_{TIMEOUT, MIN}$). The master must detect this condition and generate a stop condition within or after the transfer of the interrupted data byte. Slave devices must reset their communication and be able to receive a new START condition no later than 35 ms ($T_{TIMEOUT, MAX}$).

Note: Some simple devices do not contain a clock low drive circuit; this simple kind of device typically resets its communications port after a start or stop condition. The slave device timeout must be implemented.

4.2.3 Stretching the SCLK Signal

The hub supports stretching of the **SCLK** by other devices on the SMBus. The hub will stretch the clock as needed.

4.2.4 Bus Reset Sequence

The SMBus slave interface resets and returns to the idle state upon a START condition followed immediately by a STOP condition.

4.2.5 SMBus Alert Response Address

The SMBALERT# signal is not supported by the USB5533B.

4.3 Reset

There are two different resets that the device experiences. One is a hardware reset (either from the internal POR reset circuit or via the **RESET_N** pin) and the second is a USB Bus Reset.

4.3.1 Internal POR

All reset timing parameters are guaranteed by design.

4.3.2 External Hardware Reset

A valid hardware reset is defined as assertion of **RESET_N** for a minimum of 1 µs after all power supplies are within operating range.

Assertion of **RESET_N** (external pin) causes the following:

1. The PHY is disabled, and the differential pairs will be in a high-impedance state.
2. All transactions immediately terminate; no states are saved.
3. All internal registers return to the default state.
4. The external crystal oscillator is halted.
5. The PLL is halted.

4.4 Standard Port Power Configuration

The device natively operates with standard port power controllers or poly-fuse devices for the downstream port powers when battery charging is not enabled on a port. It is not recommended to have the downstream ports of a single device mix poly-fuse and standard power controller support, as the configuration of the hub cannot correctly report which ports are poly-fuse and which are port power controllers to the host.

Any port without battery charging can also be used in individual port power controls or ganged power controls. The port power control output only supports either Ganged or Individual modes on a global basis for all downstream ports.

The overcurrent setting also supports individual or global settings, but also adds the ability to configure specific ports to be part of an overcurrent gang with others setup for individual connections. This hybrid configuration should only be used when utilizing poly-fuse power devices.

4.4.1 Port Power Controller

The most common method for downstream port power controls is to utilize current-limited power switches for USB applications. The devices allow the downstream port powers to be enabled through a control signal and report over-current conditions through a flag output.

Two connection methods are possible for these controllers, Combined mode and Independent mode.

In Combined mode, the FLG and EN signals are tied together with an external 10K ohm pull-up and driven to a single PRT_CTL signal on the device, as shown in Figure 4.11.

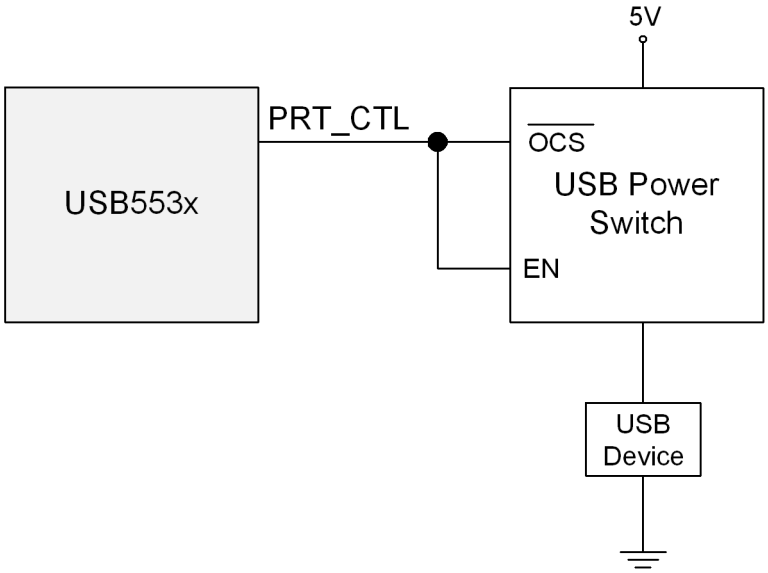

Figure 4.11 Combined Mode Implementation

In Individual mode, the PRT_CTL signal is driven directly to the EN input of the power switch and the OCS input is connected to the FLG output of the power switch with a 10K pull-up connected, as shown in Figure 4.12.

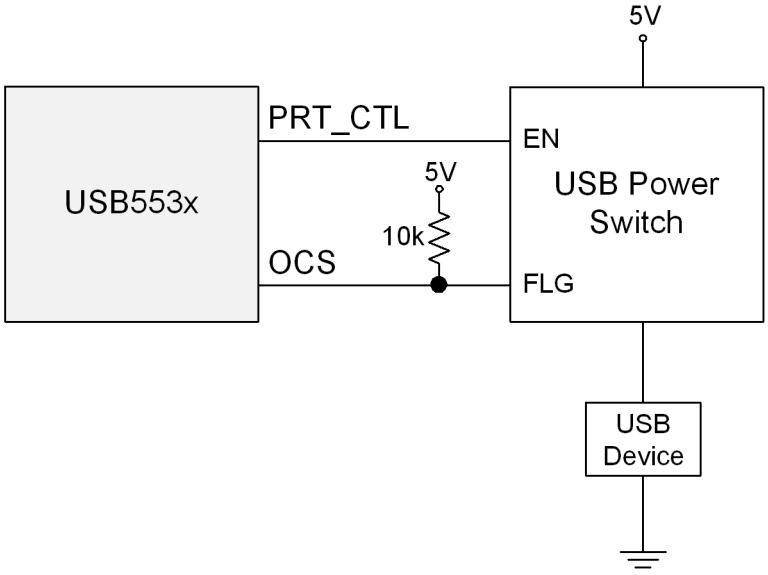

Figure 4.12 Individual Mode Implementation

4.4.2 Poly-Fuse

An alternate method of downstream power control is to utilize poly-fuse devices. In this configuration, the poly-fuse devices are used to report overcurrent conditions to the USB5533B through the OCS input, as shown in Figure 4.13.

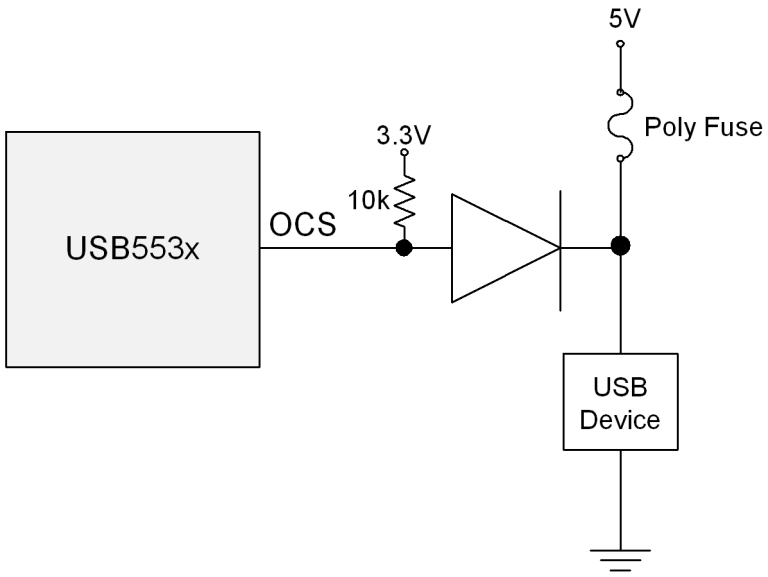

Figure 4.13 Poly-Fuse Implementation

4.5 Charging Port Configurations

The device can also be configured to operate as a charging port for one or more downstream ports. Ganged port power control and/or overcurrent is not supported if any of the downstream ports are configured as charging ports. If a port is configured to support a charging port mode, either a standard port power controller or a UCS1002 may be implemented.

For more information on charging port support, refer to Section 5.1: *Charging Port Configuration* on page 30.

4.5.1 Port Power Controller

The only special limitation of using the device as a charging port is that the port power controller must be capable of the higher current to support the charging port modes. Refer to Section 4.4.1: *Port Power Controller* on page 27 for more information on this implementation.

4.5.2 UCS1002

Using a UCS1002 device as a downstream port power controller is only supported on ports that are enabled as charging ports.

If the UCS1002 is implemented, the USB5533B communicates with all of the implemented UCS1002 ports over SMBus using one of the PRT_CTLx/OCSx signals as the SMCLK/SMDAT. Additionally, DYNCPDIS_N becomes the UCS_SMBALERT_N signal. Multiple UCS1002 devices may be connected to the SMBus in parallel.

After reset, for any enabled charging ports, the USB5533B performs SMBus commands on the configured PRT_CTLx/OCSx signals and checks UCS1002 devices at specific addresses (see Table 4.1) to confirm which ports are utilizing UCS1002 devices as the downstream power controllers.

Table 4.1 UCS1002 Address Mapping

PORT	ADDRESS
1	0x30
2	0x31
3	0x32

In this configuration, the UCS1002 is utilized as an SMBus enabled port power switch and all charging port handshaking on the D+/D- signals are controlled directly from the USB5533B. An example implementation can be seen in Figure 4.14.

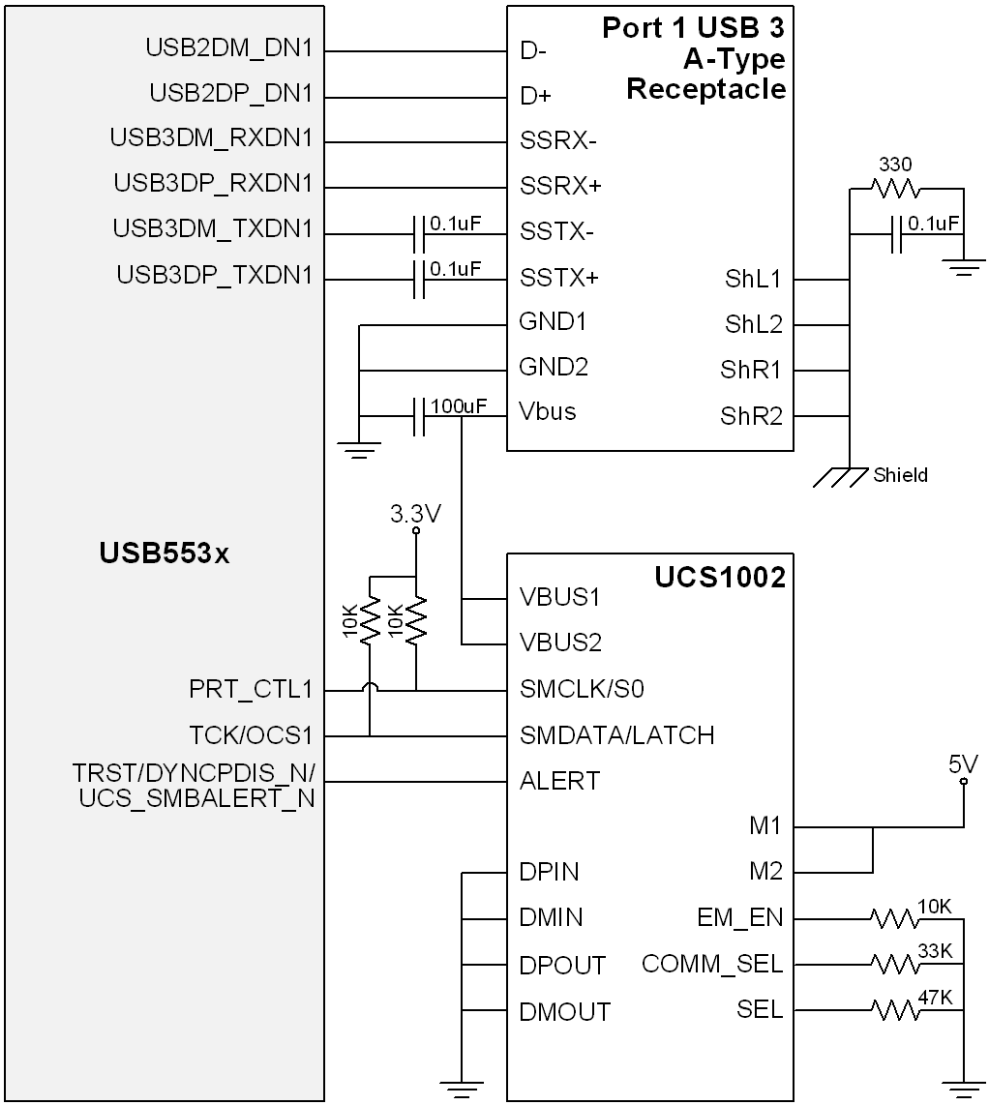

Figure 4.14 UCS1002 Charging Implementation

Chapter 5 Functional Operation

This chapter details the functional operation of various device features.

5.1 Charging Port Configuration

The USB5533B supports downstream charging ports on any available port. The hub contains internal hardware and algorithms to natively support various voltage levels on the D+/D- signals along with the BC 1.2 Handshaking protocol, allowing charging devices to detect the downstream port as a charging port.

A port can be configured for either RapidCharge support or Samsung Legacy Charging mode support. This section details the various charging port modes. The following terminology will be helpful in the understanding of these features:

- SDP - Standard Downstream Port - A port that is not operating as a charging port and has active USB communications.
- CDP - Charging Downstream Port - A port that is operating as a charging port and has active USB communications.
- DCP - Dedicated Charging Port - A port that is operating as a charging port but has no USB communications.
- S0 - Normal system power state in full run.
- S3 - Typically a Sleep state, where the system can be woken from USB HID devices
- S4 - Typically a Hibernate sleep state, where the system state is stored to a hard drive and does not support wake from USB HID devices.
- S5 - Typically an OFF state for a system.

5.1.1 Rapid Charge

This mode enables concurrent operation of Apple, BC 1.2 and DP/DM Shorted Emulation charging. The only applicable options are to choose Apple 1A or Apple 2A charging mode on a per port basis. Refer to Section 5.2.1.1: *Apple Charging Mode* on page 32.

Note: Apple and DP/DM Shorted Emulation charging modes are only operational in DCP mode.

5.1.2 Samsung Legacy Charging

This mode drives a specified voltage on the DP/DM lines to allow legacy Samsung devices to detect the port as Charging capable. This is only operational in DCP modes.

5.1.3 Dynamic Charging Port (6080 Only)

Dynamic Charging Port support utilizes the device's DYNCPDIS_N pin to disable Battery Charging support globally when low and, when high, allow any ports configured as Charging Ports (either through a configuration file or straps) to resume their Battery Charging operation in the configured Charging mode.

This feature is currently supported only when using standard USB port power controllers. Please contact your Microchip FAE if required to use this feature with other port power controller configurations.

Figure 5.1, Figure 5.2, and Figure 5.3 detail the operation of Dynamic Charging Port in the S0, S3, and S4/S5 power modes, respectively. For any of the flow diagram transitions, there is a Y/Z nomenclature.

Y = Dynamic BC enable signal

Z = Device attached and sensed by device

Note: The Dynamic Charging Port feature and related DYNCPDIS_N pin function is available in the "-6080" version of the device only.

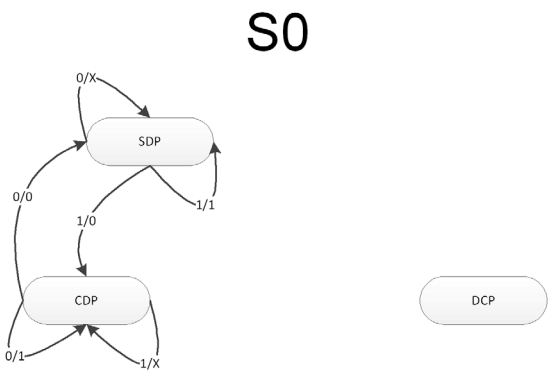

Figure 5.1 S0 State Transitions

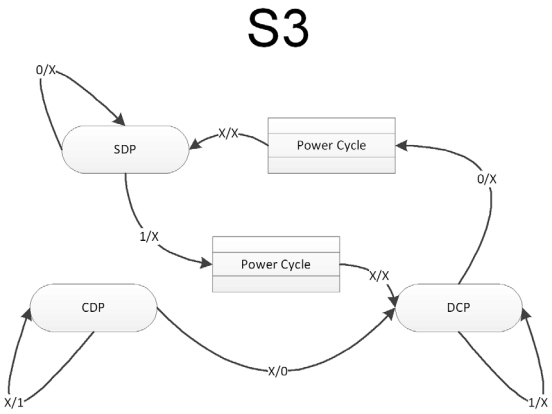

Figure 5.2 S3 State Transitions

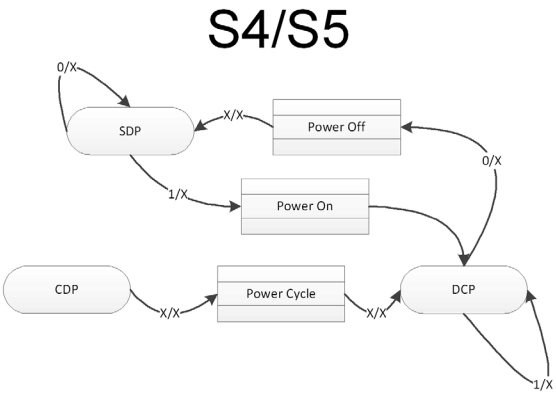

Figure 5.3 S4/S5 State Transitions

5.2 Configuration Options

By default, the USB5533B configuration allows the device to operate as a standard USB hub when connected to a USB host controller. The device also contains a number of configurable options which can be set through its user interfaces:

- One-Time Programmable (OTP) Memory (one time burn configuration)
- External SPI (only when using external SPI firmware)
- SMBus Slave Interface (controlled by SMBus host controller. Must be updated every time.)

Refer to Chapter 4: *Standard Interface Connections* on page 20 for details on the SPI and SMBus interfaces.

SPI and OTP configuration can be created and applied through the Protouch tool. The following subsections detail to various device parameters that can be configured via the Protouch tool.

5.2.1 Charging Port Enable

This option enables, on a per-port basis, DFPs to become charging ports. If this is enabled on a port, it must be configured as a per-port PWR/OCS control. Ganged OCS or PWR controls are not supported concurrently. The normal configuration is to support the RapidCharge protocol. Refer to Section 5.2.17: *Port Power/OCS Control* on page 34 for more information.

5.2.1.1 Apple Charging Mode

This option enables either Apple 1 Amp or Apple 2 Amp for the RapidCharge protocol charging mode when a port is configured as a charging port and not enabled for Samsung Mode. This mode enables the selected Apple charging mode to operate concurrently with BC1.2.

5.2.1.2 Samsung Charging Mode

This option enables the Samsung Charging mode on a port. If this is selected, the Apple Charging mode setting is ignored and only the Samsung charging mode is supported on that port.

5.2.1.3 UCS1002 SMBus Interface Selection

USC1002 port power controllers are only supported if battery charging is enabled on that port. When BC is enabled, there is an option to select the external signals (PRTCTLx/OCSx) that are used for the SMBus SDA/SCL signals. Only Ports 1-4 signals can be used. This feature is supported on “-6080” and newer devices.

5.2.2 USB VID

This field is the 16-bit USB Vendor ID reported by both USB 2.0 and USB 3.0 hubs.

5.2.3 USB2 PID

This field is the 16-bit USB Product ID reported by the USB 2.0 hub only.

5.2.4 USB3 PID

This field is the 16-bit USB Product ID reported by the USB 3.0 Hub only.

5.2.5 USB DID

This field is the 16-bit USB Device ID reported by both the USB 2.0 and USB 3.0 hubs.

5.2.6 USB Non-Removable Setting

This is the per-port Non-Removable setting for both USB 2.0 and USB 3.0 hubs. If any ports are set as Non-Removable, both the USB 2.0 and USB 3.0 hubs will be automatically set to report as Compound devices.

5.2.7 USB Port Disables

This is the per-port setting used to disable ports for both USB 2.0 and USB 3.0 hubs.

5.2.8 USB Self/Bus-Powered

This setting is used to configure the USB2 and USB3 hubs to report as Self-Powered or Bus-Powered.

5.2.9 USB System Max Power

This field is the maximum total system power on VBUS including non-Removable devices if permanently attached.

5.2.10 USB Hub Max Current

This field is the maximum current of the hub and system components to support the hub on VBUS.

5.2.11 USB Language ID

This field selects the USB language ID.

5.2.12 USB Manufacturer String

This field contains the manufacturer string reported by both USB 2.0 and USB 3.0 hubs (maximum of 30 characters).

5.2.13 USB 2.0 Product String

This field contains the product string reported by the USB 2.0 hub (maximum of 30 characters).

5.2.14 USB 3.0 Product String

This field contains the product string reported by the USB 3.0 hub (maximum of 30 characters).

5.2.15 USB Serial String

This field contains the serial string reported by the USB 2.0 and USB 3.0 hubs (maximum of 30 characters).

5.2.16 Pin Strap Disables

This setting disables the external pin configuration straps on power-up that select the following on ports 1-4:

- Port Disable
- Port Non-Removable
- Battery Charging Enable

If the user needs to select the above settings in a configuration file for ports 1-4, they must also disable the pin straps to ensure the settings are not overridden by the strap controls.

5.2.17 Port Power/OCS Control

5.2.17.1 Per-Port PWR/OCS Combined Mode

This per-port setting controls whether the Power Enable and OCS signals are on the same pin. This setting is only valid for ports 1-4.

Refer to Section 4.4: *Standard Port Power Configuration* on page 26 for additional port power setting details and connection diagrams.

5.2.17.2 OCS Gang Control

This setting can gang multiple ports into an OCS ganging to report overcurrent on any port in this gang.

ALL GANGED

This single setting configures all ports into an OCS gang.

SPLIT GANGED

This setting allows the user to gang select ports together while not ganging others.

Requires the setting of the following:

- USB 2.0 hub OCS gang set
- USB 3.0 hub OCS gang set
- Ports contained within the OCS gang (any other ports will operate as a per-port power control/ocs)
- GPIO used as OCS Gang input

5.2.17.3 USB Port Power Gang Control

This setting can gang all ports into single Port Power control.

5.2.17.4 No Port Power Controls

This parameter requires setting the hubs power-on time to 0 for both USB 2.0 and USB 3.0 hubs. It also requires the setting of the USB3 PWR_SW_CTL signal.

USB POWER-ON TIME (ADVANCED)

This parameter sets the USB power-on to power Good time in 2ms intervals for both the USB 2.0 and USB 3.0 hubs.

USB 3.0 NO POWER SWITCH SELECT

When enabled, the USB 3.0 hub operates in accordance with the USB 3.0 specification for No Power Switches.

5.2.17.5 USB 2.0 Over-Current Timer

This setting controls the signal filter on the OCS pin for the USB 2.0 hub. These settings should be controlled with care, as the default configuration has been tested thoroughly.

The valid settings are:

- 50ns
- 1000ns
- 200ns
- 400ns

5.2.17.6 USB 3.0 Over-Current Timer

This setting controls the signal filter on the OCS pin for the USB 3.0 hub. These settings should be controlled with care, as the default configuration has been tested thoroughly.

The valid settings are:

- 750ns
- 10000ns
- 1250ns
- 1500ns

5.2.18 USB2 Port DP/DM Pin Swap

This per-port setting internally swaps the DP and DM signals for the USB 2.0 port.

Port 0 = UFP

Port 1-7 = DFP ports 1-7

5.2.19 USB 2.0 Port HS Output Current

This per-port setting boosts the USB High-Speed driver output.

Port 0 = UFP

Port 1-7 = DFP ports 1-7

Settings are defined within the Protouch tool.

5.2.20 USB 2.0 Port Squelch

This per-port setting modifies the USB input squelch setting.

Port 0 = UFP

Port 1-7 = DFP ports 1-7

Settings are defined within the Protouch tool.

5.2.21 USB 2.0 Hub Advanced Controls

The settings in the following sub-sections are advanced controls, which most applications will not require to be set, since the default configurations allow seamless operation. Only advanced users/applications should override the default configurations detailed here.

5.2.21.1 USB 2.0 HS Disable

This setting disables USB High-Speed operation on the entire USB 2.0 hub.

5.2.21.2 USB 2.0 MTT Disable

This setting disables the Multi-TT operation on the entire USB 2.0 hub.

5.2.21.3 USB 2.0 FS EOP Disable

This setting disables the End Of Packet (EOP) generation of End Of Frame 1 (EOF1) when in Full-Speed mode.

5.2.22 UUID Override

These controls allow the user to override the 128-bit UUID value within the device (set at the Microchip Factory as a unique value for each device). By USB Specification, if multiple devices are connected within one system as a single Compound Device, all UUID (within the BOS descriptor) should be set the same.

5.3 One-Time Programmable (OTP) Memory

The device contains an internal One-Time Programmable memory, which allows various configuration settings to be configured for the end application. This memory requires a configuration to be created through the Microchip ProTouch tool or by a Microchip FAE. The ProTouch tool then allows programming of this block over a USB 2.0 connection to a Microsoft Windows Host.

There is also an option to support OTP programming via the SMBus interface. However, this method of OTP programming is not preferred. Please contact your local Microchip FAE for more information on OTP programming via SMBus.

5.3.1 Configuration File Creation

For information on configuration file creation, refer to the ProTouch tool.

5.4 External SPI

The device supports operation utilizing an external SPI Flash or ROM. In normal operation, the internal microcontroller runs from the internal ROM. If an external SPI memory is implemented, the full Firmware image must be loaded into the SPI.

When using an external SPI memory, there are two options available. The configuration can be loaded from the internal OTP, or the internal OTP can be ignored and the configuration file loaded into the SPI memory.

Please contact your Microchip FAE for more information on how to obtain access to an external SPI memory image and how to support the different configuration options.

For information on SPI interface connections, refer to Section 4.1: *SPI Interface* on page 20.

5.4.1 Configuration File Creation

For information on configuration file creation, refer to the ProTouch tool.

5.5 SMBus Slave Interface

Typical block write and block read protocols are shown in Figure 5.4 and Figure 5.5. SMBus RAM buffer offset accesses are performed using 7-bit slave addressing, a 16-bit SMBus RAM buffer offset field (for legacy and advanced modes, respectively), and an 8-bit data field. The shading shown in the figures during a read or write indicates the hub is driving data on the **SM_DAT** line; otherwise, host data is on the **SM_DAT** line.

The SMBus slave address assigned to the hub (0101100b or 0101101b) allows it to be identified on the SMBus. The SMBus RAM buffer offset field is the internal offset in SMBus RAM to be accessed. The data field is the data that the host is attempting to read/write from/to the SMBus RAM buffer.

Note: Data bytes are transferred MSB first.

For information on connecting the SMBus slave interface to a host, refer to Section 4.2: *SMBus Slave Interface* on page 25.

5.5.1 Block Write

The block write begins with a slave address and a write condition. After the command code, the host issues a byte count which describes how many more bytes will follow in the message. If a slave had 20 bytes to send, the first byte would be the number 20 (14h), followed by the 20 bytes of data. The byte count may not be zero. A block write or read allows a transfer maximum of 32 data bytes.

Note: For the following SMBus tables:

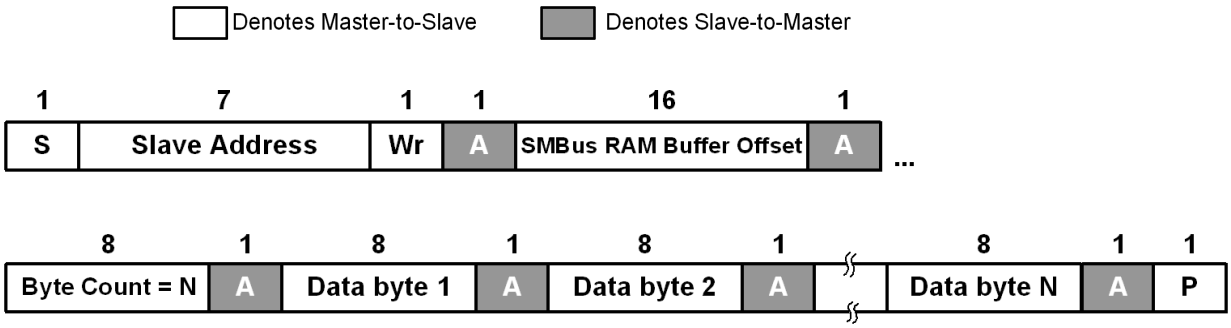

Figure 5.4 Block Write

5.5.2 Block Read

A block read differs from a block write in that the repeated start condition exists to satisfy the I^2C specification's requirement for a change in the transfer direction.

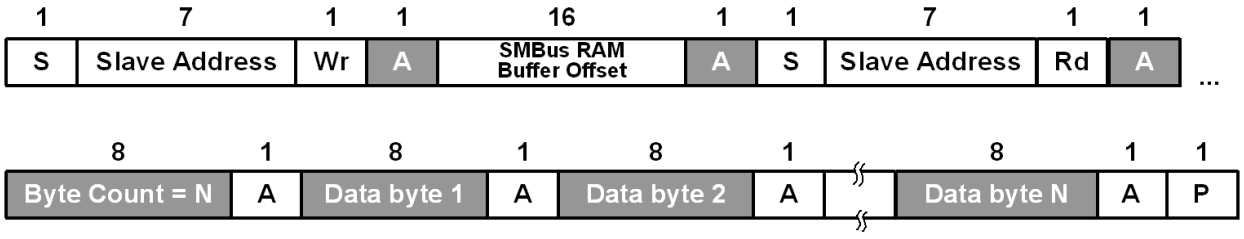

Figure 5.5 Block Read

5.5.3 Standard SMBus Commands

There are special commands that can be sent in the place of the 16-bit address bytes. These commands are used to enumerate the hub, access the configuration registers, or simply reset the device. The commands consist of the 16-bit command followed by a 00h byte to terminate the command.

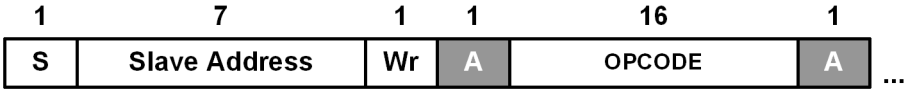

Figure 5.6 SMBus Commands

Table 5.1 Special SMBus Commands

OPERATION	OPCODE	DESCRIPTION
Reboot	9936h	Reboot internal MCU.
Configuration Register Access	9937h	Read and Write Configuration Registers
Extended Command	993Eh	Execute Extended Status Commands
USB Attach	AA55h	Enter Configuration Stage
USB Attach with SMBus Access	AA56h	Enter Configuration Stage with SMBus Access Enabled

5.5.4 Special Hub Commands

Below is a list of the extended commands and the code used to execute them.

Table 5.2 Extended Commands

COMMAND	CODE
Set Address	00h
Get Default Address	01h
Get Hub Info	02h
Get UCS Port Mask	03h
Port Connect Status	80h
Port Power Status	81h
Port Force Disable	82h
Port DP/DM Status	83h
UCS Byte Read	84h
UCS Byte Write	85h
UCS Block Read	86h
UCS Block Write	87h

The extended commands provide access to the status of the device. From these registers a SMBus controller can see the connection status of the hub, communicate with the UCS1000, and change the SMBus address if desired. When the extended command is sent the hub will interpret the memory starting at offset 00h as follows:

Table 5.3 Memory Format for Extended Hub Command

RAM Address	Description	Notes
0000h	Command	Code of the extended command to execute.
0001h	Status	Always write 0 to this register, it will be updated after the command is executed with the status.
0002h	Data1	The first byte of data to write to or read from when executing the command.
...	...	...
0004h+N	DataN	The Nth byte of data to write to or read from when executing the command.

5.5.4.1 Special Command Example

The following example shows how to read the Charger Detection register to find out what type of charger the hub has connected to:

1. First write data to the memory of the hub.

Table 5.4 Example SMBus Write Command

BYTE	VALUE	COMMENT
0	5Ah	Address plus write bit.
1	00h	Memory address **00**00h.
2	00h	Memory address 00**00**h.
3	03h	Number of bytes to write to memory.
4	80h	Get Port Device Status.
5	00h	Reading one data bytes.
6	1Fh	Read all ports.

2. After the data is written, execute the Configuration Register Access command.

Table 5.5 Configuration Register Access Command

BYTE	VALUE	COMMENT
0	5Ah	Address plus write bit.
1	99h	Command **99**3Eh.
2	3Eh	Command 99**3E**h.
3	00h	Command Completion.

3. Finally, read back data starting at memory offset 04h, which is where the Data byte starts.

Table 5.6 Example SMBus Read Command

BYTE	VALUE	COMMENTS
0	5Ah	Address plus Write bit.
1	00h	Memory Address **00**04h.
2	03h	Memory Address 00**04**h.
0	59h	Address plus Read bit.
1	80h	Device sends 128 bytes of data.
2	03h	Upstream Connection Status. (SS and HS)
3	02h	Port 1 Connection Status. (HS/FS/LS Only)
4	01h	Port 2 Connection Status. (SS Only)
5	02h	Port 3 Connection Status.(HS/FS/LS Only)

Although the device can send out 128 bytes of memory data, it isn't necessary to read the entire set, the SMBus Master can send a stop at any time.

5.5.4.2 Set Address (00h)

The set address command will change the SMBus address to the value in Data1 or memory address 0002h. The next SMBus read will have to account for this change in address.

Table 5.7 Set Address Byte

SET ADDR (0x00)			SMBUS ADDRESS
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	DEFAULT	W	Resets to the default SMBus address.
7:0	ADDRESS	W	New SMBus Address

5.5.4.3 Get Default Address (01h)

This command will always return the default address of the USB5x3xB (2dh).

5.5.4.4 Get Hub Info (02h)

The command will return the status of the hub in Data1. The status byte follows the following format:

Table 5.8 Hub Information

USB2_HUB_INFO (0x02)			USB2 HUB INFORMATION
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	CONFIGURED	R	1 = Hub is in the configured state. 2 = Hub is in the unconfigured state.
6:0	USB2_ADDRESS	R	The address of the USB2 hub.

5.5.4.5 Get UCS Port Mask(03h)

This will return a mask of which port is assigned a UCS port controller based on the UCS device detection.

5.5.4.6 Port Connect Status (80h)

Data1 of the memory is written by the SMBus master and after the command is executed Data 2-6 will be populated with the status of each port.

Data1 is a port mask where each bit represents the port status to return. Bit 0 is the upstream port, bit 1 is the downstream port 1, etc.

The port connect status byte can be interpreted as follows:

Table 5.9 Hub Information

PORT_CONNECT (0x80)			PORT CONNECT STATUS
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:6	Reserved	R	Reserved
5	USB2_SUSPEND	R	0 = Port is not suspended. 1 = Port is in the L2 Suspend State.
4	USB3_SUSPEND	R	0 = Port is not suspended. 1 = Port is in the U3 Suspend State.
3:2	Reserved	R	Reserved
1	USB2_CONNECT	R	0 = No USB2 connection detected. (HS/FS/LS) 1 = USB2 connection detected.
0	USB3_CONNECT	R	0 = No USB3 connection detected. 1 = USB3 connection detected.

5.5.4.7 Port Power Status (81h)

Data1 of the memory is written by the SMBus master and after the command is executed Data 2-6 will be populated with the status of each port. A ‘1’ means the port power is enabled, a ‘0’ means the port power is disabled.

Data1 is a port mask where each bit represents the port status to return. Bit 0 is the upstream port, bit 1 is the downstream port 1, etc

5.5.4.8 Port Force Disable (82h)

Data1 of the memory is the port mask and Data 2-6 is the port disable state requested.

Data1 is a port mask where each bit represents the port status to return. Bit 0 is the upstream port, bit 1 is the downstream port 1, etc.

The port disable byte will be interpreted as follows:

Table 5.10 Hub Information

PORT_DISABLE (0x82)			**PORT DISABLE**
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	OVERWRITE	W	If this bit is 1 then the data in bits 2:0 will be overwritten.
6:3	Reserved	W	Reserved
2	FORCE_OFF	W	0 = Port Power controlled by hub. 1 = Port Power forced off.
1	USB3_TERM_DIS	W	0 = USB3 Terminations controlled by hub. 1 = USB3 Terminations disabled.
0	USB2_TERM_DIS	W	0 = USB2 Terminations controlled by hub. 1 = USB2 Terminations disabled.

5.5.4.9 Port DP/DM Status (83h)

Data1 of the memory is written by the SMBus master and after the command is executed Data 2-6 will be populated with the status of each port.

Data1 is a port mask where each bit represents the port status to return. Bit 0 is the upstream port, bit 1 is the downstream port 1, etc.

The port DP/DM status byte can be interpreted as follows:

Table 5.11 Port DP/DM Status

PORT_DPDM (0x83)			PORT DP/DM STATUS
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:2	Reserved	W	Reserved
1	FS_DM	W	0 = DM line is below the FS threshold. 1 = DM line is above the FS threshold (LS idle state)
0	FS_DP	W	0 = DP line is below the FS threshold. 1 = DP line is above the FS threshold. (FS idle state)

5.5.4.10 UCS Byte Read (84h)

The first data byte (Data1) contains the address of the UCS register to read. The second data byte (Data2) will contain the data after the command is executed.

5.5.4.11 UCS Byte Write (85h)

The first data byte (Data1) contains the address of the UCS register to write to. The second data byte (Data2) contains the data to be written.

5.5.4.12 UCS Block Read (86h)

The first data byte (Data1) contains the address of the UCS register to read. The second data byte (Data2) contains the number of bytes to read. The subsequent data bytes will be populated with the contents of the Data2 registers starting at Data1.

5.5.4.13 UCS Block Write (87h)

The first data byte (Data1) contains the address of the UCS register to write to. The second data byte (Data2) contains the number of bytes to write. The subsequent data bytes contain the data to write.

5.6 Runtime Register Definitions

Below is the list of configuration registers and their address. The INIT column contains the values that will be loaded when the USB Attach commands are sent. Register definitions are provided in the subsequent sub-sections. For information on accessing these registers, refer to Section 5.6.1: *Accessing Runtime Registers* on page 46.

Configuration Register Memory Map

ADDR	R/W	NAME	FUNCTION	INIT
0806h	R/W	LED0_PIO0_CTL1	LED0/PIO0 Register 1	00h
0807h	R/W	LED0_PIO0_CTL2	LED0/PIO0 Register 2	00h
0808h	R/W	LED1_PIO1_CTL1	LED1/PIO1 Register 1	00h
0809h	R/W	LED1_PIO1_CTL2	LED1/PIO1 Register 2	00h
082Dh	R/W	VBUS_OCS_PD	VBUS and OCS Pull-down Register	00h
082Fh	R/W	LED0_PD	LED0 Pull-down Register	00h
0831h	R/W	VBUS_OCS_DIR	VBUS and OCS Direction Register	00h
0833h	R/W	LED0_DIR	LED0 Direction Register	00h
0835h	R/W	VBUS_OCS_OUT	VBUS and OCS Output Register	00h
0837h	R/W	LED0_OUT	LED0 Output Register	00h
0839h	R/W	VBUS_OCS_IN	VBUS and OCS Input Register	Note 5.1
083Bh	R/W	LED0_IN	LED0 Input Register	Note 5.1
083Dh	R/W	VBUS_OCS_PU	VBUS and OCS Pull-up Resistor Register	FEh
083Fh	R/W	LED0_PU	LED0 Pull-up Resistor Register	00h
092Eh	R/W	PRT_PWR_PD	Port Power Pull-down Resistor Register	00h
0932h	R/W	PRT_PWR_DIR	Port Power Direction Register	00h
0936h	R/W	PRT_PWR_OUT	Port Power Output Register	00h
093Ah	R/W	PRT_PWR_IN	Port Power Input Register	Note 5.1
093Eh	R/W	PRT_PWR_PU	Port Power Pull-up Resistor Register	00h
3C00h	R/W	PRT_PWR_SEL1	Port 1 Power Select Register	03h
3C04h	R/W	PRT_PWR_SEL2	Port 2 Power Select Register	03h
3C08h	R/W	PRT_PWR_SEL3	Port 3 Power Select Register	03h
3C20h	R/W	OCS_CFG_SEL1	Port 1 OCS Select Register	01h
3C24h	R/W	OCS_CFG_SEL2	Port 2 OCS Select Register	01h
3C28h	R/W	OCS_CFG_SEL3	Port 3 OCS Select Register	01h
5246h	R/W	CDP_DETECT	Charging Downstream Detected Register	Note 5.1

525Ah	R/W	OSC_GANG	OCS Gang Control Register	00h
525Bh	R/W	OCS_GANG_GPIO	OCS Gang Signal Select Register	00h
60CAh	R/W	HS_UP_BOOST	USB Upstream Boost Register	00h
60CCh	R/W	HS_UP_SENSE	USB Upstream VariSense Register	00h
61C0h	R/W	SS_UP_STATE	USB3 Upstream Link State Register	Note 5.1
64CAh	R/W	HS_P1_BOOST	USB Port 1 Boost Register	00h
64CCh	R/W	HS_P1_SENSE	USB Port 1 VariSense Register	00h
65C0h	R/W	SS_P1_STATE	USB3 Port 1 Link State	Note 5.1
68CAh	R/W	HS_P2_BOOST	USB Port 2 Boost Register	00h
68CCh	R/W	HS_P2_SENSE	USB Port 2 VariSense Register	00h
69C0h	R/W	SS_P2_STATE	USB3 Port 2 Link State	Note 5.1
6CCAh	R/W	HS_P3_BOOST	USB Port 3 Boost Register	00h
6CCCh	R/W	HS_P3_SENSE	USB Port 3 Varisense Register	00h
6DC0h	R/W	SS_P3_STATE	USB3 Port 3 Link State	Note 5.1

Note 5.1 Status registers do not have a default value because the status can change depending on system conditions.

5.6.1 Accessing Runtime Registers

The Configuration Register Access operation allows the SMBus Master to read or write to the internal registers of the hub. When the Configuration Register Access command is sent the hub will interpret the memory starting at offset 00h as follows:

Table 5.12 Memory Format for Configuration Register Access

RAM ADDRESS	DESCRIPTION	NOTES
0000h	Direction	0 = Register Write, 1 = Register Read.
0001h	Data Length	Number of bytes to Read/Write when executing the command.
0002h	Configuration Address MSB	The upper byte of the 16-bit configuration register address.
0003h	Configuration Address LSB	The lower byte of the 16-bit configuration register address.
0004h	Data1	The first byte of data to write to or read from the Configuration Address.
...	...	...
0004h+N	DataN	The Nth byte of data to write to or read from the Configuration Address, N is equal to the Data Length.

5.6.1.1 Configuration Register Write Example

The following example shows how the SMBus messages will be formatted to set the VID of the hub to a custom value, AA55h.

1. Write data to the memory of the hub:

Table 5.13 Example SMBus Write Command

BYTE	VALUE	COMMENT
0	5Ah	Address plus write bit.
1	00h	Memory address **00**00h.
2	00h	Memory address 00**00**h.
3	06h	Number of bytes to write to memory.
4	00h	Write Configuration Register.
5	02h	Writing two data bytes.
6	30h	VID is in register **30**00h.
7	00h	VID is in register 30**00**h.
8	55h	LSB of Vendor ID AA**55**h.
9	AAh	MSB of Vendor ID **AA**55h.

2. Execute the Configuration Register Access command:

Table 5.14 Configuration Register Access Command

BYTE	VALUE	COMMENT
0	5Ah	Address plus write bit.
1	99h	Command **99**37h.
2	37h	Command 99**37**h.
3	00h	Command Completion.

5.6.1.2 Configuration Register Read Example

The following example shows how to read the Charger Detection register to find out what type of charger the hub has connected to:

1. Write data to the memory of the hub.

Table 5.15 Example SMBus Write Command

BYTE	VALUE	COMMENT
0	5Ah	Address plus write bit.
1	00h	Memory address **00**00h.
2	00h	Memory address 00**00**h.
3	04h	Number of bytes to write to memory.
4	01h	Read Configuration Register.
5	01h	Reading one data bytes.
6	30h	BC Detect is in register **30**E2h.
7	E2h	BC Detect is in register 30**E2**h.

2. Execute the Configuration Register Access command.

Table 5.16 Configuration Register Access Command

BYTE	VALUE	COMMENT
0	5Ah	Address plus write bit.
1	99h	Command **99**37h.
2	37h	Command 99**37**h.
3	00h	Command Completion.

3. Read back data starting at memory offset 04h, which is where the Data byte starts.

Table 5.17 Example SMBus Read Command

BYTE	VALUE	COMMENTS
0	5Ah	Address plus Write bit.
1	00h	Memory Address **00**04h.
2	04h	Memory Address 00**04**h.
3	59h	Address plus Read bit.
4	80h	Device sends 128 bytes of data.
5	56h	Charging Downstream Port Detected.

Although the device can send out 128 bytes of memory data, it isn't necessary to read the entire set, the SMBus Master can send a stop at any time.

5.6.2 LED0/PIO0 Register 1

Table 5.18 LED0/PIO0 Register 1

LED0_CTL1 (0x0806)			**LED0_PIO0 CONTROL REGISTER**
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	XNOR	R/W	This bit toggles the polarity of the LED output. It can be used to invert the polarity.
6	MODE	R/W	0 - Blink the LED. 1 - Breath the LED.
5:0	RATE	R/W	In Blink mode: This is the Blink Rate of LED in 50 ms increments. Duty cycle of 50%. Rate range is 50 ms to 3.15 seconds. In Breath mode: This is the time for an active breadth in 500 ms increments.

5.6.3 LED0/PIO0 Register 2

Table 5.19 LED0/PIO0 Register 2

LED0_CTL2 (0x0807)			**LED0_PIO0 CONTROL REGISTER 2**
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:2	TRAILOFF_TIME	R/W	In Blink mode: Time the LED must continue blinking after LED_ON is turned off. TRAIL_TIME is in 50ms increments. Range is 50 ms to 3.15 seconds. In Breath mode: This is the time for an sleeping in between breadths in 500 ms increments
1	LED_ON	R/W	If LED_ON is set, then start blinking or breathing this LED. Blink timer starts when this bit is enabled. No short blinks permitted. When this bit is disabled, blinking stops when TRAIL_TIME expires. In Breath Mode: Breath timer starts when this bit is enabled. No short blinks permitted. When this bit is disabled, blinking stops immediately.
0	LED_PIO	R/W	‘0’ = PIO0 ‘1’ = LED0

5.6.4 LED1/PIO1 Register 1

Table 5.20 LED1/PIO1 Register 1

LED1_CTL1 (0x0808)			**LED1_PIO1 CONTROL REGISTER**
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	XNOR	R/W	This bit toggles the polarity of the LED output. It can be used to invert the polarity.
6	MODE	R/W	0 - Blink the LED. 1 - Breath the LED.
5:0	RATE	R/W	In Blink mode: This is the Blink Rate of LED in 50 ms increments. Duty cycle of 50%. Rate range is 50 ms to 3.15 seconds. In Breath mode: This is the time for an active breadth in 500 ms increments.

5.6.5 LED1/PIO1 Register 2

Table 5.21 LED1/PIO1 Register 2

LED1_CTL2 (0x0809)			LED1_PIO1 CONTROL REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:2	TRAILOFF_TIME	R/W	In Blink mode: Time the LED must continue blinking after LED_ON is turned off. TRAIL_TIME is in 50ms increments. Range is 50 ms to 3.15 seconds. In Breath mode: This is the time for an sleeping in between breadths in 500 ms increments.
1	LED_ON	R/W	If LED_ON is set, then start blinking or breathing this LED. Blink timer starts when this bit is enabled. No short blinks permitted. When this bit is disabled, blinking stops when TRAIL_TIME expires. In Breath Mode: Breath timer starts when this bit is enabled. No short blinks permitted. When this bit is disabled, blinking stops immediately.
0	LED_GPIO	R/W	‘0’ = PIO1 ‘1’ = LED1

5.6.6 VBUS and OCS Pull-Down Register

Table 5.22 VBUS and OCS Pull-down Register

VBUS_OCS_PD (0x082D)			VBUS AND OCS PULL DOWN REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:5	Reserved	R/W	Reserved
4	OCS4	R/W	“0” = Disables the pull-down resistor on the OCS4 pin. “1” = Enables the pull-down resistor on the OCS4 pin.
3	OCS3	R/W	“0” = Disables the pull-down resistor on the OCS3 pin. “1” = Enables the pull-down resistor on the OCS3 pin.
2	OCS2	R/W	“0” = Disables the pull-down resistor on the OCS2 pin. “1” = Enables the pull-down resistor on the OCS2 pin.
1	OCS1	R/W	“0” = Disables the pull-down resistor on the OCS1 pin. “1” = Enables the pull-down resistor on the OCS1 pin.
0	VBUS	R/W	“0” = Disables the pull-down resistor on the VBUS pin. “1” = Enables the pull-down resistor on the VBUS pin.

5.6.7 LED0 Pull-Down Register

Table 5.23 LED0 Pull-down Register

LED0_PD (0x082F)			LED0 PULL DOWN REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:1	Reserved	R/W	Reserved.
0	LED0	R/W	“0” = Disables the pull-down resistor on the LED0 pin. “1” = Enables the pull-down resistor on the LED0 pin.

5.6.8 VBUS and OCS Direction Register

Table 5.24 VBUS and OCS Direction Register

VBUS_OCS_DIR (0x0831)			VBUS AND OCS DIRECTION REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:5	Reserved	R/W	Reserved
4	OCS4	R/W	Direction: 0 = In, 1 = Out.
3	OCS3	R/W	Direction: 0 = In, 1 = Out.
2	OCS2	R/W	Direction: 0 = In, 1 = Out.
1	OCS1	R/W	Direction: 0 = In, 1 = Out.
0	VBUS	R/W	Direction: 0 = In, 1 = Out.

5.6.9 LED0 Direction Register

Table 5.25 LED0 Direction Register

LED0_DIR (0x0833)			LED0 DIRECTION REGISTER 1
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:1	Reserved	R/W	Reserved
0	LED0	R/W	Direction: 0 = In, 1 = Out.

5.6.10 VBUS and OCS Output Register

Table 5.26 VBUS and OCS Output Register

VBUS_OCS_OUT (0x0835)			VBUS AND OCS REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:5	Reserved	R/W	Reserved
4	OCS4	R/W	Output Buffer Data.
3	OCS3	R/W	Output Buffer Data.
2	OCS2	R/W	Output Buffer Data.
1	OCS1	R/W	Output Buffer Data.
0	VBUS	R/W	Output Buffer Data.

5.6.11 LED0 Output Register

Table 5.27 LED0 Output Register

LED0_OUT (0x0837)			LED0 OUTPUT REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:1	Reserved	R/W	Reserved
0	LED0	R/W	PIO0 Output Buffer Data. This bit has no meaning if PIO0 is in LED mode.

5.6.12 VBUS and OCS Input Register

Table 5.28 VBUS and OCS Input Register

VBUS_OCS_IN (0x0839)			VBUS AND OCS INPUT REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:5	Reserved	R	Reserved
4	OCS4	R	Input Buffer Data.
3	OCS3	R	Input Buffer Data.
2	OCS2	R	Input Buffer Data.
1	OCS1	R	Input Buffer Data.
0	VBUS	R	Input Buffer Data.

5.6.13 LED0 Input Register

Table 5.29 LED0 Input Register

LED0_IN (0x083B)			LED0 INPUT REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:1	Reserved	R	Reserved
0	LED0	R	PIO0 Input Buffer Data. This bit is not valid if PIO0 is in LED mode.

5.6.14 VBUS and OCS Pull-Up Resistor Register

Table 5.30 VBUS and OCS Pull-up Resistor Register

VBUS_OCS_PU (0x083D)			VBUS AND OCS PULL UP REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:5	Reserved	R/W	Reserved
4	OCS4	R/W	“0” = Disables the pull-up resistor on the OCS4 pin. “1” = Enables the pull-up resistor on the OCS4 pin.
3	OCS3	R/W	“0” = Disables the pull-up resistor on the OCS3 pin. “1” = Enables the pull-up resistor on the OCS3 pin.
2	OCS2	R/W	“0” = Disables the pull-up resistor on the OCS2 pin. “1” = Enables the pull-up resistor on the OCS2 pin.
1	OCS1	R/W	“0” = Disables the pull-up resistor on the OCS1 pin. “1” = Enables the pull-up resistor on the OCS1 pin.
0	VBUS	R/W	“0” = Disables the pull-up resistor on the VBUS pin. “1” = Enables the pull-up resistor on the VBUS pin.

5.6.15 LED0 Pull-Up Resistor Register

Table 5.31 LED0 Pull-up Resistor Register

LED0_PU (0x083F)			LED0 PULL UP REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:1	Reserved	R/W	Reserved
0	LED0	R/W	“0” = Disables the pull-up resistor on the LED0 pin. “1” = Enables the pull-up resistor on the LED0 pin.

5.6.16 Port Power Pull-Down Resistor Register

Table 5.32 Port Power Pull-down Resistor Register

PRT_PWR_PD (0x092E)			PORT POWER PULL DOWN REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:1	PRT_PWR_PD[7:1]	R/W	“0” = Disables the pull-down resistor on the PRT_PWR[N] pad. Where N is the bit being controlled. Bit 1 controls PRT_PWR 1 and so on. “1” = Enables the pull-down resistor on the PRT_PWR[N] pad.
0	Reserved	R/W	Reserved

5.6.17 Port Power Direction Register

Table 5.33 Port Power Direction Register

PRT_PWR_DIR (0x0932)			Port Power DIRECTION REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:1	PRT_PWR_D[7:1]	R/W	PRT_PWR[7:1] Direction: 0 = In, 1 = Out.
0	Reserved	R/W	Reserved

5.6.18 Port Power Output Register

Table 5.34 Port Power Output Register

PRT_PWR_OUT (0x0936)			Port Power OUTPUT REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:1	PRT_PWR_O[7:1]	R/W	PRT_PWR[7:1] Output Buffer Data.
0	Reserved	R/W	Reserved

5.6.19 Port Power Input Register

Table 5.35 Port Power Input Register

PRT_PWR_IN (0x093A)			Port Power INPUT REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:1	PRT_PWR[7:1]	R	PRT[7:1] Input Buffer Data.
0	Reserved	R	Reserved

5.6.20 Port Power Pull-Up Resistor Register

Table 5.36 Port Power Pull-up Resistor Register

PRT_PWR_PU (0x093E)			Port Power PULL UP REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:1	PRT_PWR_PU[7:1]	R/W	“0” = Disables the pull-up resistor on the PRT_PWR[N] pad. Where N is the bit being controlled. Bit 1 controls PRT_PWR 1 and so on. “1” = Enables the pull-up resistor on the PIO pad.
0	Reserved	R	Reserved

5.6.21 Port 1 Power Select Register

The bits in this register are configured via a configuration file. Users must not change the values of these settings dynamically.

Table 5.37 Port 1 Power Select Register

PRT_PWR_SEL1 (0x3C00)			**PORT 1 POWER SELECT**
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	COMBINED_MODE	R/W	0 - The Port Power and over-current sense use separate pins. 1 - The Port Power and over-current sense use the same pins.
6	Reserved	R	Reserved
5	DISABLED	R/W	When set this disables the port. Used to inform the hub a port is permanently disabled.
4	NR_DEVICE	R/W	When set indicates this port has a permanently attached device.
3:0	PRT_SEL	R/W	This selects the source for the port power for port1 0000b - Port Power is disabled for this Port. 0001b - Port is on if USB2 port power is on 0010b - Port is on if USB3 port power is on 0011b - Port is on if USB2 or USB3 port power is on 0100b - Port is on if designated GPIO is on All other values are reserved.

Note: The port disable, port non-removable and combined mode bits must be set through a configuration file to ensure functionality when the part enumerates.

5.6.22 Port 2 Power Select Register

The bits in this register are configured via a configuration file. Users must not change the values of these settings dynamically.

Table 5.38 Port 2 Power Select Register

PRT_PWR_SEL2 (0x3C04)			PORT 2 POWER SELECT
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	COMBINED_MODE	R/W	0 - The Port Power and over-current sense use separate pins. 1 - The Port Power and over-current sense use the same pins.
6	Reserved	R	Reserved
5	DISABLED	R/W	When set this disables the port. Used to inform the hub a port is permanently disabled.
4	NR_DEVICE	R/W	When set indicates this port has a permanently attached device.
3:0	PRT_SEL	R/W	This selects the source for the port power for port1 0000b - Port Power is disabled for this Port. 0001b - Port is on if USB2 port power is on 0010b - Port is on if USB3 port power is on 0011b - Port is on if USB2 or USB3 port power is on 0100b - Port is on if designated GPIO is on All other values are reserved.

Note: The port disable, port non-removable and combined mode bits must be set through a configuration file to ensure functionality when the part enumerates.

5.6.23 Port 3 Power Select Register

The bits in this register are configured via a configuration file. Users must not change the values of these settings dynamically.

Table 5.39 Port 3 Power Select Register

PRT_PWR_SEL3 (0x3C08)			PORT 3 POWER SELECT
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	COMBINED_MODE	R/W	0 - The Port Power and over-current sense use separate pins. 1 - The Port Power and over-current sense use the same pins.
6	Reserved	R	Reserved
5	DISABLED	R/W	When set this disables the port. Used to inform the hub a port is permanently disabled.
4	NR_DEVICE	R/W	When set indicates this port has a permanently attached device.
3:0	PRT_SEL	R/W	This selects the source for the port power for port1 0000b - Port Power is disabled for this Port. 0001b - Port is on if USB2 port power is on 0010b - Port is on if USB3 port power is on 0011b - Port is on if USB2 or USB3 port power is on 0100b - Port is on if designated GPIO is on All other values are reserved.

Note: The port disable, port non-removable and combined mode bits must be set through a configuration file to ensure functionality when the part enumerates.

5.6.24 Port 1 OCS Select Register

The bits in this register are configured via a configuration file. Users must not change the values of these settings dynamically.

Table 5.40 Port 1 OCS Select Register

OCS_CFG_SEL1 (0x3C20)			PORT 1 OCS SELECT
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	Reserved	R/W	Reserved.
3:0	OCS_SEL	R/W	This selects the source for the port power for port1 0000b - The port is disabled 0001b - OCS comes from OCS pin 0010b - OCS comes from GPIO 1111b - OCS is force on (for testing) All other values are reserved.

5.6.25 Port 2 OCS Select Register

The bits in this register are configured via a configuration file. Users must not change the values of these settings dynamically.

Table 5.41 Port 2 OCS Select Register

OCS_CFG_SEL2 (0x3C24)			PORT 2 OCS SELECT
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	Reserved	R/W	Reserved.
3:0	OCS_SEL	R/W	This selects the source for the port power for port1 0000b - The port is disabled 0001b - OCS comes from OCS pin 0010b - OCS comes from GPIO 1111b - OCS is force on (for testing) All other values are reserved.

5.6.26 Port 3 OCS Select Register

The bits in this register are configured via a configuration file. Users must not change the values of these settings dynamically.

Table 5.42 Port 3 OCS Select Register

OCS_CFG_SEL3 (0x3C28)			**PORT 3 OCS SELECT**
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	Reserved	R/W	Reserved.
3:0	OCS_SEL	R/W	This selects the source for the port power for port1 0000b - The port is disabled 0001b - OCS comes from OCS pin 0010b - OCS comes from GPIO 1111b - OCS is force on (for testing) All other values are reserved.

5.6.27 Charging Downstream Detected Register

Table 5.43 Charging Downstream Detected Register

CDP_DETECT (0x5246)			CHARGING DOWNSTREAM DETECTED
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R/W	Reserved
2	P3_CDP	R/W	0 = No CDP handshake detected. 1 = Charging Downstream Port handshake detected prior to enumeration.
1	P2_CDP	R/W	0 = No CDP handshake detected. 1 = Charging Downstream Port handshake detected prior to enumeration.
0	P1_CDP	R/W	0 = No CDP handshake detected. 1 = Charging Downstream Port handshake detected prior to enumeration.

5.6.28 OCS Gang Control Register

Table 5.44 OCS Gang Control Register

OCS_GANG (0x525A)			**OCS GANG CONTROL**
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	Reserved	R/W	Reserved
3	P3_OCS_GANG	R/W	Setting this bit to 1 will cause this ports OCS status to be ganged to the selected pin.
2	P2_OCS_GANG	R/W	Setting this bit to 1 will cause this ports OCS status to be ganged to the selected pin.
1	P1_OCS_GANG	R/W	Setting this bit to 1 will cause this ports OCS status to be ganged to the selected pin.
0	Reserved	R/W	Reserved

5.6.29 OCS Gang Signal Select Register

Table 5.45 OCS Gang Signal Select Register

OCS_GANG_GPIO (0x525B)			**OCS GANG CONTROL**
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:6	RESERVED	R/W	Reserved
5:0	GANGED_OCS_ SIGNAL	R/W	Only the following configurations are valid settings: 0 = TRST 1 = OCS1 3 = OCS2 4 = SPI_CLK 5 = SPI_DO 6 = OCS3 7 = OCS4 8 = PRTCTL1 9 = PRTCTL2 10 = PRTCTL3 15 = SM_CLK

5.6.30 USB Upstream Boost Register

Table 5.46 USB Upstream Boost Register

HS_UP_BOOST (0x60CA)			USB UPSTREAM BOOST REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R/W	Reserved
2:0	HS_BOOST	R/W	HS Output Current. 3’b000: Nominal 3’b001: Decrease by 5% 3’b010: Increase by 10% 3’b011: Increase by 5% 3’b100: Increase by 20% 3’b101: Increase by 15% 3’b110: Increase by 30% 3’b111: Increase by 25%

5.6.31 USB Upstream VariSense Register

Table 5.47 USB Upstream VariSense Register

PHY_UP_SENSE (0x60CC)			USB UPSTREAM VARISENSE REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R	Reserved
2:0	HS_SQ_TUNE[2:0]	R/W	Squelch Tune 3’b000: Nominal 100mV Trip Point 3’b001: Decrease by 12.5mV 3’b010: Decrease by 25mV 3’b011: Decrease by 37.5mV 3’b100: Decrease by 50mV 3’b101: Decrease by 62.5mV 3’b110: Increase by 25mV 3’b111: Increase by 12.5mV

5.6.32 USB3 Upstream Link State Register

Table 5.48 USB3 Upstream Link State Register

SS_UP_STATE (0x61C0)			USB3 UPSTREAM LINK STATE
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	LINK_STATE	R	Refer to Table 5.58, "USB 3.0 Link States" for more details.
3	Reserved	R	Reserved
2:0	LINK_SUB_STATE	R	Refer to Table 5.58, "USB 3.0 Link States" for more details.

5.6.33 USB Port 1 Boost Register

Table 5.49 USB Port 1 Boost Register

HS_P1_BOOST (0x64CA)			USB PORT 1 BOOST REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R/W	Reserved
2:0	HS_BOOST	R/W	HS Output Current. 3’b000: Nominal 3’b001: Decrease by 5% 3’b010: Increase by 10% 3’b011: Increase by 5% 3’b100: Increase by 20% 3’b101: Increase by 15% 3’b110: Increase by 30% 3’b111: Increase by 25%

5.6.34 USB Port 1 VariSense Register

Table 5.50 USB Port 1 VariSense Register

PHY_P1_SENSE (0x64CC)			USB PORT 1 VARISENSE REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R	Reserved
2:0	HS_SQ_TUNE[2:0]	R/W	Squelch Tune 3’b000: Nominal 100mV Trip Point 3’b001: Decrease by 12.5mV 3’b010: Decrease by 25mV 3’b011: Decrease by 37.5mV 3’b100: Decrease by 50mV 3’b101: Decrease by 62.5mV 3’b110: Increase by 25mV 3’b111: Increase by 12.5mV

5.6.35 USB3 Port 1 Link State

Table 5.51 USB3 Port 1 Link State

SS_P1_STATE (0x65C0)			USB3 PORT1 LINK STATE
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	LINK_STATE	R	Refer to Table 5.58, "USB 3.0 Link States" for more details.
3	Reserved	R	Reserved
2:0	LINK_SUB_STATE	R	Refer to Table 5.58, "USB 3.0 Link States" for more details.

5.6.36 USB Port 2 Boost Register

Table 5.52 USB Port 2 Boost Register

HS_P2_BOOST (0x68CA)			USB PORT 2 BOOST REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R/W	Reserved
2:0	HS_BOOST	R/W	HS Output Current. 3’b000: Nominal 3’b001: Decrease by 5% 3’b010: Increase by 10% 3’b011: Increase by 5% 3’b100: Increase by 20% 3’b101: Increase by 15% 3’b110: Increase by 30% 3’b111: Increase by 25%

5.6.37 USB Port 2 VariSense Register

Table 5.53 USB Port 2 VariSense Register

PHY_P2_SENSE (0x68CC)			USB PORT 2 VARISENSE REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R	Reserved
2:0	HS_SQ_TUNE[2:0]	R/W	Squelch Tune 3’b000: Nominal 100mV Trip Point 3’b001: Decrease by 12.5mV 3’b010: Decrease by 25mV 3’b011: Decrease by 37.5mV 3’b100: Decrease by 50mV 3’b101: Decrease by 62.5mV 3’b110: Increase by 25mV 3’b111: Increase by 12.5mV

5.6.38 USB3 Port 2 Link State

Table 5.54 USB3 Port 2 Link State

SS_P2_STATE (0x69C0)			USB3 PORT 2 LINK STATE
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	LINK_STATE	R	Refer to Table 5.58, "USB 3.0 Link States" for more details.
3	Reserved	R	Reserved
2:0	LINK_SUB_STATE	R	Refer to Table 5.58, "USB 3.0 Link States" for more details.

5.6.39 USB Port 3 Boost Register

Table 5.55 USB Port 3 Boost Register

HS_P3_BOOST (0x6CCA)			USB PORT 3 BOOST REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R/W	Reserved
2:0	HS_BOOST	R/W	HS Output Current. 3’b000: Nominal 3’b001: Decrease by 5% 3’b010: Increase by 10% 3’b011: Increase by 5% 3’b100: Increase by 20% 3’b101: Increase by 15% 3’b110: Increase by 30% 3’b111: Increase by 25%

5.6.40 USB Port 3 VariSense Register

Table 5.56 USB Port 3 Varisense Register

PHY_P3_SENSE (0x6CCC)			USB PORT 3 VARISENSE REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:3	Reserved	R	Reserved
2:0	HS_SQ_TUNE[2:0]	R/W	Squelch Tune 3’b000: Nominal 100mV Trip Point 3’b001: Decrease by 12.5mV 3’b010: Decrease by 25mV 3’b011: Decrease by 37.5mV 3’b100: Decrease by 50mV 3’b101: Decrease by 62.5mV 3’b110: Increase by 25mV 3’b111: Increase by 12.5mV

5.6.41 USB3 Port 3 Link State

Table 5.57 USB3 Port 3 Link State

SS_P3_STATE (0x6DC0)			USB3 PORT 3 LINK STATE
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:4	LINK_STATE	R	Refer to Table 5.58, "USB 3.0 Link States" for more details.
3	Reserved	R	Reserved
2:0	LINK_SUB_STATE	R	Refer to Table 5.58, "USB 3.0 Link States" for more details.

Table 5.58 USB 3.0 Link States

NUM	LINK STATE
00h	U0
01h	U1
02h	U2
03h	U3
04h	SIS.Disabled
05h	RX.Detect
06h	SS.Inactive
07h	Polling
08h	Recovery
09h	Hot Reset
0Ah	Compliance
0Bh	Loopback

Chapter 6 DC Parameters

6.1 Maximum Guaranteed Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Storage Temperature	T_A	-55	150	°C	
Lead Temperature				°C	Refer to JEDEC Specification J-STD-020D.
1.25 V supply voltage	V_{DD12}	-0.5	1.6	V	
3.3 V supply voltage	V_{DD33}	-0.5	4.0	V	
Voltage on USB+ and USB- pins		-0.5	(3.3 V supply voltage + 2) ≤ 6	V	
Voltage on any signal powered by VDD33 rail		-0.5	V_{DD33} + 0.3	V	
Voltage on any signal pin powered by the VDD12		-0.5	VDD12 + 0.3	V	
HBM ESD Performance			2	kV	
Power Consumption			1.6	W	

Notes:

- Stresses above the specified parameters could cause permanent damage to the device. This is a stress rating only. Therefore, functional operation of the device at any condition above those indicated in the operation sections of this specification are not implied.
- When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.

6.2 Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
USB5533B Operating Temperature	T_A	0	70	°C	
Die Temperature	T_J		115	°C	
1.25 V supply voltage	V_{DD12}	1.22	1.31	V	
3.3 V supply voltage	V_{DD33}	3.0	3.6	V	
1.25 V supply rise time	t_{RT}	0	400	µs	(Figure 6.1)
3.3 V supply rise time	t_{RT}	0	400	µs	(Figure 6.1)
Voltage on USB+ and USB- pins		-0.3	5.5	V	If any 3.3 V supply voltage drops below 3.0 V, then the MAX becomes: (3.3 V supply voltage) + 0.5 ≤ 5.5
Voltage on any signal powered by VDD33 rail		-0.3	V_{DD33}	V	

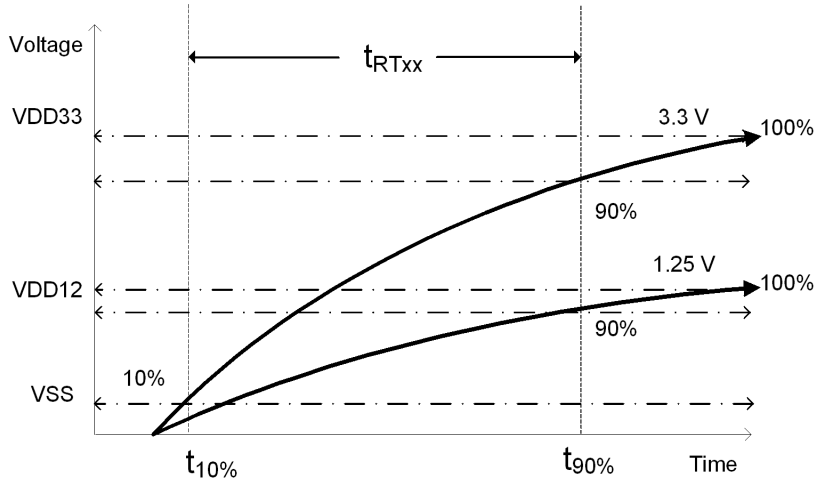

Figure 6.1 Supply Rise Time Model

6.3 Power Consumption

This section details the power consumption of the device as measured during various modes of operation. All typical measurements were taken with power supplies at nominal values (VDD12 = 1.25 V, VDD33 = 3.3 V).

	TYPICAL SUPPLY CURRENT (mA)		TYPICAL POWER (mW)
	VDD33	VDD12	
Reset	0.2	5.0	6.9
No VBUS	5.6	25.0	49.7
Global Suspend (Note 6.1)	1.1	8.3	14.0
3 FS Ports	23	70	163
3 HS Ports	46	78	249
3 SS Ports	18	971	1273
3 SS/HS Ports	56	1029	1471

Note 6.1 The Global Suspend typical supply current and power are stated for device version -6080. Version -5000 has a typical supply current of 9 mA for VDD33, 29 mA for VDD12, and 66 mW of total power consumption.

6.4 DC Electrical Characteristics

Table 6.1 DC Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
IS Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Hysteresis (IS only)	V_{HYSI}		420		mV	
I, IPU, IPD Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
Pull Down	PD		72		µA	V_{IN} = 0
Pull Up	PU		58		µA	V_{IN} = **VDD33**

Table 6.1 DC Electrical Characteristics (continued)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
ICLK Input Buffer						
Low Input Level	V_{ILCK}			0.3	V	
High Input Level	V_{IHCK}	0.8			V	
Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0 to **VDD33**
Input Leakage (All I and IS buffers)						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	µA	V_{IN} = **VDD33**
O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA @ **VDD33** = 3.3 V
High Output Level	V_{OH}	V_{DD33} -0.4			V	I_{OH} = -12 mA @ **VDD33** = 3.3 V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to **VDD33** (Note 6.2)
I/O12, I/O12PU & I/O12PD Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA @ **VDD33** = 3.3 V
High Output Level	V_{OH}	V_{DD33} -0.4			V	I_{OH} = -12 mA @ **VDD33** = 3.3 V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to **VDD33** (Note 6.2)
Pull Down	PD		72		µA	
Pull Up	PU		58		µA	
IO-U (Note 6.3)						

Note 6.2 Output leakage is measured with the current pins in high impedance.

Note 6.3 See *USB 2.0 Specification* [1] for USB DC electrical characteristics.

6.5 Capacitance

Table 6.2 Pin Capacitance

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{XTAL}			2	pF	All pins except USB pins and the pins under the test tied to AC ground
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			10	pF	

Note 6.4 Capacitance T_A = 25°C; fc = 1 MHz; VDD33 = 3.3 V

6.5.1 Package Thermal Specifications

Thermal parameters are measured or estimated for devices with the exposed pad soldered to thermal vias in a multilayer 2S2P PCB per JESD51. Thermal resistance is measured from the die to the ambient air. The values provided are based on the package body, die size, maximum power consumption, 70°C ambient temperature, and 125°C junction temperature of the die.

SYMBOL	USB5533B (°C/W)	VELOCITY (meters/s)
Θ_{JA}	23.0	0
Ψ_{JT}	0.1	0
Θ_{JC}	1.4	0

Table 6.3 Package Thermal Resistance Parameters

Use the following formulas to calculate the junction temperature:

$$T_J = P \times \Theta_{JA} + T_A$$

$$T_J = P \times \Psi_{JT} + T_T$$

$$T_J = P \times \Theta_{JC} + T_C$$

SYMBOL	DESCRIPTION
$\mathbf{T_J}$	Junction temperature
P	Power dissipated
$\mathbf{\Theta_{JA}}$	Junction-to-ambient-temperature
$\mathbf{\Theta_{JC}}$	Junction-to-top-of-package
$\mathbf{\Psi_{JT}}$	Junction-to-bottom-of-case
$\mathbf{T_A}$	Ambient temperature
$\mathbf{T_C}$	Temperature of the bottom of the case
$\mathbf{T_T}$	Temperature of the top of the case

Table 6.4 Package Thermal Legend

Chapter 7 AC Specifications

7.1 Oscillator/Crystal

Crystal: Parallel resonant, fundamental mode, 25 MHz ±30 ppm

External Clock: 50% duty cycle ± 10%, 25 MHz ± 30 ppm, jitter < 100 ps rms

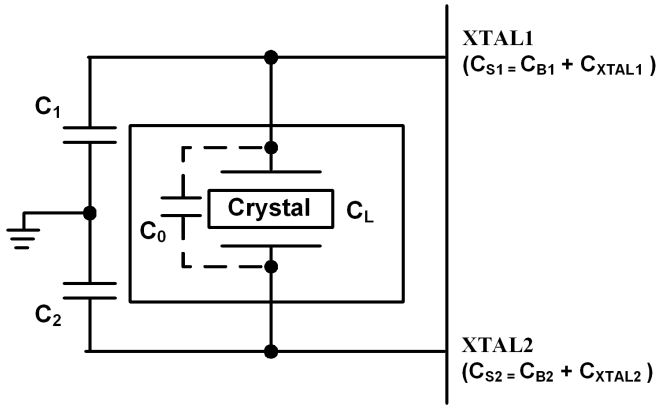

Figure 7.1 Typical Crystal Circuit

Table 7.1 Crystal Circuit Legend

SYMBOL	DESCRIPTION	IN ACCORDANCE WITH
C_0	Crystal shunt capacitance	Crystal manufacturer's specification (Note 7.1)
C_L	Crystal load capacitance	
C_B	Total board or trace capacitance	OEM board design
C_S	Stray capacitance	Microchip IC and OEM board design
C_{XTAL}	XTAL pin input capacitance	Microchip IC
C_1	Load capacitors installed on OEM board	Calculated values based on Figure 7.2 (Note 7.2)
C_2		

$$C_1 = 2 \times (C_L - C_0) - C_{S1}$$

$$C_2 = 2 \times (C_L - C_0) - C_{S2}$$

Figure 7.2 Formula to Find the Value of C_1 and C_2

Note 7.1 C_0 is usually included (subtracted by the crystal manufacturer) in the specification for C_L and should be set to 0 for use in the calculation of the capacitance formulas in Figure 7.2. However, the PCB itself may present a parasitic capacitance between **XTALIN** and **XTALOUT**. For an accurate calculation of C_1 and C_2, take the parasitic capacitance between traces **XTALIN** and **XTALOUT** into account.

Note 7.2 Consult crystal manufacturer documentation for recommended capacitance values.

7.2 External Clock

50% duty cycle ± 10%, 25 MHz ± 30 ppm, jitter < 100 ps rms.

Note: The external clock is based upon 1.2 V CMOS Logic. **XTALOUT** should be treated as a no connect when an external clock is supplied.

7.2.1 SMBus Clock

The maximum frequency allowed on the SMBus clock line is 100 kHz.

7.2.2 USB 2.0

The Microchip hub conforms to all voltage, power, and timing characteristics and specifications as set forth in the *USB 2.0 Specification* [1].

7.3 SPI Timing

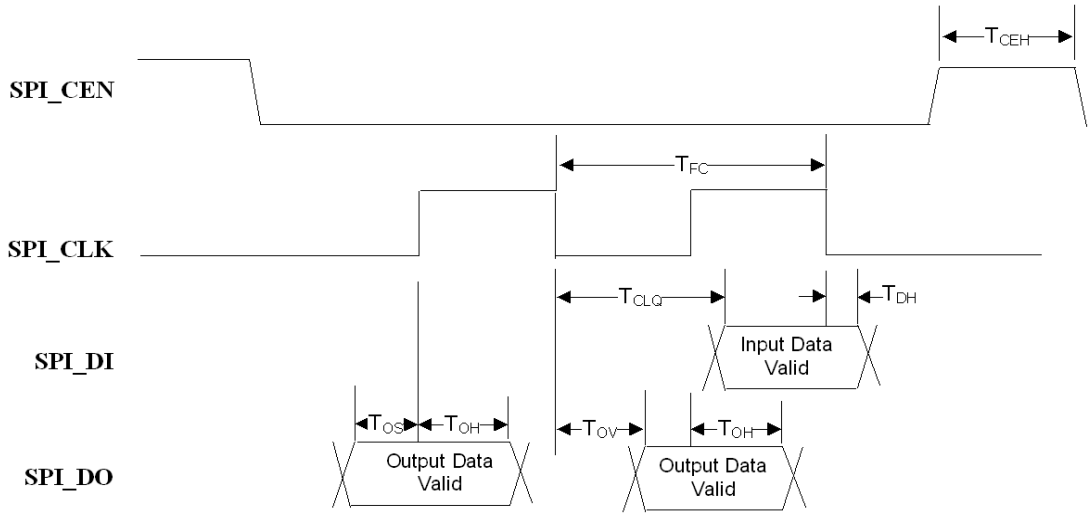

Figure 7.3 SPI Timing

Table 7.2 SPI Timing Operation

Name	Parameter	Min	Max	Unit
T_{FC}	Clock Frequency		60	MHz
T_{CEH}	Chip Enable High Time	50		ns
T_{CLQ}	Clock to Input Data		9	ns
T_{DH}	Input Data Hold Time	0		ns
T_{OS}	Output Set up Time	5		ns
T_{OH}	Output Hold Time	5		ns
T_{OV}	Clock to Output Valid	4		ns

7.4 SMBus Timing

The SMBus slave interface complies with the *SMBus Specification Revision 1.0*. See Section 2.1, *AC Specifications* on page 3 for more information.

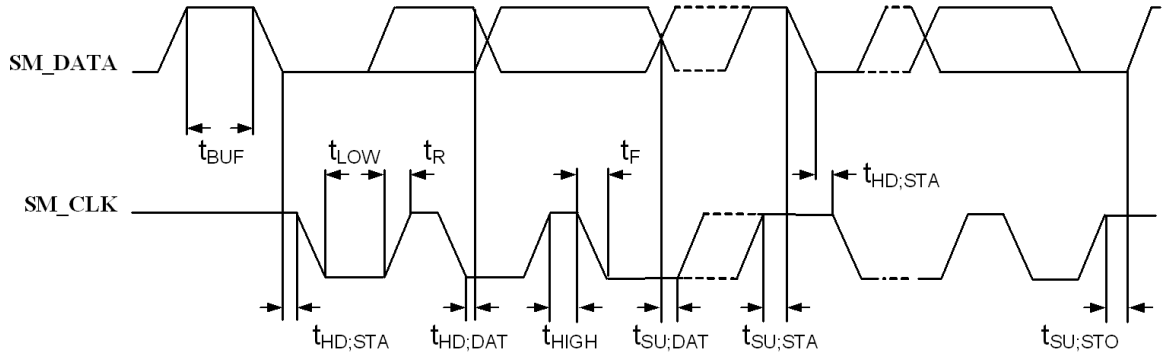

Figure 7.4 SMBus Slave Timing Diagram

Table 7.3 SMBus Slave Timing Modes

SYMBOL	PARAMETER	MIN	MAX	UNIT
f_{SCL}	SM_CLK clock frequency	0	100	KHz
$t_{HD;STA}$	Hold time START condition	4	-	µs
t_{LOW}	LOW period of the SM_CLK clock	4.7	-	µs
t_{HIGH}	HIGH period of the SM_CLK clock	4	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	-	µs
$t_{HD;DAT}$	DATA hold time\	0	-	ns
$t_{SU;DAT}$	DATA set-up time	250	-	ns
t_R	Rise time of both SM_DATA and SM_CLK signals	-	1000	ns
t_F	Fall time of both SM_CLK and SM_DATA lines	-	300	ns
$t_{SU;STO}$	Set-up time for a STOP condition	4	-	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	µs

Chapter 8 Package Drawing

Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging.

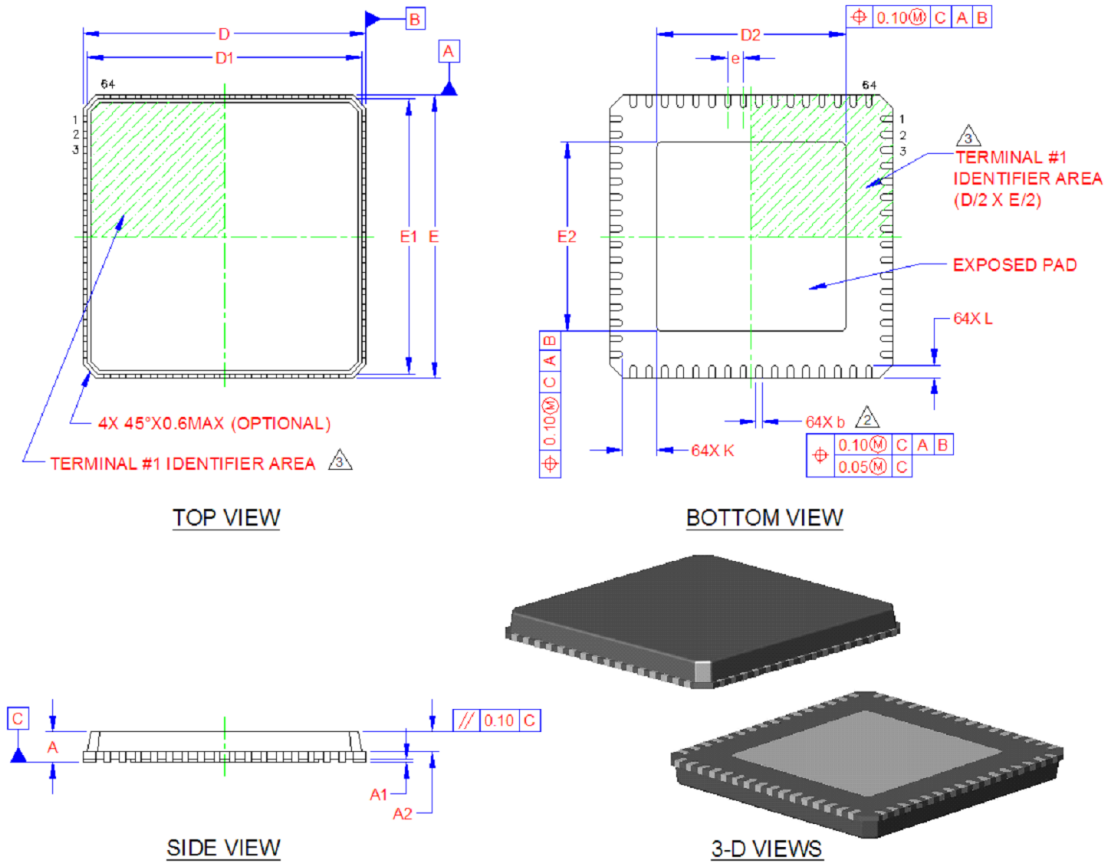

Figure 8.1 USB5533B 64 Pin QFN Package

Table 8.1 USB5533B 64-Pin QFN Dimensions

	MIN	NOMINAL	MAX	REMARKS
A	0.80	0.85	1.00	Overall Package Height
A1	0	0.02	0.05	Standoff
A2	-	0.65	0.80	Mold Cap Thickness
D/E	8.90	9.00	9.10	X/Y Body Size
D1/E1	8.65	8.75	8.85	X/Y Mold Cap Size
D2/E2	5.90	6.00	6.10	X/Y Exposed Pad Size
L	0.30	0.40	0.50	Terminal Length
b	0.18	0.25	0.30	Terminal Width
K	0.90	-	-	Center Pad to Pin Clearance
e		0.50 BSC		Terminal Pitch

Notes:

1. All dimensions are in millimeters unless otherwise noted.
2. Dimension “b” applies to plated terminals and is measured between 0.15 and 0.30 mm from the terminal tip.

3. The pin 1 identifier may vary, but is always located within the zone indicated.

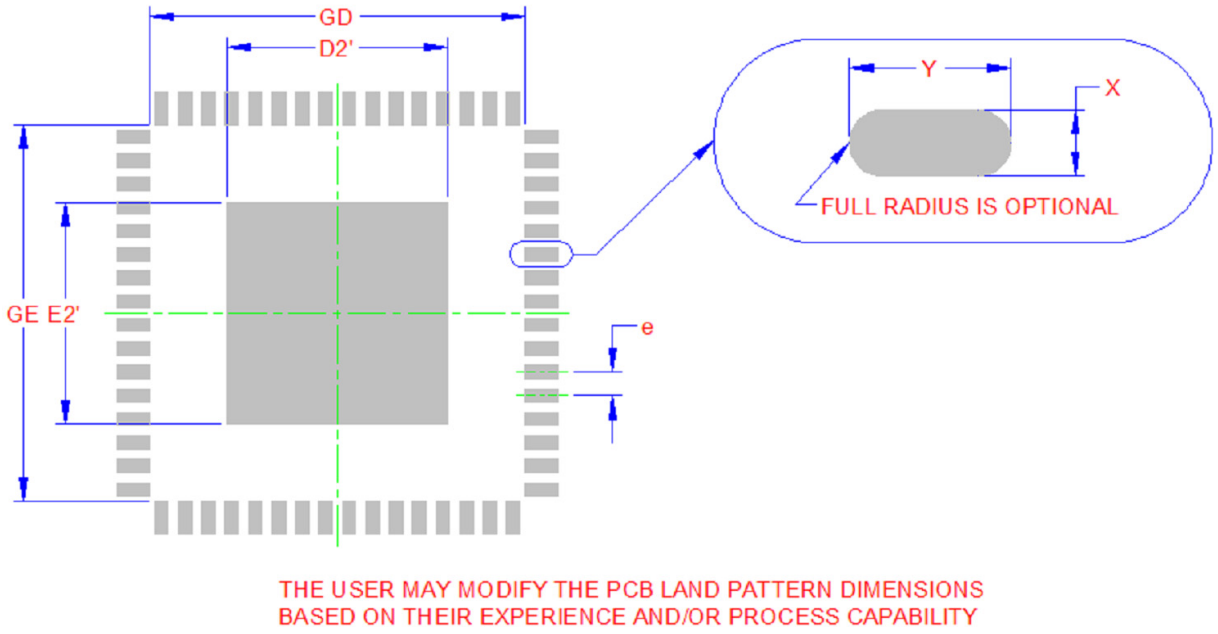

Figure 8.2 USB5533B Recommended PCB Land Pattern

Table 8.2 USB5533B Recommended PCB Land Pattern Dimensions

	MIN (mm)	**NOMINAL** (mm)	**MAX** (mm)
GD/GE	7.93	-	-
D2'/E2'	-	6.00	-
X	-	-	0.28
Y	-	-	0.69
e		0.50	

Chapter 9 Revision History

Table 9.1 Datasheet Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
REV A	Replaces previous SMSC version 1.3; document has been Microchip branded General Description on cover: “legacy” is replaced with “non-USB 1.2”	
Rev. 1.3 (01-23-14)	All	Added -6080 firmware ordering code and info throughout document.
	Chapter 2: *Overview* on page 11	Added information on the -5000 vs. -6080 firmware differences.
	Section 6.5.1: *Package Thermal Specifications* on page 75	Added package thermal specifications.
	Chapter 5: *Functional Operation* on page 30	Renamed chapter. Updated entire chapter with additional information on battery charging, configuration options, OTP, and external SPI operation, runtime register definitions, etc..
	Chapter 4: *Standard Interface Connections* on page 20	Renamed chapter. Added Non-BC Power Configuration and Battery Charging sections.
	Chapter 3: *Pin Information* on page 13	Added alternate functions to TRST pin.
	Section 6.3: *Power Consumption* on page 73	Updated power consumption values.
Rev. 1.2 (05-31-13)	All	Removed industrial temp. SKU information from document.
	Section 6.1: *Maximum Guaranteed Ratings* on page 71	Added maximum power consumption row/data to table.
	Section 6.2: *Operating Conditions* on page 72	Added maximum die temperature row/data to table.
	Section 6.3: *Power Consumption* on page 73	Added power consumption numbers
	on page 17 and Note 3.2 on page 18	Updated note to reflect configuration straps are enabled by default.
	Chapter 3: *Pin Information* on page 13	Updated TRST pin description with the following note: “If using the SMBus interface, a pull-up on this signal will enable Legacy Mode, while leaving it unconnected or pulled-down will enable Advanced Mode.”
	Chapter 8: *Package Drawing* on page 80	Updated recommended land pattern drawings and information.

Table 9.1 Datasheet Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.1 (03-05-13)	Ordering Codes	Updated ordering codes to for A2 material
	Ordering Codes	Corrected tape and reel quantity from 3000 to 2500.
	Section 3.2: *Pin Descriptions (Grouped by Function)* on page 14	Added and Note 3.2 explaining the configuration strap functions on the PRT_PWRx and OCSx pins.
	Section 4.1.2: *Operation of the Dual Hi-Speed Read Sequence* on page 21	Updated first sentence to state that dual data mode is supported only at an SPI speed of 30 MHz
	Chapter 4: *Standard Interface Connections* on page 20	Clarified interface ordering explanation.
	Section 4.2: *SMBus Slave Interface* on page 25	Removed “either an external I2C (if present) and” from last sentence of section.
	Section 4.2: *SMBus Slave Interface* on page 25	Added additional sentence: “For operation in SMBus Legacy Mode, an additional pull-up resistor is required on **TRST**.”
	Section 5.5: *SMBus Slave Interface* on page 37, Figure 5.4: *Block Write* on page 37, Figure 5.5: *Block Read* on page 37	Updated “register address” references to “SMBus RAM buffer offset”.
	SPI_DO pin description & Note 3.1	Added note to describe the SPI_SPD_SEL configuration strap function on the SPI_DO.
	All	Removed references to GPIOs and LEDs
Rev. 1.0 (09-06-12)	All	Initial revision.

Appendix A (Acronyms)

I^2C®: Inter-Integrated Circuit[1]

OCS: Over-Current Sense

PCB: Printed Circuit Board

PHY: Physical Layer

PLL: Phase-Locked Loop

QFN: Quad Flat No Leads

RoHS: Restriction of Hazardous Substances Directive

SCL: Serial Clock

SIE: Serial Interface Engine

SMBus: System Management Bus

TT: Transaction Translator

1. I^2C is a registered trademark of Philips Corporation.

Appendix B (References)

[1] Universal Serial Bus Specification, Version 2.0, April 27, 2000 (12/7/2000 and 5/28/2002 Errata)
USB Implementers Forum, Inc. http://www.usb.org

[2] Universal Serial Bus Specification, Version 3.0, November 13, 2008
USB Implementers Forum, Inc. http://www.usb.org

[3] System Management Bus Specification, version 1.0
SMBus. http://smbus.org/specs/

[4] MicroChip 24AA02/24LC02B (Revision C)
Microchip Technology Inc. http://www.microchip.com/

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