N-Channel Enhancement-Mode Vertical DMOS FET

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral source-drain diode
- High input impedance and high gain

Applications

- Motor controls
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

General Description

This enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven, silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Device	Package Option	BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (max) (Ω)	$I_{D(ON)}$ (min) (A)
	TO-92			
VN1206	VN1206L-G	120	6.0	1.0

-G indicates package is RoHS compliant ('Green')

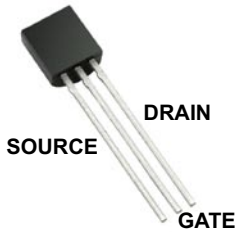
Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Gate-to-source voltage	±30V
Operating and storage temperature	-55°C to +150°C
Soldering temperature*	300°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

* *Distance of 1.6mm from case for 10 seconds.*

Pin Configuration



TO-92 (L)

Product Marking

YY = Year Sealed
WW = Week Sealed
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-92 (L)

Thermal Characteristics

Package	I_D (continuous)† (mA)	I_D (pulsed) (A)	Power Dissipation @T_c = 25°C (W)	θ_{jc} (°C/W)	θ_{ja} (°C/W)	I_{DR}† (mA)	I_{DRM} (A)
TO-92	230	2.0	1.0	125	170	230	2.0

Notes:

† I_D (continuous) is limited by max rated T_j .

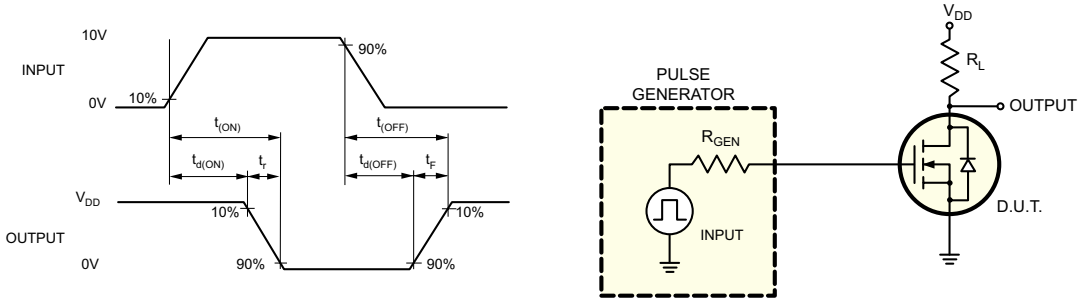
Electrical Characteristics (T_A = 25°C unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	120	-	-	V	V_{GS} = 0V, I_D = 100µA
$V_{GS(th)}$	Gate threshold voltage	0.8	-	2.0	V	V_{GS} = V_{DS}, I_D = 1.0mA
I_{GSS}	Gate body leakage	-	-	100	nA	V_{GS} = ±15V, V_{DS} = 0V
I_{DSS}	Zero gate voltage drain current	-	-	10	µA	V_{GS} = 0V, V_{DS} = Max Rating
		-	-	500		V_{DS} = 0.8Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	On-state drain current	1.0	-	-	A	V_{GS} = 10V, V_{DS} = 10V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	-	10	Ω	V_{GS} = 2.5V, I_D = 100mA
		-	-	6.0		V_{GS} = 10V, I_D = 500mA
G_{FS}	Forward transductance	300	-	-	mmho	V_{DS} = 10V, I_D = 500mA
C_{ISS}	Input capacitance	-	-	125	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz
C_{OSS}	Common source output capacitance	-	-	50		
C_{RSS}	Reverse transfer capacitance	-	-	20		
t_r	Rise time	-	-	8.0	ns	V_{DD} = 60V, I_D = 400mA, R_{GEN} = 25Ω
$t_{d(ON)}$	Turn-on delay time	-	-	8.0		
t_f	Fall time	-	-	12		
$t_{d(OFF)}$	Turn-off delay time	-	-	18		
V_{SD}	Diode forward voltage drop	-	1.2	-	V	V_{GS} = 0V, I_{SD} = 250mA

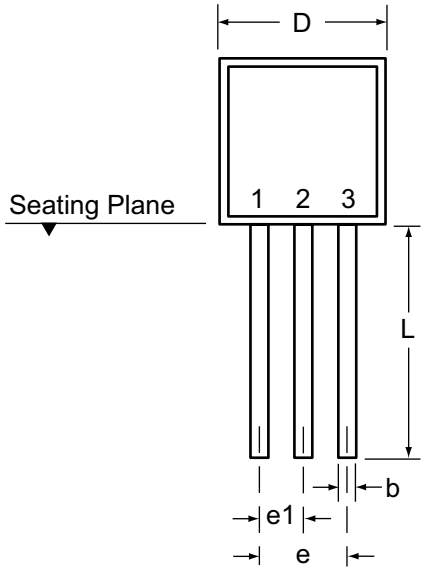
Notes:

1. *All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)*
2. *All A.C. parameters sample tested.*

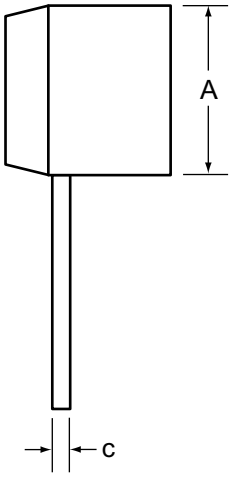
Switching Waveforms and Test Circuit



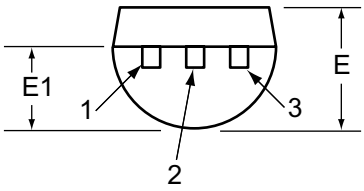
3-Lead TO-92 Package Outline (L)



Front View



Side View



Bottom View

Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014†	.014†	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022†	.022†	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
***Supertex Doc.#:** DSPD-3TO92N3, Version E041009.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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