NX3008CBKV

30 / 30 V, 400 / 220 mA N/P-channel Trench MOSFET Rev. 1 — 29 July 2011 Product

Product data sheet

1. **Product profile**

1.1 General description

Complementary N/P-channel enhancement mode Field-Effect Transistor (FET) in an ultra small and flat lead SOT666 Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Low threshold voltage
- Very fast switching
- Trench MOSFET technology
- ESD protection up to 2 kV
- AEC-Q101 qualified

1.3 Applications

- Level shifter
- Power supply converter

- Load switch
- Switching circuits

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
TR2 (P-cha	annel)						
V_{DS}	drain-source voltage	T _j = 25 °C		-	-	-30	V
V_{GS}	gate-source voltage			-8	-	8	V
I _D	drain current	V_{GS} = -4.5 V; T_{amb} = 25 °C	[1]	-	-	-220	mA
TR1 (N-cha	annel)						
V_{DS}	drain-source voltage	T _j = 25 °C		-	-	30	V
V_{GS}	gate-source voltage			-8	-	8	V
I _D	drain current	$V_{GS} = 4.5 \text{ V}; T_{amb} = 25 ^{\circ}\text{C}$	<u>[1]</u>	-	-	400	mA
TR1 (N-cha	annel), Static character	istics					
R _{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 350 \text{ mA};$ $T_j = 25 \text{ °C}$		-	1	1.4	Ω
TR2 (P-channel), Static characteristics							
R _{DSon}	drain-source on-state resistance	V_{GS} = -4.5 V; I_{D} = -200 mA; T_{j} = 25 °C		-	2.8	4.1	Ω

^[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1		
2	G1	gate TR1	6 5 4	D1 D2
3	D2	drain TR2		
4	S2	source TR2		$G1 \longrightarrow G2$
5	G2	gate TR2	1 2 3	
6	D1	drain TR1	SOT666 (SOT666)	S1 S2 017aaa262

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
NX3008CBKV	SOT666	plastic surface-mounted package; 6 leads	SOT666

4. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
NX3008CBKV	AC

^{[1] % =} placeholder for manufacturing site code.

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
TR2 (P-char	nnel)				
V_{DS}	drain-source voltage	T _j = 25 °C	-	-30	V
V_{GS}	gate-source voltage		-8	8	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C	<u>[1]</u> _	-220	mA
		V _{GS} = -4.5 V; T _{amb} = 100 °C	<u>[1]</u> _	-140	mA
I _{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \le 10 \mu s$	-	-0.9	А
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	330	mW
			<u>[1]</u> _	390	mW
		T _{sp} = 25 °C	-	1090	mW
TR1 (N-char	nnel)				
V_{DS}	drain-source voltage	T _j = 25 °C	-	30	V
V_{GS}	gate-source voltage		-8	8	V
I_{D}	drain current	$V_{GS} = 4.5 \text{ V}; T_{amb} = 25 ^{\circ}\text{C}$	<u>[1]</u> _	400	mA
		V _{GS} = 4.5 V; T _{amb} = 100 °C	<u>[1]</u> _	260	mA
I_{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \le 10 \mu s$	-	1.6	Α
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	330	mW
			<u>[1]</u> _	390	mW
		T _{sp} = 25 °C	-	1090	mW
Per device					
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	500	mW
Tj	junction temperature		-55	150	°C
T _{amb}	ambient temperature		-55	150	°C
T _{stg}	storage temperature		-65	150	°C
TR1 (N-char	nnel), Source-drain diode				
Is	source current	T _{amb} = 25 °C	<u>[1]</u> -	400	mA
TR2 (P-char	nnel), Source-drain diode				
Is	source current	T _{amb} = 25 °C	<u>[1]</u> -	-220	mA
TR1 N-chan	nel), ESD maximum rating				
V_{ESD}	electrostatic discharge voltage	НВМ	<u>[3]</u> _	2000	V
TR2 (P-char	nnel), ESD maximum rating				
V _{ESD}	electrostatic discharge voltage	НВМ	<u>[3]</u> _	2000	V

 $[\]label{eq:condition} \textbf{[1]} \quad \text{Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm2.}$

^[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper; tin-plated and standard footprint.

^[3] Measured between all pins.

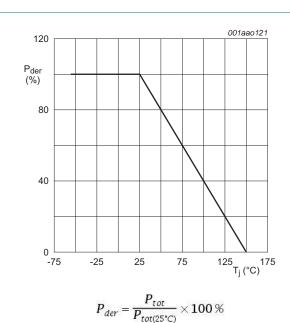


Fig 1. Normalized total power dissipation as a function of junction temperature

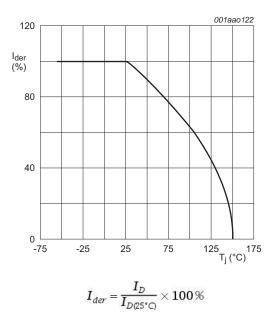
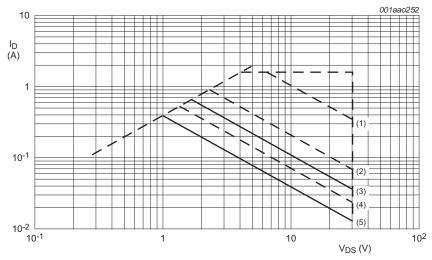


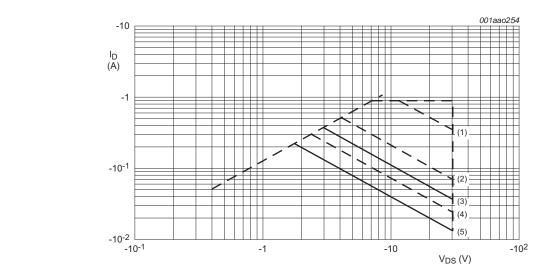
Fig 2. Normalized continuous drain current as a function of junction temperature



I_{DM} is a single pulse

- (1) $t_p = 1 \text{ ms}$
- (2) $t_p = 10 \text{ ms}$
- (3) DC; $T_{sp} = 25 \, ^{\circ}\text{C}$
- (4) $t_p = 100 \text{ ms}$
- (5) DC; T_{amb} = 25 °C; 1 cm² drain mounting pad

Fig 3. Safe operating area TR1 (N-channel); junction to ambient; continuous and peak drain currents as a function of drain-source voltage



I_{DM} is a single pulse

- (1) $t_p = 1 \text{ ms}$
- (2) $t_p = 10 \text{ ms}$
- (3) DC; $T_{sp} = 25 \, ^{\circ}\text{C}$
- (4) $t_p = 100 \text{ ms}$
- (5) DC; T_{amb} = 25 °C; 1 cm² drain mounting pad

Fig 4. Safe operating area TR2 (P-channel); junction to ambient; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per device							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	<u>[1]</u>	-	-	250	K/W
TR1 (N-chani	nel)						
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	<u>[1]</u>	-	330	380	K/W
			[2]	-	280	320	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	-	115	K/W
TR2 (P-chani	nel)						
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	<u>[1]</u>	-	330	380	K/W
			[2]	-	280	320	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	-	115	K/W

^[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper; tin-plated and standard footprint.

^[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².

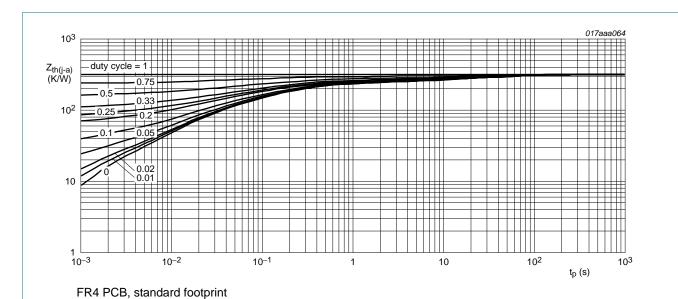
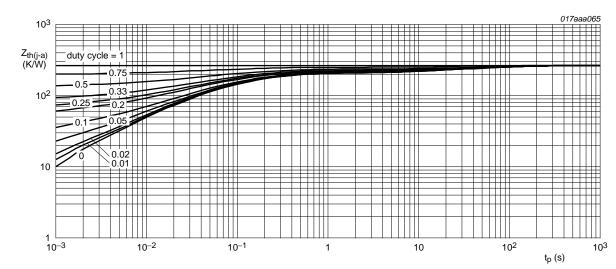
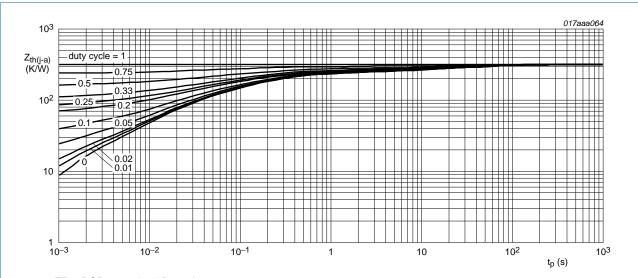


Fig 5. TR1: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



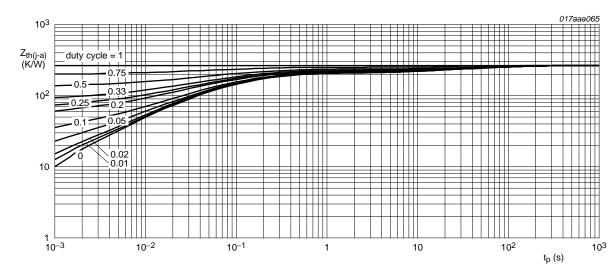
FR4 PCB, mounting pad for drain 1 cm²

Fig 6. TR1: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, standard footprint

Fig 7. TR2, Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 1 cm²

Fig 8. TR2, Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
TR2 (P-cha	nnel), Static characteristic	s				
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	-30	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ °C}$	-0.6	-0.9	-1.1	V
I_{DSS}	drain leakage current	$V_{DS} = -30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	-1	μΑ
		$V_{DS} = -30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ °C}$	-	-	-10	μΑ
I_{GSS}	gate leakage current	$V_{GS} = 8 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-0.2	-1	μΑ
		$V_{GS} = -8 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-0.2	-1	μΑ
		$V_{GS} = 4.5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-10	-	nΑ
		$V_{GS} = -4.5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-10	-	nΑ
		$V_{GS} = 2.5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-1	-	nΑ
		$V_{GS} = -2.5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-1	-	nΑ
R _{DSon}	drain-source on-state	V_{GS} = -4.5 V; I_D = -200 mA; T_j = 25 °C	-	2.8	4.1	Ω
	resistance	$V_{GS} = -2.5 \text{ V}; I_D = -10 \text{ mA}; T_j = 25 \text{ °C}$	-	5.3	6.5	Ω
		$V_{GS} = -4.5 \text{ V}; I_D = -200 \text{ mA}; T_j = 150 \text{ °C}$	-	5.3	7.8	Ω
g _{fs}	transfer conductance	$V_{DS} = -10 \text{ V}; I_D = -200 \text{ mA}; T_j = 25 \text{ °C}$	-	160	-	mS
TR1 (N-cha	nnel), Static characteristic	s				
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	30	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ °C}$	0.6	0.9	1.1	V
I _{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	1	μΑ
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 ^{\circ}\text{C}$	-	-	10	μΑ
I _{GSS}	gate leakage current	$V_{GS} = 8 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.2	1	μΑ
		$V_{GS} = -8 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.2	1	μΑ
		$V_{GS} = 4.5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	10	-	nA
		$V_{GS} = -4.5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	10	-	nA
		$V_{GS} = 2.5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	1	-	nA
		$V_{GS} = -2.5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	1	-	nA
R _{DSon}	drain-source on-state	$V_{GS} = 4.5 \text{ V}; I_D = 350 \text{ mA}; T_j = 25 \text{ °C}$	-	1	1.4	Ω
	resistance	$V_{GS} = 4.5 \text{ V}; I_D = 350 \text{ mA}; T_j = 150 \text{ °C}$	-	1.8	2.5	Ω
		$V_{GS} = 2.5 \text{ V}; I_D = 200 \text{ mA}; T_j = 150 \text{ °C}$	-	1.4	2.1	Ω
		$V_{GS} = 1.8 \text{ V}; I_D = 10 \text{ mA}; T_j = 25 \text{ °C}$	-	2	2.8	Ω
9 _{fs}	transfer conductance	$V_{DS} = 10 \text{ V}; I_D = 350 \text{ mA}; T_j = 25 \text{ °C}$	-	310	-	mS
TR1 (N-cha	nnel), Dynamic characteri	stics				
Q _{G(tot)}	total gate charge	$V_{DS} = 15 \text{ V}; I_D = 400 \text{ mA}; V_{GS} = 4.5 \text{ V};$	-	0.52	0.68	nC
Q _{GS}	gate-source charge	T _j = 25 °C	-	0.17	-	nC
Q_{GD}	gate-drain charge		-	0.08		nC

Table 7. Characteristics ... continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
C _{iss}	input capacitance	$V_{DS} = 15 \text{ V}; f = 1 \text{ MHz}; V_{GS} = 0 \text{ V};$	-	34	50	pF
Coss	output capacitance	T _j = 25 °C	-	6.5	-	pF
C _{rss}	reverse transfer capacitance		-	2.2	-	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 20 \text{ V}; R_L = 250 \Omega; V_{GS} = 4.5 \text{ V};$	-	15	30	ns
t _r	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 °C$	-	11	-	ns
t _{d(off)}	turn-off delay time		-	69	138	ns
t _f	fall time		-	19	-	ns
TR2 (P-chani	nel), Dynamic characteri	istics				
Q _{G(tot)}	total gate charge	$V_{DS} = -15 \text{ V; } I_D = -200 \text{ mA;}$ $V_{GS} = -4.5 \text{ V; } T_j = 25 \text{ °C}$	-	0.55	0.72	nC
Q_{GS}	gate-source charge		-	0.23	-	nC
Q_{GD}	gate-drain charge		-	0.09	-	nC
C _{iss}	input capacitance	$V_{DS} = -15 \text{ V}; f = 1 \text{ MHz}; V_{GS} = 0 \text{ V};$	-	31	46	pF
C _{oss}	output capacitance	T _j = 25 °C	-	6.5	-	pF
C _{rss}	reverse transfer capacitance		-	2.3	-	pF
t _{d(on)}	turn-on delay time	V_{DS} = -20 V; R_L = 250 Ω ; V_{GS} = -4.5 V;	-	19	38	ns
t _r	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 °C$	-	30	-	ns
t _{d(off)}	turn-off delay time		-	65	130	ns
t _f	fall time		-	38	-	ns
TR2 (P-chann	nel), Source-drain diode	characteristics				
V_{SD}	source-drain voltage	$I_S = -200 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-0.47	-0.88	-1.2	V
TD4 /N shop	nel), Source-drain diode	characteristics				
TRT (IN-Chan	nei), oodi ce-arain diode					

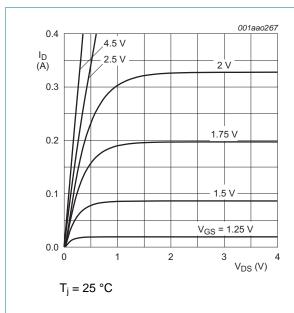
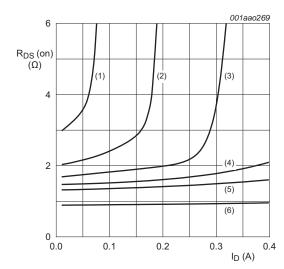


Fig 9. TR1: Output characteristics: drain current as a function of drain-source voltage; typical values



 $T_i = 25 \, ^{\circ}C$

(1) $V_{GS} = 1.5 \text{ V}$

(2) $V_{GS} = 1.75 \text{ V}$

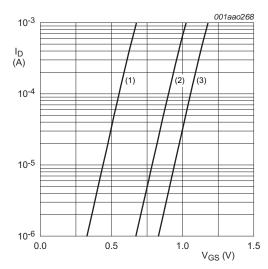
(3) $V_{GS} = 2.0 \text{ V}$

(4) $V_{GS} = 2.25 \text{ V}$

(5) $V_{GS} = 2.5 \text{ V}$

(6) $V_{GS} = 4.5 \text{ V}$

Fig 11. TR1: Drain-source on-state resistance as a function of drain current; typical values



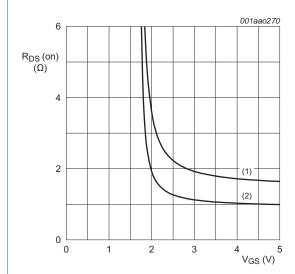
 $T_{j} = 25 \, ^{\circ}\text{C}; \, V_{DS} = 5 \, \text{V}$

(1) minimum values

(2) typical values

(3) maximum values

Fig 10. TR1: Sub-threshold drain current as a function of gate-source voltage

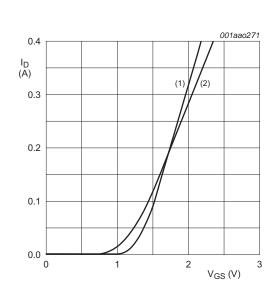


 $I_D = 400 \text{ mA}$

(1) $T_i = 150 \,^{\circ}C$

(2) $T_i = 25 \, ^{\circ}C$

Fig 12. TR1: Drain-source on-state resistance as a function of gate-source voltage; typical values



 $V_{DS} > I_D \times R_{DSon}$

(1)
$$T_j = 25 \, ^{\circ}C$$

(2) $T_i = 150 \, ^{\circ}\text{C}$

Fig 13. TR1: Transfer characteristics: drain current as a function of gate-source voltage; typical values

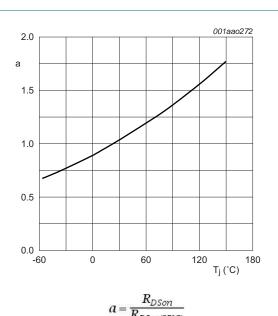
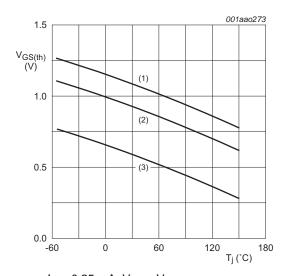


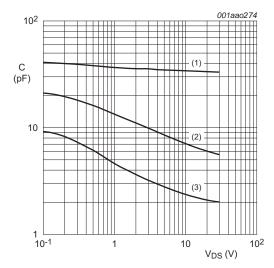
Fig 14. TR1: Normalized drain-source on-state resistance as a function of junction temperature; typical values



 I_D = 0.25 mA; V_{DS} = V_{GS}

- (1) maximum values
- (2) typical values
- (3) minimum values

Fig 15. TR1: Gate-source threshold voltage as a function of junction temperature



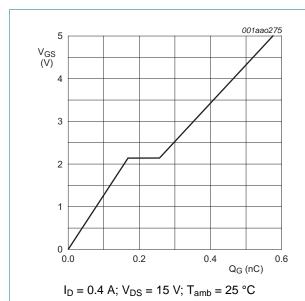
 $f = 1 MHz; V_{GS} = 0 V$

(1)C_{iss}

(2)Coss

(3)C_{rss}

Fig 16. TR1: Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



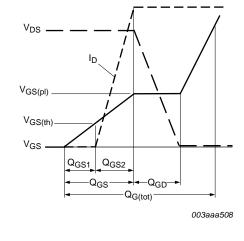
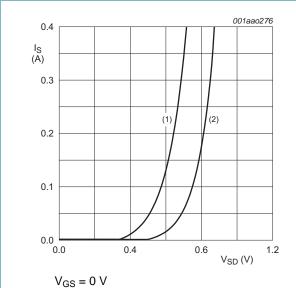
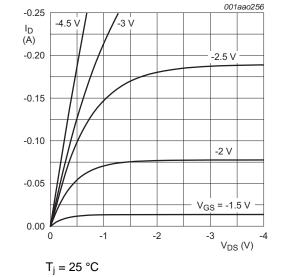


Fig 17. TR1: Gate-source voltage as a function of gate charge; typical values

Fig 18. Gate charge waveform definitions

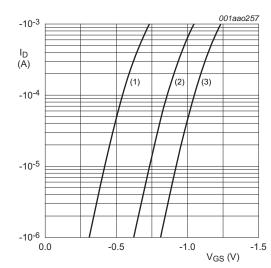




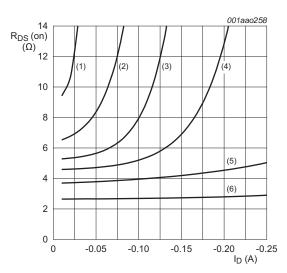
 $(1) T_j = 150 \text{ °C}$ $(2) T_j = 25 \text{ °C}$

Fig 19. TR1: Source current as a function of source-drain voltage; typical values

Fig 20. TR2: Output characteristics: drain current as a function of drain-source voltage; typical values



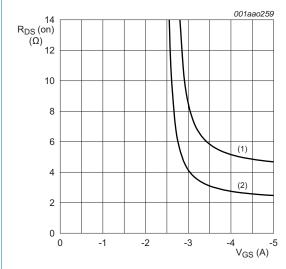
- $T_{j} = 25 \, ^{\circ}\text{C}; \, V_{DS} = -5 \, \text{V}$
- (1) minimum values
- (2) typical values
- (3) maximum values



- T_j = 25 °C
- (1) $V_{GS} = -1.75 \text{ V}$
- (2) $V_{GS} = -2.0 \text{ V}$
- (3) $V_{GS} = -2.25 \text{ V}$
- (4) $V_{GS} = -2.5 \text{ V}$
- (5) $V_{GS} = -3.0 \text{ V}$
- (6) $V_{GS} = -4.5 \text{ V}$

Fig 21. TR2: Sub-threshold drain current as a function of gate-source voltage



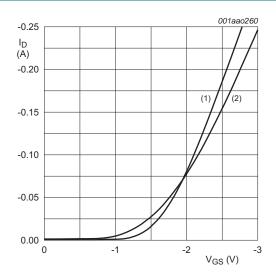


 $I_D = -200 \text{ mA}$

(1) $T_i = 150 \, ^{\circ}\text{C}$

(2) $T_j = 25 \, {}^{\circ}\text{C}$

Fig 23. TR2: Drain-source on-state resistance as a function of gate-source voltage; typical values



 $V_{DS} > I_D \times R_{DSon}$

(1) $T_i = 25 \, ^{\circ}C$

(2) $T_i = 150 \, ^{\circ}\text{C}$

Fig 24. TR2: Transfer characteristics: drain current as a function of gate-source voltage; typical values

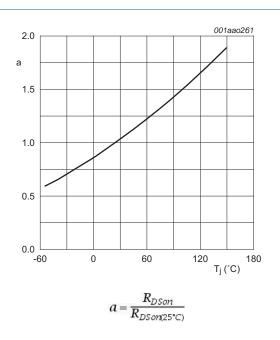
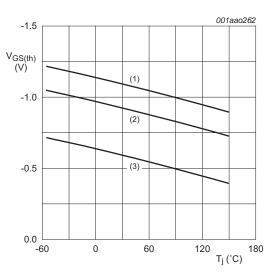


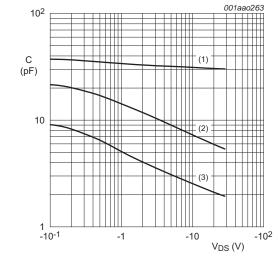
Fig 25. TR2: Normalized drain-source on-state resistance as a function of junction temperature; typical values



 I_D = -0.25 mA; V_{DS} = V_{GS}

- (1) maximum values
- (2) typical values
- (3) minimum values

Fig 26. TR2: Gate-source threshold voltage as a function of junction temperature



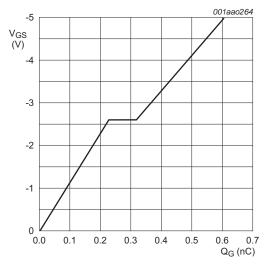
 $f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$

 $(1)C_{iss}$

(2)Coss

(3)C_{rss}

Fig 27. TR2: Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

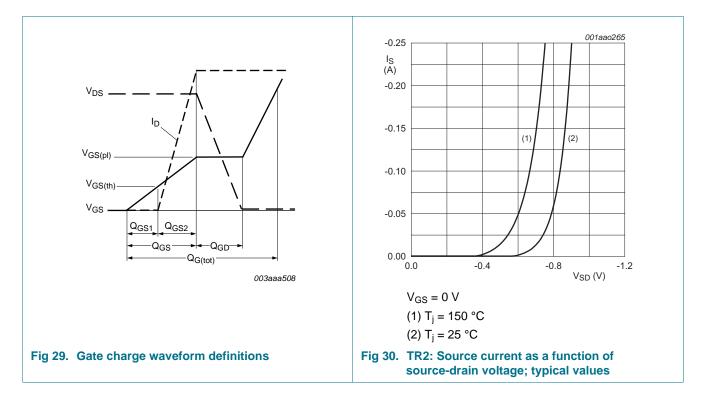


 $I_D = -200 \text{ mA}; V_{DS} = -15 \text{ V}; T_{amb} = 25 \text{ °C}$

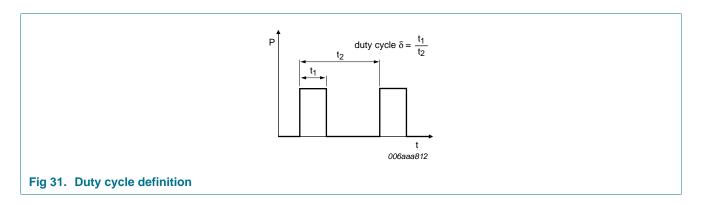
Fig 28. Gate-source voltage as a function of gate charge; typical values

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8. Test information



8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

9. Package outline

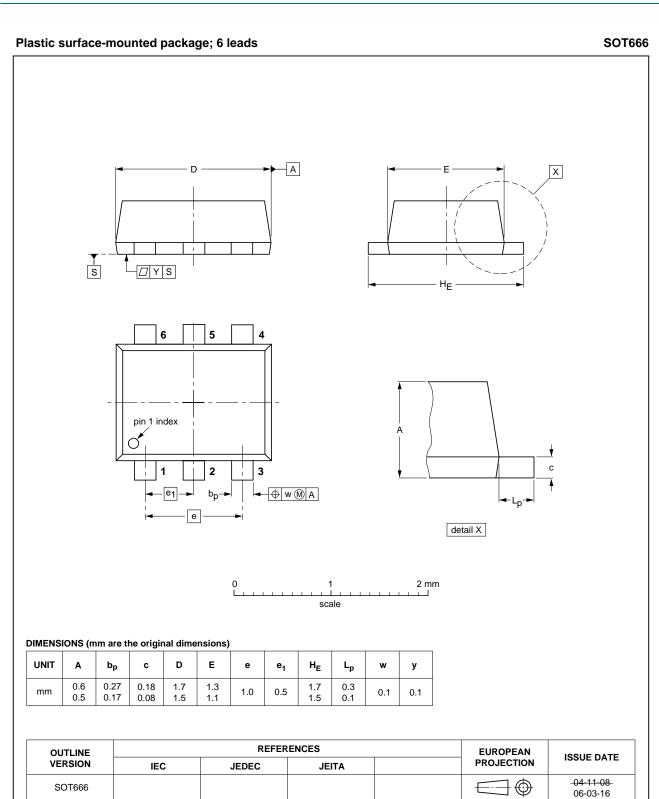


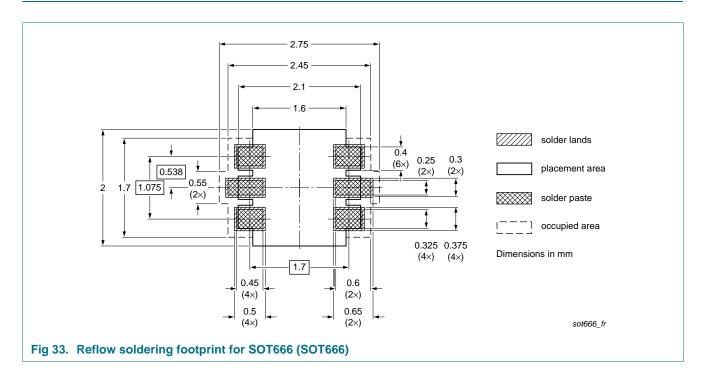
Fig 32. Package outline SOT666 (SOT666)

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10. Soldering



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11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX3008CBKV v.1	20110729	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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