



# PHPT610035PK

PNP/PNP matched high power double bipolar transistor

24 October 2014

Product data sheet

## 1. General description

PNP/PNP high power matched double bipolar transistor in a SOT1205 (LFAK56D) Surface-Mounted Device (SMD) power plastic package. Matched version of PHPT610030PK.

NPN/NPN complement: PHPT610035NK.

## 2. Features and benefits

- Current gain matching 10 %
- High thermal power dissipation capability
- Suitable for high temperature applications up to 175 °C
- Reduced Printed-Circuit Board (PCB) requirements comparing to transistors in DPAK
- High energy efficiency due to less heat generation
- AEC-Q101 qualified

## 3. Applications

- Current mirror
- Motor control
- Power management
- Backlighting applications
- Relay replacement
- Differential amplifiers

## 4. Quick reference data

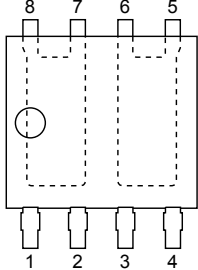
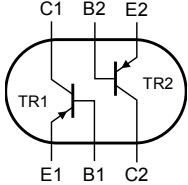
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
$V_{CEO}$	collector-emitter voltage	open base	-	-	-100	V
$I_C$	collector current		-	-	-3	A
<b>Per transistor</b>						
$R_{CEsat}$	collector-emitter saturation resistance	$I_C = -2\text{ A}; I_B = -200\text{ mA};$ pulsed; $t_p \leq 300\ \mu\text{s}; \delta \leq 0.02; T_{amb} = 25\text{ °C}$	-	110	180	m $\Omega$



## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E1	emitter TR1	 <p><b>LFPAK56D (SOT1205)</b></p>	 <p><i>sym138</i></p>
2	B1	base TR1		
3	E2	emitter TR2		
4	B2	base TR2		
5	C2	collector TR2		
6	C2	collector TR2		
7	C1	collector TR1		
8	C1	collector TR1		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PHPT610035PK	LFPAK56D	Plastic single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

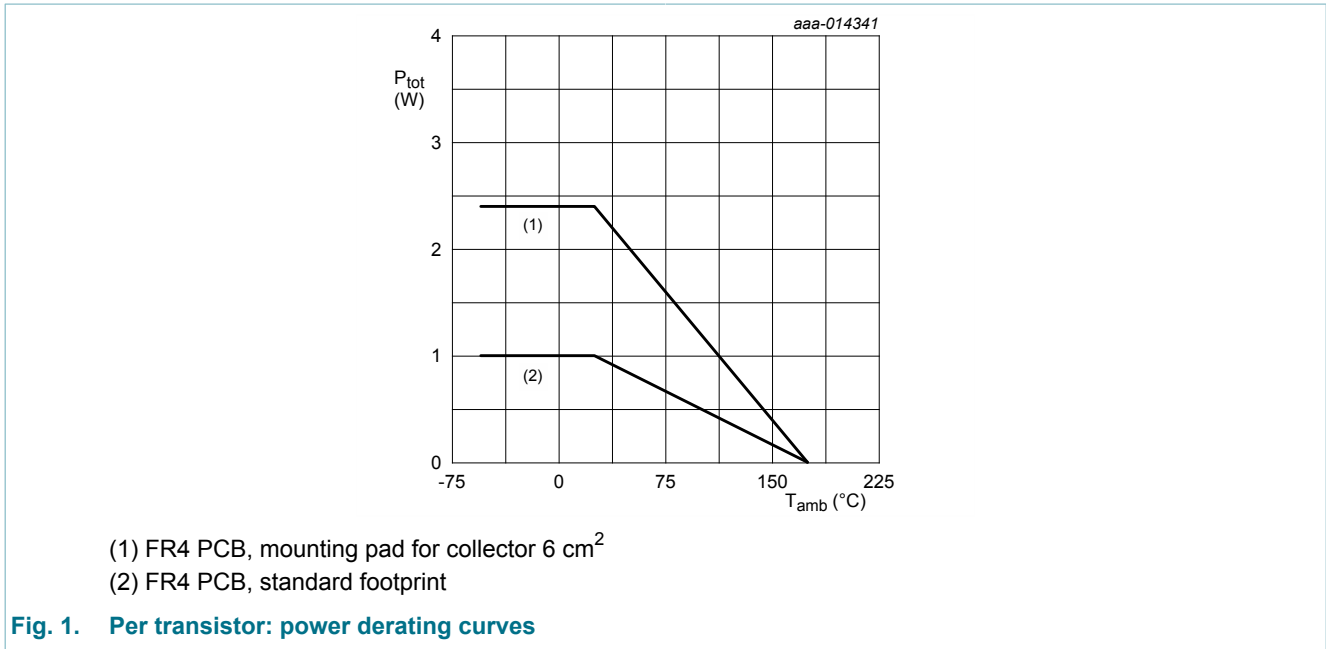
## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
<b>Per transistor</b>						
V <sub>CBO</sub>	collector-base voltage	open emitter		-	-100	V
V <sub>CEO</sub>	collector-emitter voltage	open base		-	-100	V
V <sub>EBO</sub>	emitter-base voltage	open collector		-	-8	V
I <sub>C</sub>	collector current			-	-3	A
I <sub>CM</sub>	peak collector current	single pulse; t <sub>p</sub> ≤ 1 ms		-	-8	A
I <sub>B</sub>	base current			-	-0.5	A
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	1	W
			[2]	-	2.4	W
			[3]	-	25	W
<b>Per device</b>						
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	1.25	W
			[2]	-	3	W
			[4]	-	5	W
T <sub>j</sub>	junction temperature			-	175	°C
T <sub>amb</sub>	ambient temperature			-55	175	°C
T <sub>stg</sub>	storage temperature			-65	175	°C

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm<sup>2</sup>.
- [3] Power dissipation from junction to mounting base.
- [4] Device mounted on a ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint.

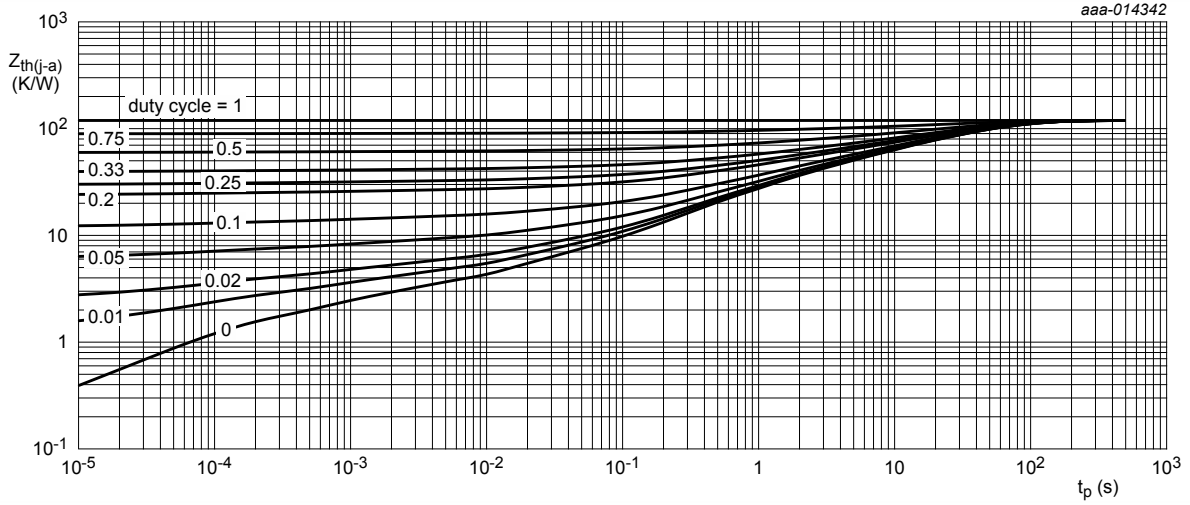


## 8. Thermal characteristics

Table 5. Thermal characteristics

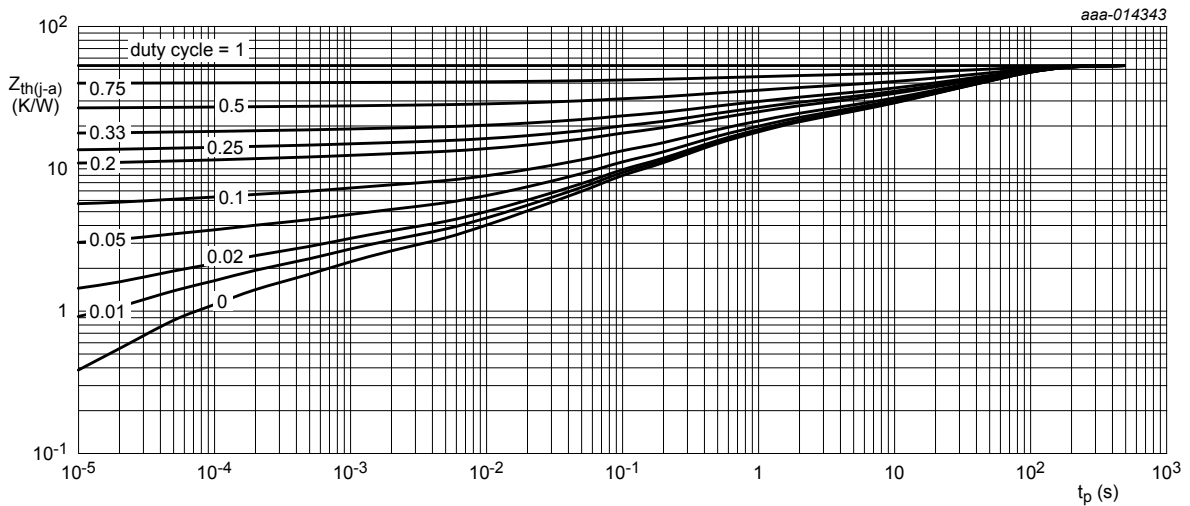
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per transistor</b>							
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	-	150	K/W
			[2]	-	-	62.5	K/W
R <sub>th(j-sp)</sub>	thermal resistance from junction to solder point			-	-	6	K/W
<b>Per device</b>							
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	-	120	K/W
			[2]	-	-	50	K/W
			[3]	-	-	30	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm<sup>2</sup>.
- [3] Device mounted on a ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint.



FR4 PCB, standard footprint

**Fig. 2. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



FR4 PCB, mounting pad for collector  $6 \text{ cm}^2$

**Fig. 3. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

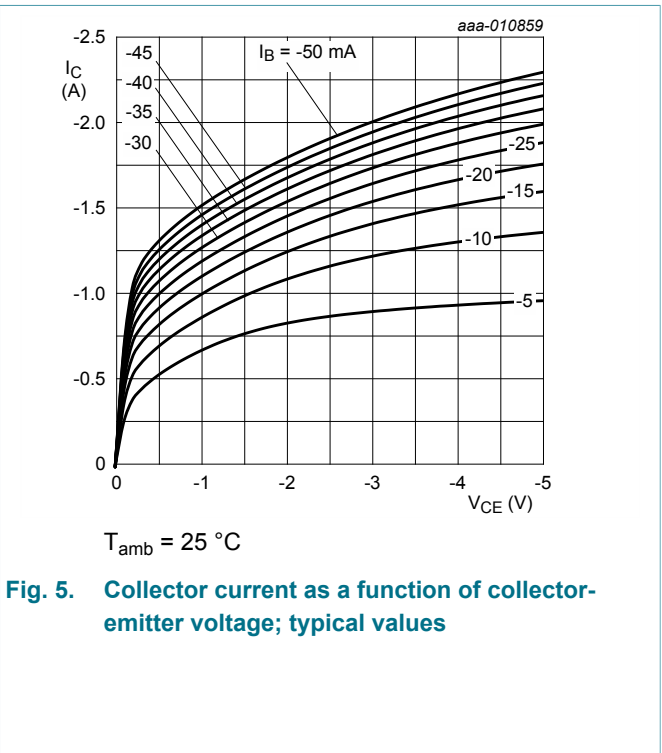
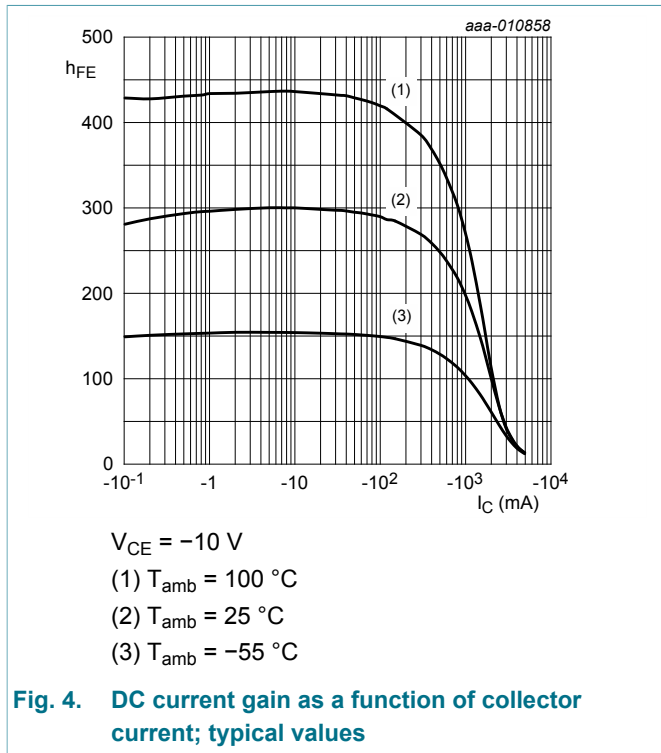
## 9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$h_{FE1}/h_{FE2}$	$h_{FE}$ matching	$V_{CE} = -2\text{ V}; I_C = 1\text{ A}$	0.9	1	1.1	
<b>Per transistor</b>						
$I_{CBO}$	collector-base cut-off current	$V_{CB} = -80\text{ V}; I_E = 0\text{ A}; T_{amb} = 25\text{ °C}$	-	-	-100	nA
		$V_{CB} = -80\text{ V}; I_E = 0\text{ A}; T_j = 150\text{ °C}$	-	-	-50	$\mu\text{A}$
$I_{CES}$	collector-emitter cut-off current	$V_{CE} = -80\text{ V}; V_{BE} = 0\text{ V}; T_{amb} = 25\text{ °C}$	-	-	-100	nA
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = -7\text{ V}; I_C = 0\text{ A}; T_{amb} = 25\text{ °C}$	-	-	-100	nA
$h_{FE}$	DC current gain	$V_{CE} = -10\text{ V}; I_C = -500\text{ mA}; T_{amb} = 25\text{ °C}$	150	220	-	
		$V_{CE} = -10\text{ V}; I_C = -1\text{ A};$ pulsed; $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02; T_{amb} = 25\text{ °C}$	80	210	-	
		$V_{CE} = -10\text{ V}; I_C = -2\text{ A};$ pulsed; $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02; T_{amb} = 25\text{ °C}$	20	100	-	
		$V_{CE} = -2\text{ V}; I_C = -1\text{ A}; T_{amb} = 25\text{ °C}$	100	200	-	
		$V_{CE} = -10\text{ V}; I_C = -3\text{ A};$ pulsed; $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02; T_{amb} = 25\text{ °C}$	10	40	-	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = -500\text{ mA}; I_B = -50\text{ mA}; T_{amb} = 25\text{ °C}$	-	-70	-110	mV
		$I_C = -2\text{ A}; I_B = -200\text{ mA};$ pulsed; $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02; T_{amb} = 25\text{ °C}$	-	-220	-360	mV
$R_{CEsat}$	collector-emitter saturation resistance	$t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02; T_{amb} = 25\text{ °C}$	-	110	180	$\text{m}\Omega$
$V_{BEsat}$	base-emitter saturation voltage	$I_C = -1\text{ A}; I_B = -50\text{ mA};$ pulsed; $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02; T_{amb} = 25\text{ °C}$	-	-0.91	-1	V
		$I_C = -2\text{ A}; I_B = -200\text{ mA};$ pulsed; $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02; T_{amb} = 25\text{ °C}$	-	-1.02	-1.2	V
$V_{BEon}$	base-emitter turn-on voltage	$V_{CE} = -2\text{ V}; I_C = -100\text{ mA};$ pulsed; $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02; T_{amb} = 25\text{ °C}$	-	-0.68	-0.9	V
$t_d$	delay time	$V_{CC} = -12.5\text{ V}; I_C = -1\text{ A}; I_{Bon} = -50\text{ mA}; I_{Boff} = 50\text{ mA}; T_{amb} = 25\text{ °C}$	-	20	-	ns
$t_r$	rise time		-	180	-	ns
$t_{on}$	turn-on time		-	200	-	ns
$t_s$	storage time		-	350	-	ns
$t_f$	fall time		-	220	-	ns
$t_{off}$	turn-off time		-	570	-	ns

PNP/PNP matched high power double bipolar transistor

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_T$	transition frequency	$V_{CE} = -10\text{ V}; I_C = -100\text{ mA};$ $f = 100\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}$	-	125	-	MHz
$C_c$	collector capacitance	$V_{CB} = -10\text{ V}; I_E = 0\text{ A}; i_e = 0\text{ A};$ $f = 1\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}$	-	30	-	pF



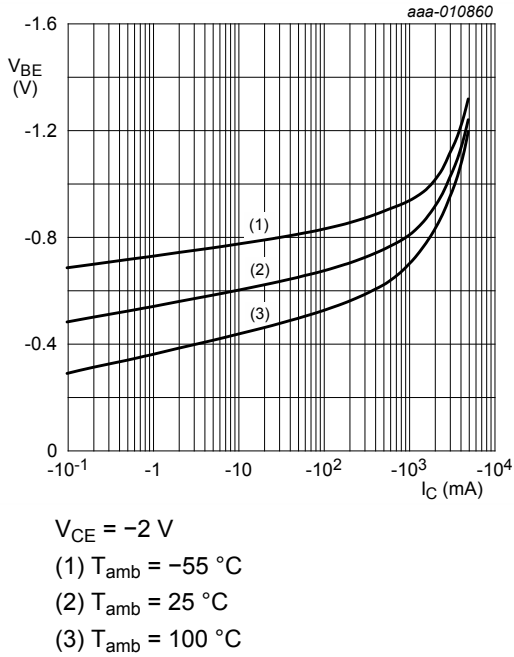


Fig. 6. Base-emitter voltage as a function of collector current; typical values

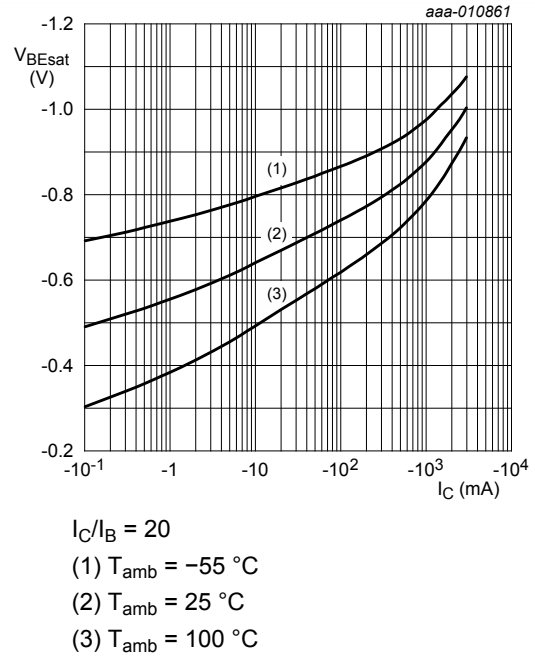


Fig. 7. Base-emitter saturation voltage as a function of collector current; typical values

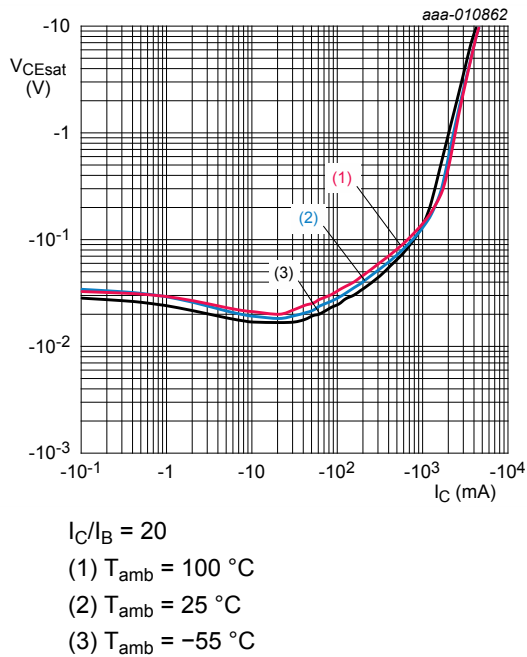


Fig. 8. Collector-emitter saturation voltage as a function of collector current; typical values

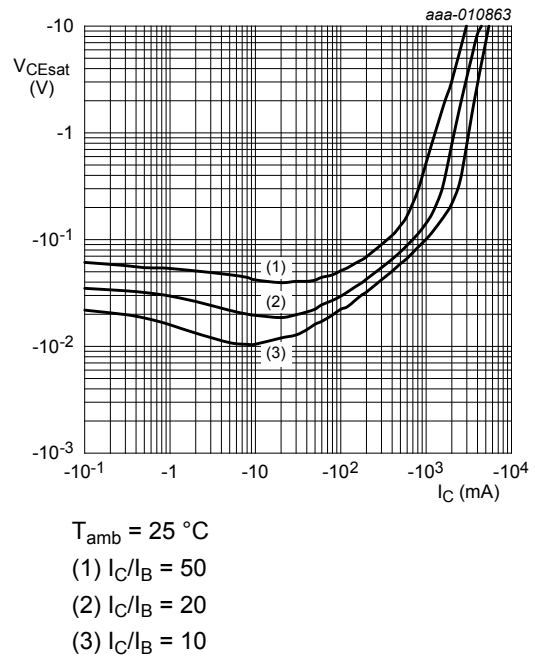


Fig. 9. Collector-emitter saturation voltage as a function of collector current; typical values



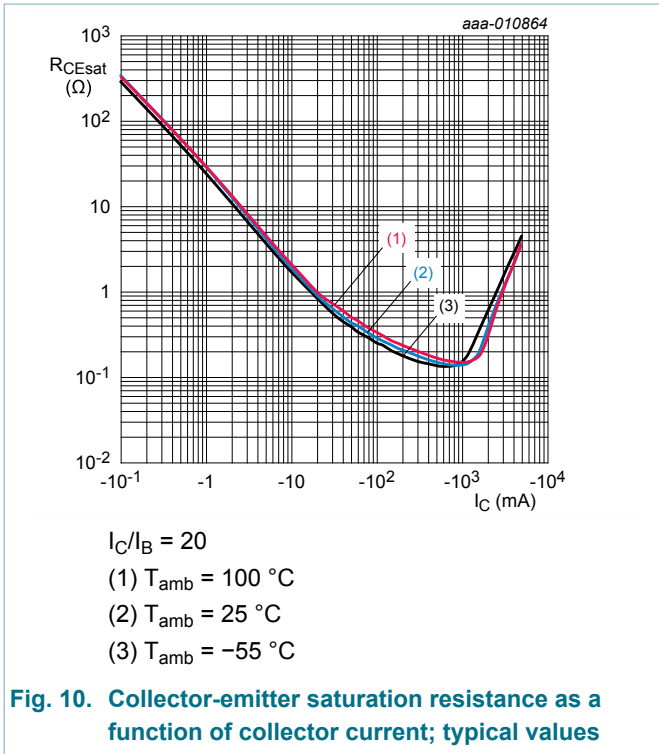


Fig. 10. Collector-emitter saturation resistance as a function of collector current; typical values

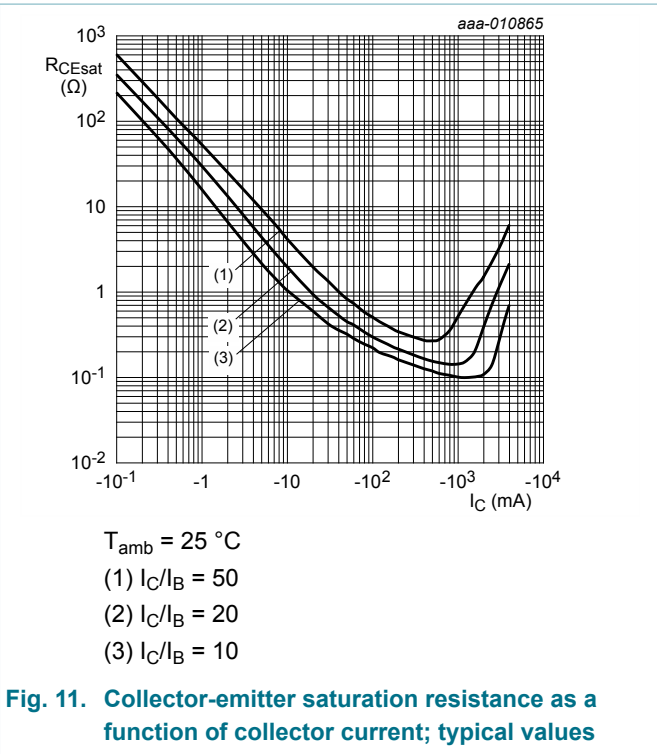


Fig. 11. Collector-emitter saturation resistance as a function of collector current; typical values

### 10. Test information

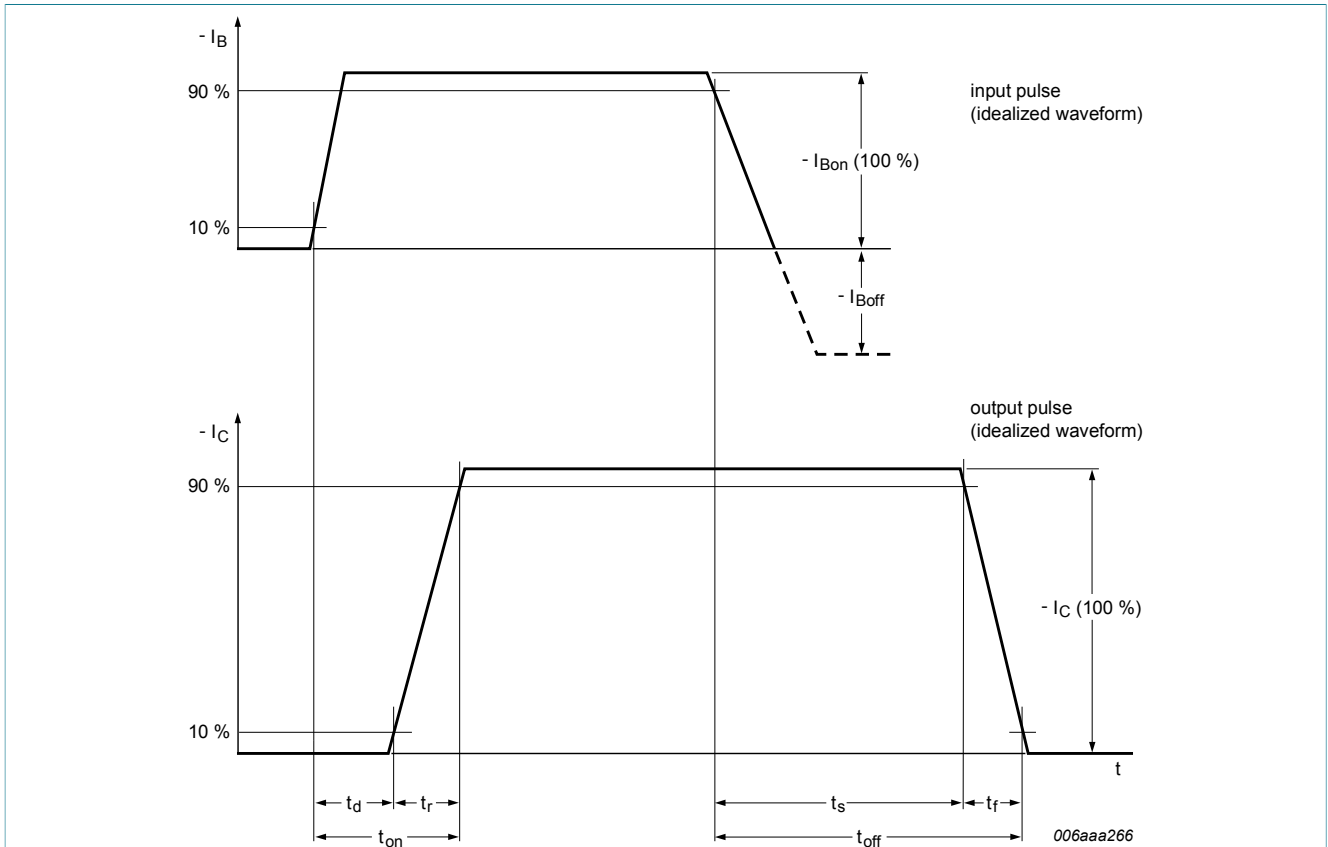


Fig. 12. BISS transistor switching time definition

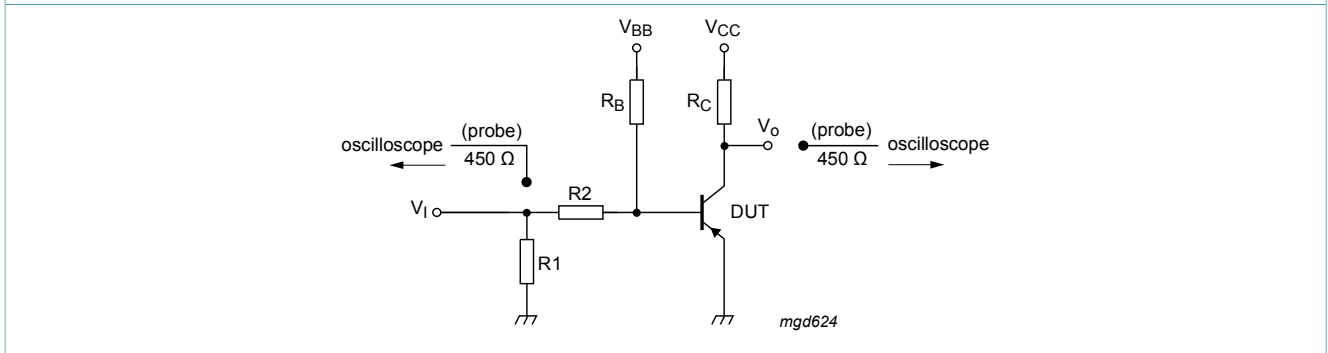


Fig. 13. Test circuit for switching times

#### 10.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

### 11. Package outline

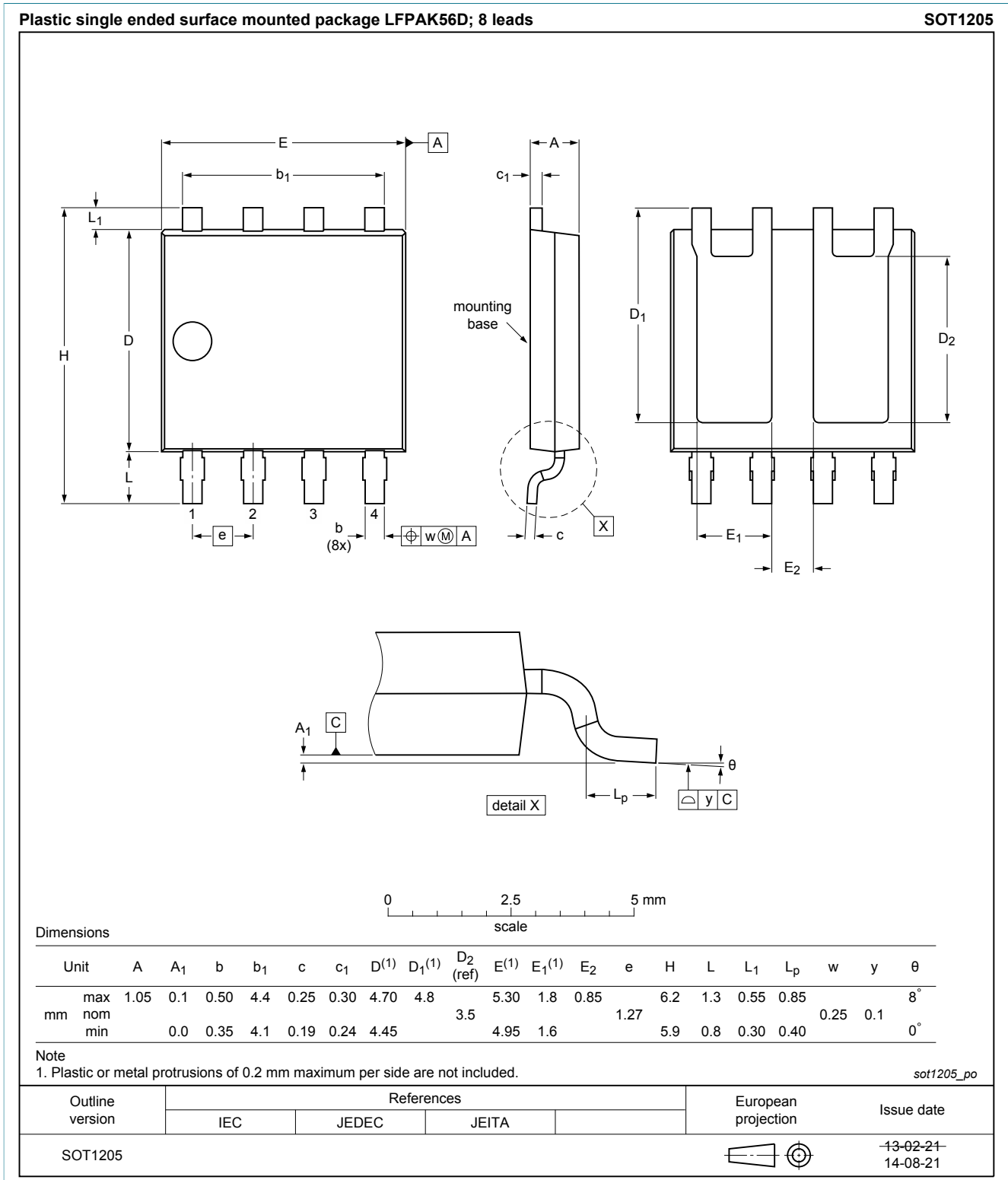


Fig. 14. Package outline LFAK56D (SOT1205)

## 12. Soldering

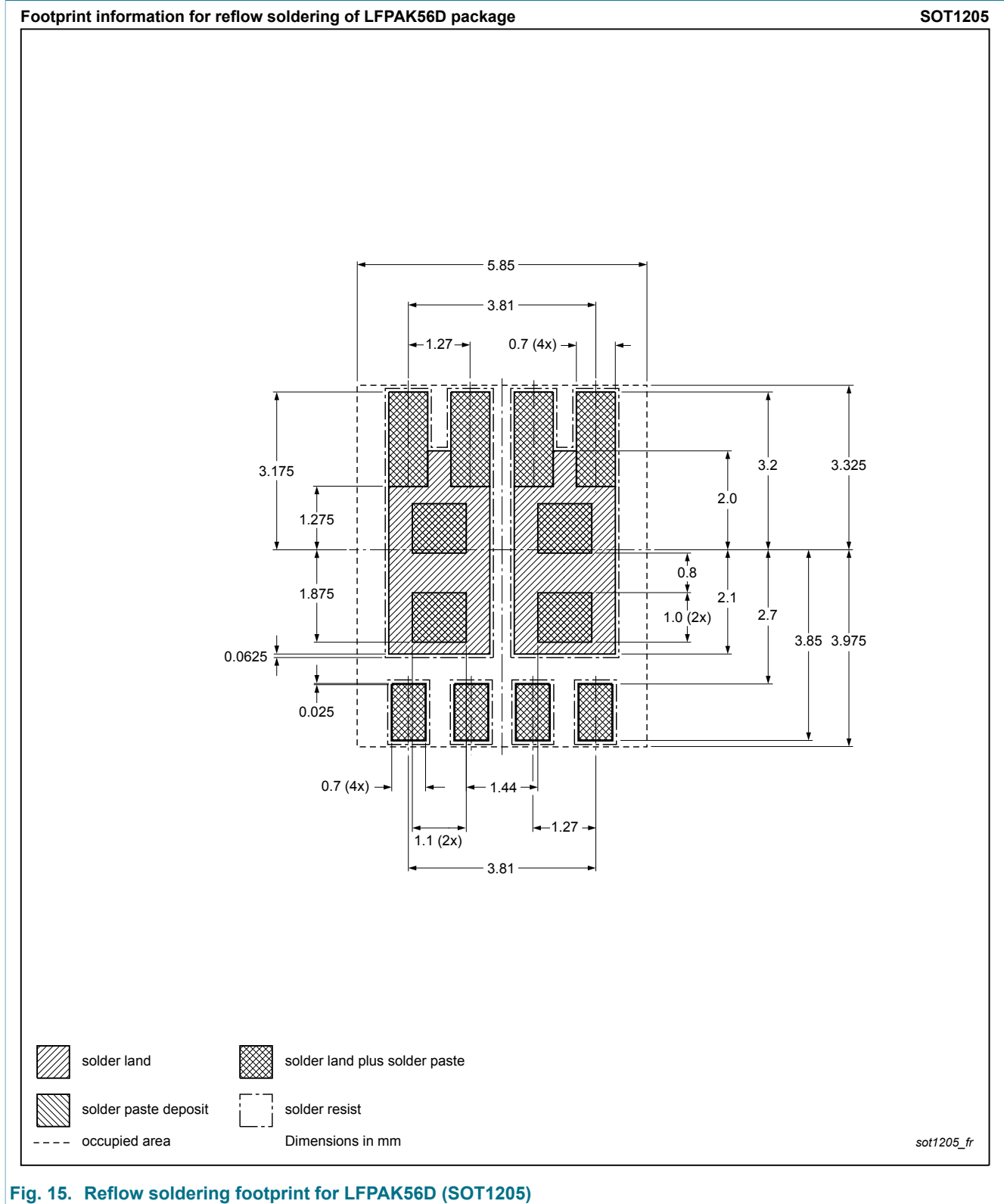


Fig. 15. Reflow soldering footprint for LFPAK56D (SOT1205)

### 13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PHPT610035PK v.1	20141024	Product data sheet	-	-

## 14. Legal information

### 14.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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