NB3N4666C

3.3 V Quad LVCMOS Differential Line Receiver Translator

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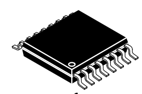
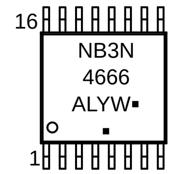


TSSOP−16
DT SUFFIX
CASE 948F

MARKING DIAGRAMS



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

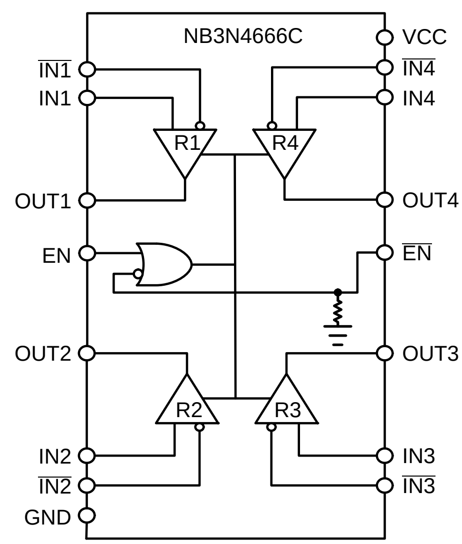


Figure 1. Functional Block Diagram

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

Description

The NB3N4666C is a quad−channel LVDS line receiver/translator offering data rates up to 400 Mbps (200 MHz) and low power consumption. The NB3N4666C receiver incorporates input fail−safe protection circuit that provides a known output voltage under input open−circuit, short and terminated (100 Ω) conditions. The four independent inputs accept differential signals such as: M−LVDS, LVDS, LVPECL and HCSL and translates them to a single−ended, 3.3 V LVCMOS.

The NB3N4666C also offers active high and active low enable/disable inputs (EN and $\overline{EN}$) that allow users to control outputs of all four receivers. These inputs enable or disable the receivers and switch the outputs to an active or high impedance state respectively (see Table 2). The high impedance mode feature helps to reduce the quiescent power consumption to less than 10 mW typical, when the outputs of one or more NB3N4666C devices are multiplexed together.

Features

- Accepts M−LVDS, LVDS, LVPECL and HCSL Differential Input Signal Levels
- Maximum Data Rate of 400 Mbps
- Maximum Clock Frequency of 200 MHz
- 25 ps Typical Channel−to−Channel Skew
- 3.3 ns Maximum Propagation Delay
- 3.3 V ±10% Power Supply
- High Impedance Outputs When Disabled
  - Low Quiescent Power < 10 mW Typical
- Supports Open, Short, and Terminated Input Fail−safe
- −40°C to +85°C Ambient Operating Temperature
- 16−Pin TSSOP, 5.0 mm x 4.4 mm x 1.2 mm
- These are Pb−Free Devices

Applications

- Point−to−point Data Transmission
- Backplane Receivers
- Clock Distribution Networks
- Multidrop Buses

Table 1. PIN DESCRIPTION

Pin TSSOP	Name	I/O	Description
1	$\overline{IN1}$	Input	Receiver Channel 1 Inverted Input.
2	IN1	Input	Receiver Channel 1 Non−inverted Input.
3	OUT1	LVCMOS Output	Receiver Channel 1 Output.
4	EN	Input Enable	Active High Enable. See Table 2 for output enable function.
5	OUT2	LVCMOS Output	Receiver Channel 2 Output.
6	IN2	Input	Receiver Channel 2 Non−inverted Input.
7	$\overline{IN2}$	Input	Receiver Channel 2 Inverted Input.
8	GND	Power	Power Supply Ground (Note 1)
9	$\overline{IN3}$	Input	Receiver Channel 3 Inverted Input.
10	IN3	Input	Receiver Channel 3 Non−inverted Input.
11	OUT3	LVCMOS Output	Receiver Channel 3 Output.
12	$\overline{EN}$	Inverted Input Enable	Active Low Enable. Defaults Low when left open; internal pull−down resistor. See Table 2 for output enable function.
13	OUT4	LVCMOS Output	Receiver Channel 4 Output.
14	IN4	Input	Receiver Channel 4 Non−inverted Input.
15	$\overline{IN4}$	Input	Receiver Channel 4 Inverted Input.
16	V_{CC}	Power	3.3 V ±10% Positive Supply Voltage (Note 1)

1. All V_{CC} and GND pins must be externally connected to a power supply for proper operation. Bypass each supply pin with 0.01 μF to GND.

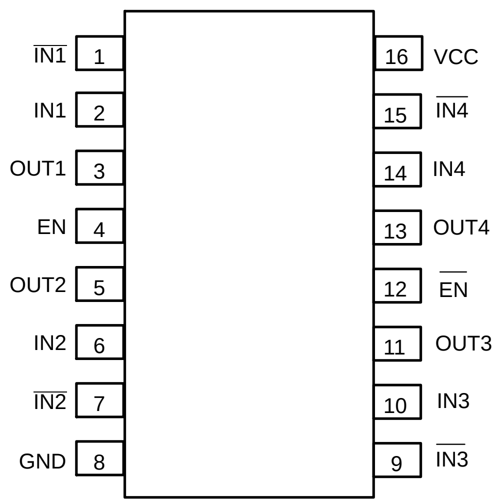


Figure 2. TSSOP−16 Pinout (Top View)

Table 2. OUTPUT ENABLE FUNCTION

ENABLES		INPUTS	OUTPUT
EN	$\overline{EN}$	IN, $\overline{IN}$	OUT
L	H	X	Z
All other combinations of ENABLE inputs		$V_{ID} \geq 100$ mV	H
		$V_{ID} \leq -100$ mV	L
		Full Fail−safe OPEN/SHORT or Terminated	H

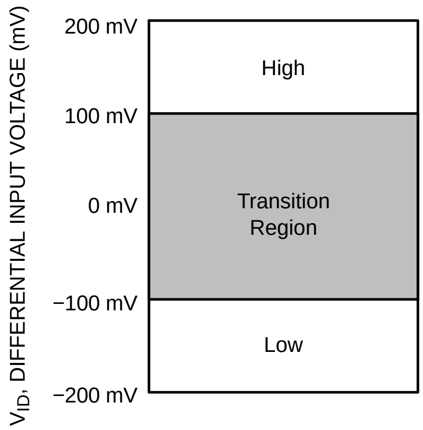


Figure 3. Receiver Differential Input Voltage Showing Transition Region

Table 3. ATTRIBUTES (Note 2)

Characteristics		Value
ESD Protection	Human Body Model	6 kV
	Charged Device Model	500 V
C_{IN} − Input Capacitance		4 pF typical
R_{IN} − Input Impedance		> 10 kΩ
R_{PD} − Inverted Input Enable Pull−down Resistor		800 kΩ
Moisture Sensitivity		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		621
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

2. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Supply Voltage Range	GND = 0 V		4.6	V
V_{IN}	Input Voltage Range	GND = 0 V		−0.5 to VCC +0.5	V
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm	TSSOP−16	138	°C/W
		500 lfpm	TSSOP−16	108	
θ_{JC}	Thermal Resistance (Junction−to−Case)	2S2P	TSSOP−16	33−36	°C/W
T_{sol}	Wave Solder (Pb−Free)			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 5. DC CHARACTERISTICS (V_{CC} = 3.3 V ± 10%; T_A = −40°C to +85°C)

Symbol	Characteristic	Min	Typ	Max	Unit
POWER SUPPLY					
V_{CC}	Power Supply Voltage	2.97	3.30	3.63	V
I_{CC}	No Load Supply, All Receivers Enabled (EN = V_{CC}, $\overline{EN}$ = GND, inputs open)		10	15	mA
I_{CCZ}	No Load Supply, All Receivers Disabled (EN = GND and $\overline{EN}$ = V_{CC}, inputs open)		3	5.5	mA
P_D	Power Dissipation (Note 6)			300	mW
LVCMOS OUTPUTS					
V_{OH}	Output High Voltage I_{OH} = −0.4 mA, V_{ID} = +200 mV I_{OH} = −0.4 mA, Input Terminated (100 Ω Across Differential Inputs) I_{OH} = −0.4 mA, Input Shorted	2.7 2.7 2.7	3.0 3.0 3.0		V
V_{OL}	Output Low Voltage I_{OL} = 2 mA, V_{ID} = −200 mV	GND	0.1	0.25	V
I_{OS}	Output Short Circuit Current (Note 4) Outputs enabled, V_{OUT} = 0 V	−15	−48	−120	mA
I_{OZ}	Output Off State Current Outputs disabled, V_{OUT} = 0 V or V_{CC}	−10	±1	+10	μA
CONTROL INPUTS (EN, $\overline{EN}$)					
V_{IH}	Input HIGH Voltage V_{CC} = 3.3 V	2.0		V_{CC}	V
V_{IL}	Input LOW Voltage V_{CC} = 3.3 V	GND		0.8	V
I_I	Input Current V_{IN} = 0 V or V_{CC}, other input = V_{CC} or 0 V	−10	±1	+10	μA
V_{CL}	Input Clamp Voltage I_{CL} = −18 mA	−1.5	−0.9		V
DIFFERENTIAL INPUTS (IN, $\overline{IN}$)					
V_{CMR}	Input Common Mode Range V_{ID} = 200 mV peak to peak; Differential Input Voltage (V_{ID}) (Notes 3 and 5) (Figures 6 and 7)	0.1		2.3	V
I_{IN}	Input Current V_{IN} = +2.8 V, V_{CC} = 3.6 V or 0 V V_{IN} = 0 V, V_{CC} = 3.6 V or 0 V V_{IN} = +3.63 V, V_{CC} = 0 V	−25 −30 −30	±1 ±1	+25 +30 +30	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

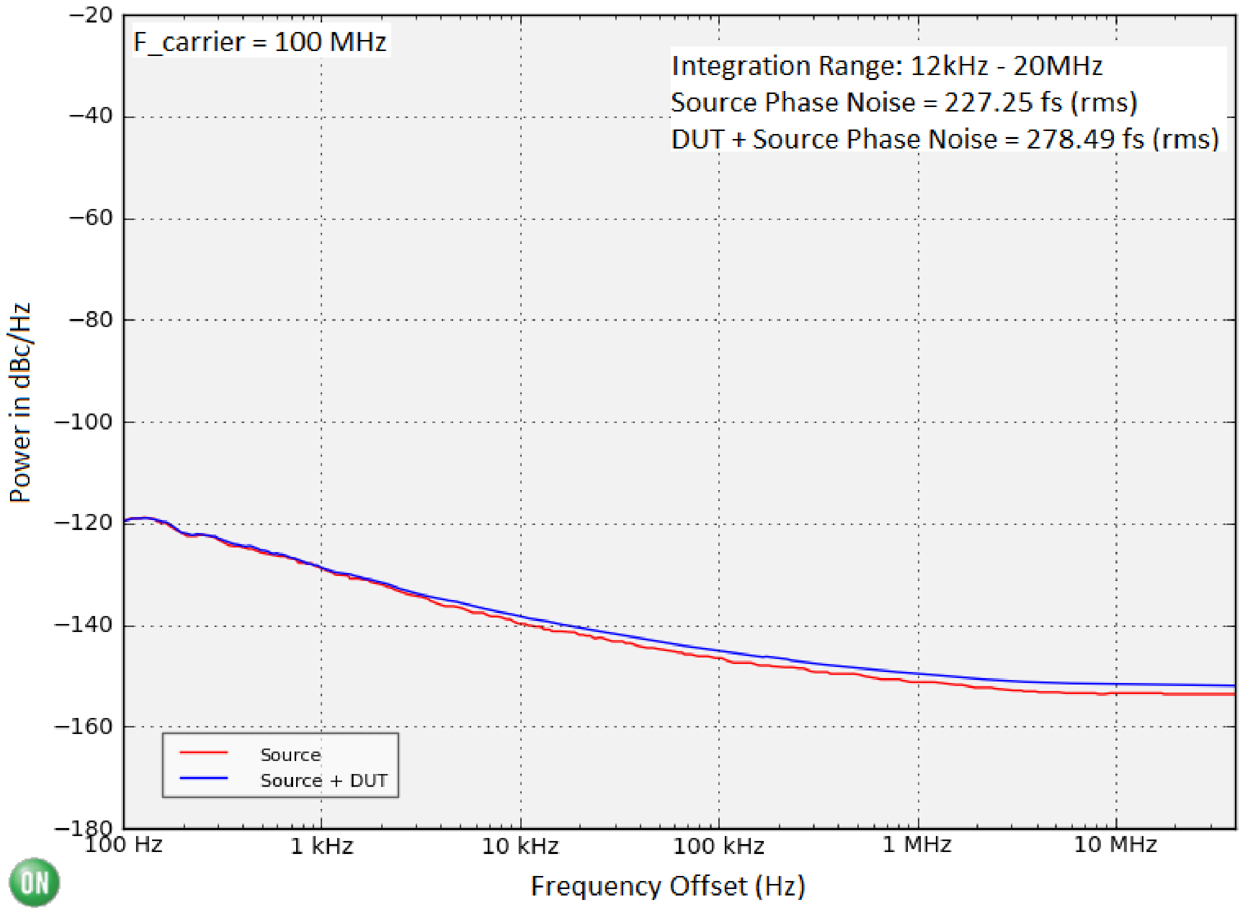
3. Guaranteed by design and characterization. Not tested in production.
4. Output short−circuit current (I_{OS}) is specified as magnitude only; a minus sign indicates direction only. Note that only one output should be shorted at a time; do not exceed the maximum junction temperature specification (150°C).
5. The V_{CMR} range is reduced for larger V_{ID}. Example: if V_{ID} = 400 mV, the V_{CMR} is 0.2 V to 2.2 V. The fail−safe condition with inputs shorted is valid over a common−mode range of 0 V to 2.3 V. A V_{ID} up to V_{CC} may be applied to the IN/$\overline{IN}$ inputs with the Common−Mode voltage set to V_{CC}/2. Propagation delay and Differential Pulse skew decrease when V_{ID} is increased from 200 mV to 400 mV. Skew specifications apply for 200 mV ≤ V_{ID} ≤ 800 mV over the common−mode range.
6. Tested with 100 MHz input frequency on all channels, EN = V_{CC}, $\overline{EN}$ = GND.

Table 6. AC CHARACTERISTICS (V_{CC} = 3.3 V ± 10%; T_A = −40°C to +85°C) (Note 7)

Symbol	Characteristic	Min	Typ	Max	Unit
f_{MAX}	Maximum Input Clock Frequency (Note 8) All Channels Switching	200	250		MHz
$f_{DATAMAX}$	Maximum Data Rate	400			Mbps
t_{plh}/t_{phl}	Propagation Delay (Note 9) (Figures 5 and 8)	1.8		3.3	ns
$t_{SKEW(o-o)}$	Channel−to−channel Skew (Note 10)	0	25	250	ps
$t_{SKEW(pp)}$	Part−to−part Skew (Note 11)		50	500	ps
$t_{SKEW(p)}$	Pulse Skew $\lvert t_{PHL} - t_{PLH} \rvert$, VCM = $V_{CC}/2$ (Note 12) (Figures 5 and 8)	0	50	300	ps
t_r/t_f	Output Rise/Fall Time, 20% − 80% (Figures 5 and 8)		600	1200	ps
T_{jit} (ϕ)	Additive RMS Phase Jitter Integration Range: 12 kHz − 20 MHz, f_c = 100 MHz, 25°C, V_{CC} = 3.3 V		161		fs
t_{plz}/t_{phz}	Output Disable Time (Figures 9 and 10) R_L = 2 kΩ		10	14	ns
t_{pzl}/t_{pzh}	Output Enable Time (Figures 9 and 10) R_L = 2 kΩ		2	5	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Generator waveform for all tests, unless otherwise specified: f = 50 MHz, C_L = 10 pF (includes jig capacitance), tr and tf (10% to 90%) ≤ 2 ns for INx/$\overline{INx}$.
8. f_{MAX} generator input conditions: $t_r = t_f$ < 1ns (10% to 90%), 50% duty cycle, differential (1.05 V to 1.35 V peak to peak). Output Criteria: 40% − 60% duty cycle, V_{OL} (max 0.4 V), V_{OH} (min 2.7 V), C_L = 10 pF (stray plus probes)
9. Measured from the differential crosspoint of the input to $V_{CC}/2$ of the output.
10. $t_{SKEW(O-O)}$ is defined as skew between outputs of the same device at the same supply voltage and with equal load conditions.
11. $t_{SKEW(pp)}$ is defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
12. $t_{SKEW(p)}$ is the magnitude difference in the differential propagation delay time between the positive−going edge and the negative−going edge of the same channel.



The above phase noise data was captured using Agilent E5052A/B. The data displays the input phase noise and output phase noise used to calculate the additive phase jitter at a specified integration range. The additive RMS phase jitter contributed by the device (integrated between 12 kHz and 20 MHz) is 161 fs.

The additive RMS phase jitter performance of the fanout buffer is highly dependent on the phase noise of the input source.

To obtain the most precise additive phase noise measurement, it is vital that the source phase noise be notably lower than that of the DUT. If the phase noise of the source is greater than the noise floor of the device under test, the source noise will dominate the additive phase jitter calculation and lead to an incorrect negative result for the additive phase noise within the integration range. The Figure above is a good example of the NB3N4666C source generator phase noise having a significantly lower floor than the DUT and results in an additive phase jitter of 161 fs.

NB3N4666C Additive RMS Phase Jitter @ 100 MHz
12 kHz to 20 MHz = 161 fs

$$\text{Additive RMS Phase Jitter} = \sqrt{(\text{Source} + \text{DUT})^2 - (\text{Source})^2}$$

$$= \sqrt{(278.49)^2 - (227.25)^2}$$

$$= 161\ \text{fs}$$

Figure 4. Typical Phase Noise Plot at $f_{carrier}$ = 100 MHz at an Operating Voltage of 3.3 V, Room Temperature

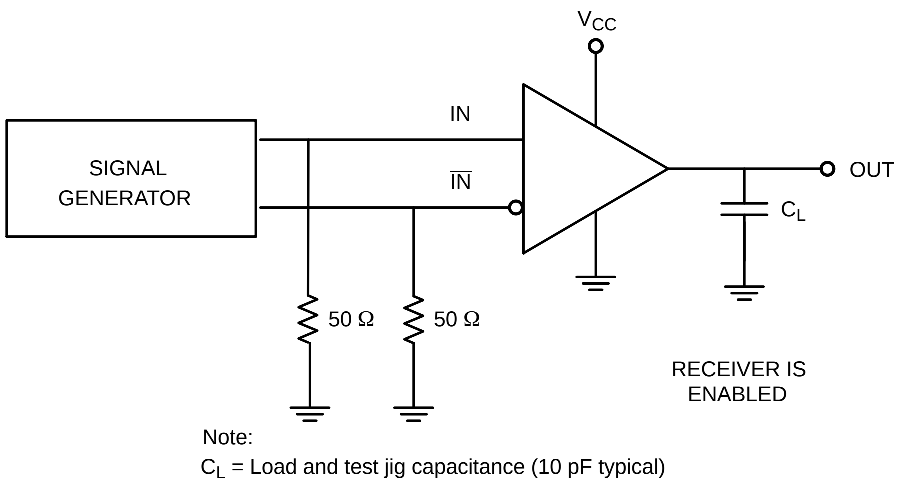


Figure 5. AC Reference Measurement

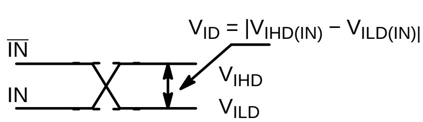


Figure 6. Differential Inputs Driven Differentially

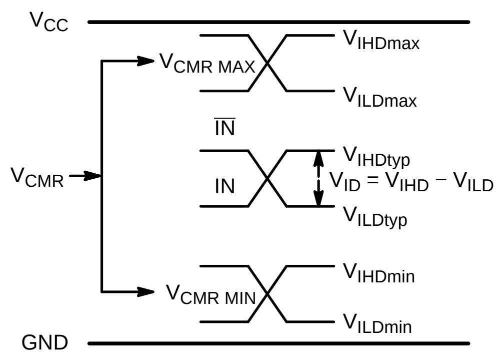


Figure 7. V_{CMR} Diagram

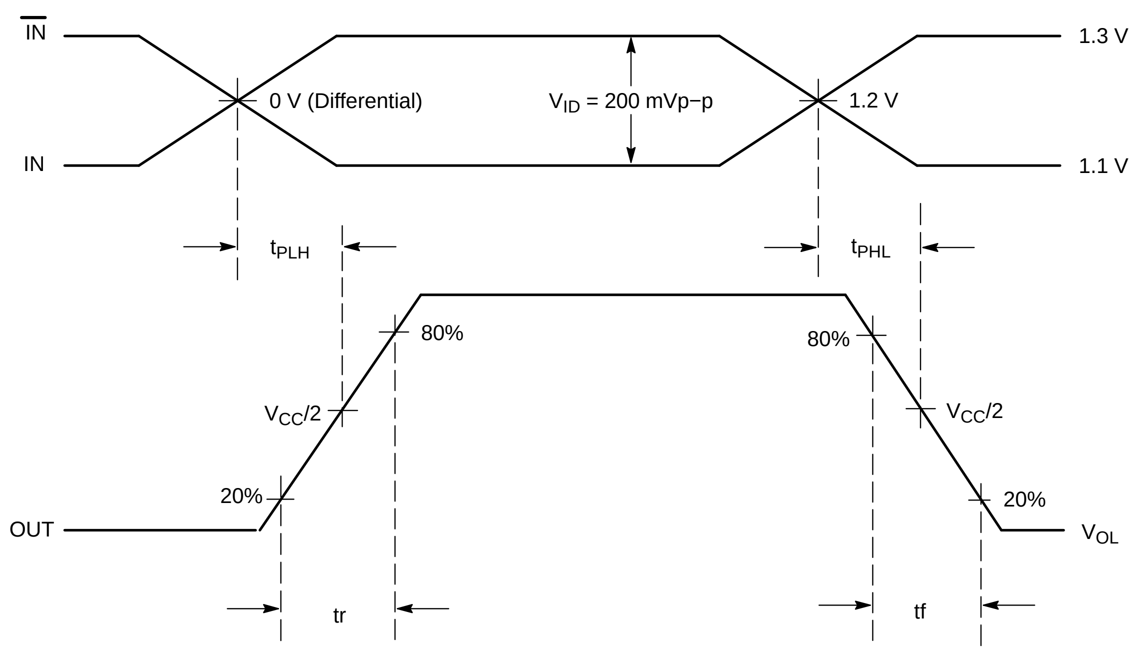
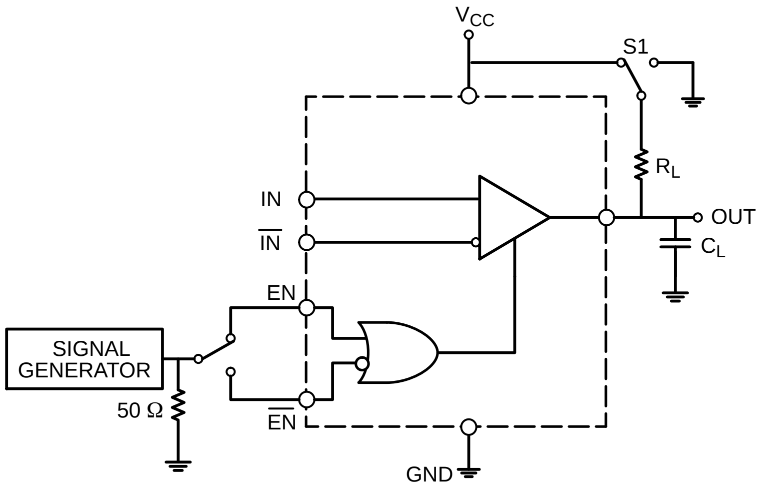


Figure 8. Receiver Propagation Delay, Rise and Fall Time



Notes:
1. C_L = Load and test jig capacitance (10 pF typical).
2. S1 connected to V_{CC} for T_{PZL} and T_{PLZ} measurements.
3. S1 connected to GND for T_{PZH} and T_{PHZ} measurements.

Figure 9. Test Circuit for Receiver Enable/Disable Delay

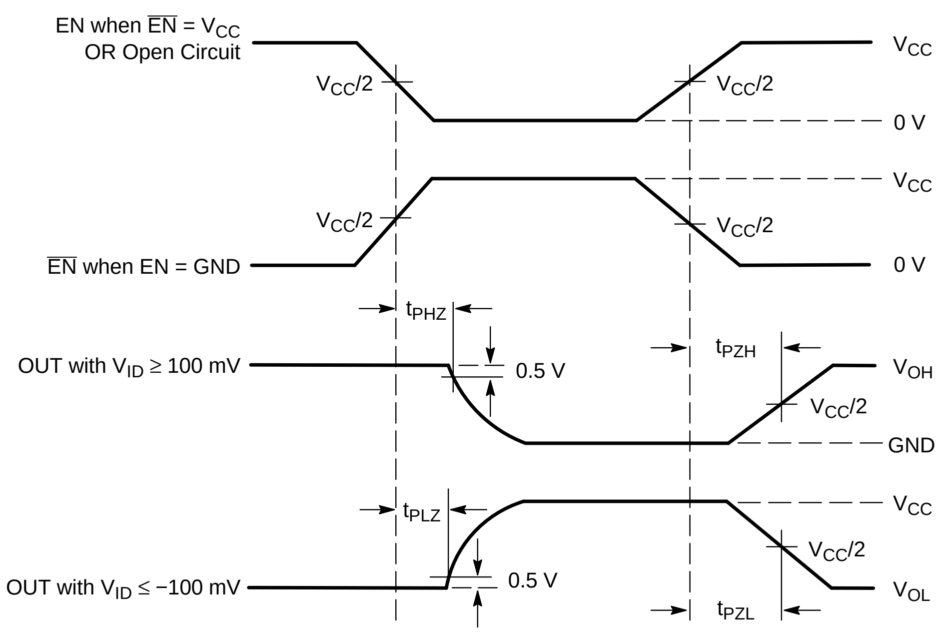


Figure 10. Receiver Enable/Disable Delay Waveform

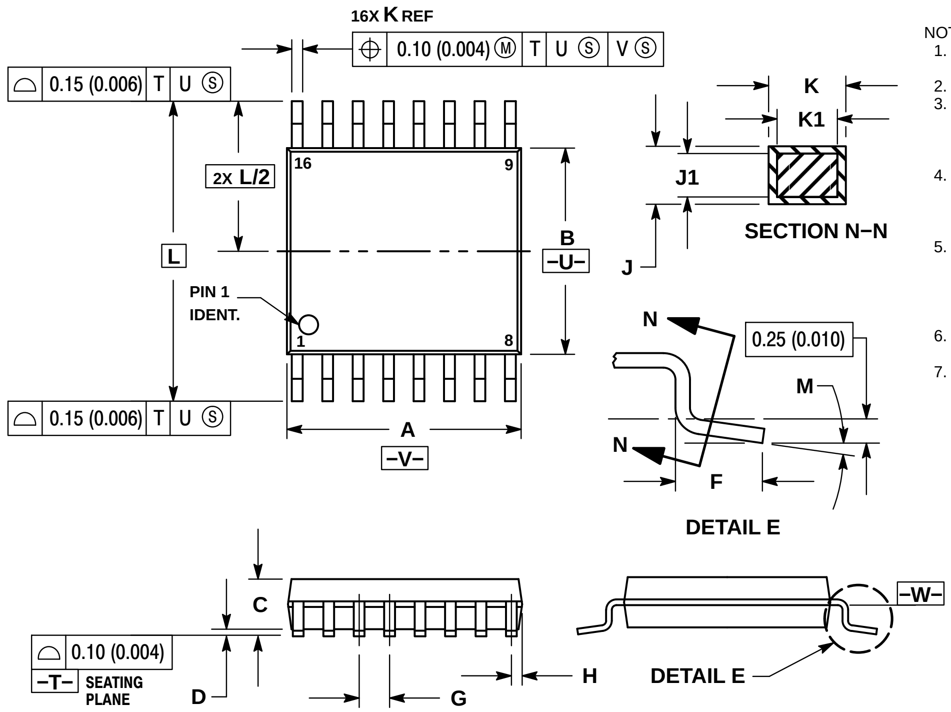
ORDERING INFORMATION

Device	Package	Shipping†
NB3N4666CDTR2G	TSSOP−16 5.0 x 4.4 mm (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

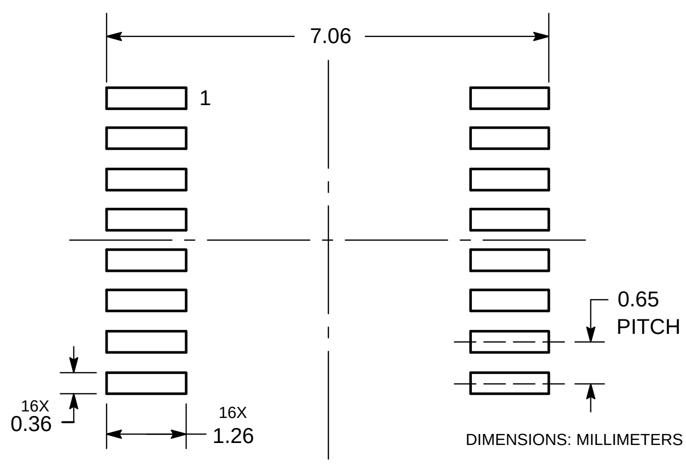
TSSOP−16
CASE 948F−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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