Protected Power MOSFET

2.6 A, 52 V, N-Channel, Logic Level, Clamped MOSFET w/ ESD Protection

Features

- Diode Clamp Between Gate and Source
- ESD Protection Human Body Model 5000 V
- Active Over-Voltage Gate to Drain Clamp
- Scalable to Lower or Higher R_{DS(on)}
- Internal Series Gate Resistance
- These are Pb-Free Devices

Benefits

- High Energy Capability for Inductive Loads
- Low Switching Noise Generation

Applications

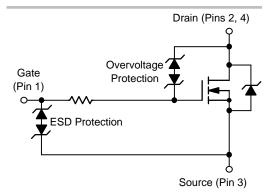
- Automotive and Industrial Markets:
 Solenoid Drivers, Lamp Drivers, Small Motor Drivers
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

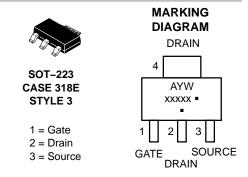


ON Semiconductor®

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V _{DSS} (Clamped)	R _{DS(ON)} TYP	I _D MAX
52 V	95 mΩ @ 10 V	2.6 A





A = Assembly Location

′ = Year

W = Work Week xxxxx = V8440 or 8440A ■ = Pb–Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

MAXIMUM RATINGS ($T_J = 25^{\circ}C$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage Internally Clamped	V_{DSS}	52–59	V
Gate-to-Source Voltage - Continuous	V _{GS}	±15	V
Drain Current - Continuous @ $T_A = 25^{\circ}C$ - Single Pulse ($t_p = 10~\mu s$) (Note 1)	I _D	2.6 10	А
Total Power Dissipation @ T _A = 25°C (Note 1)	P _D	1.69	W
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy (V _{DD} = 50 V, I _{D(pk)} = 1.17 A, V _{GS} = 10 V, L = 160 mH, R _G = 25 Ω)	E _{AS}	110	mJ
Load Dump Voltage (V _{GS} = 0 and 10 V, R _I = $2.0~\Omega$, R _L = $9.0~\Omega$, td = $400~ms$)	V_{LD}	60	V
Thermal Resistance, Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2)	$R_{ hetaJA} \ R_{ hetaJA}$	74 169	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds	TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. When surface mounted to a FR4 board using 1" pad size, (Cu area 1.127 in²).

2. When surface mounted to a FR4 board using minimum recommended pad size, (Cu area 0.412 in²).

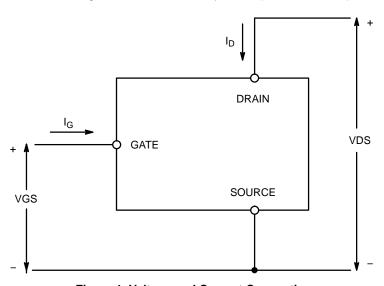


Figure 1. Voltage and Current Convention

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25$ °C unless otherwise noted)

Charac	Symbol	Min	Тур	Max	Unit		
OFF CHARACTERISTICS							
$\begin{array}{c} \textbf{Drain-to-Source Breakdown Voltage (N (V_{GS}=0~V,~I_D=1.0~mA,~T_J=25^{\circ}\text{C})}\\ \textbf{(V}_{GS}=0~V,~I_D=1.0~mA,~T_J=-40^{\circ}\text{C}\\ \textbf{Temperature Coefficient (Negative)} \end{array}$	V _{(BR)DSS}	52 50.8	55 54 –9.3	59 59.5	V V mV/°C		
Zero Gate Voltage Drain Current $(V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V})$ $(V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 125^{\circ}\text{C})$	I _{DSS}			10 25	μΑ		
Gate-Body Leakage Current $(V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V})$ $(V_{GS} = \pm 14 \text{ V}, V_{DS} = 0 \text{ V})$	I _{GSS}		±35	±10	μΑ		
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage (Note 3) $(V_{DS} = V_{GS}, I_D = 100 \mu A)$ Threshold Temperature Coefficient (Neg	gative)	V _{GS(th)}	1.1	1.5 -4.1	1.9	V mV/°C	
	R _{DS(on)}		150 135 95	180 160 110	mΩ		
Forward Transconductance (Note 3) (V _I	_{DS} = 15 V, I _D = 2.6 A)	9FS		3.8		Mhos	
DYNAMIC CHARACTERISTICS							
Input Capacitance		C _{iss}		155		pF	
Output Capacitance	$V_{DS} = 35 \text{ V}, V_{GS} = 0 \text{ V},$ f = 10 kHz	C _{oss}		60			
Transfer Capacitance		C _{rss}		25			
Input Capacitance		C _{iss}		170		pF	
Output Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 10 kHz	C _{oss}		70			
Transfer Capacitance	-	C _{rss}		30			

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- 3. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.
- 4. Not subject to production testing.5. Switching characteristics are independent of operating junction temperatures.

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25$ °C unless otherwise noted)

Characteristic			Min	Тур	Max	Unit
SWITCHING CHARACTERISTICS (No	ote 5)					
Turn-On Delay Time		t _{d(on)}		375		ns
Rise Time	$V_{GS} = 4.5 \text{ V}, V_{DD} = 40 \text{ V},$	t _r		1525		
Turn-Off Delay Time	$I_D = 2.6 \text{ A}, R_D = 15.4 \Omega$	t _{d(off)}		1530		
Fall Time		t _f		1160		
Turn-On Delay Time		t _{d(on)}		325		ns
Rise Time	V _{GS} = 4.5 V. V _{DD} = 40 V.	t _r		1275		
Turn-Off Delay Time	$V_{GS} = 4.5 \text{ V}, V_{DD} = 40 \text{ V},$ $I_{D} = 1.0 \text{ A}, R_{D} = 40 \Omega$	t _{d(off)}		1860		
Fall Time		t _f		1150		
Turn-On Delay Time		t _{d(on)}		190		ns
Rise Time	V _{GS} = 10 V, V _{DD} = 15 V,	t _r		710		
Turn-Off Delay Time	$I_D = 2.6 \text{ A}, R_D = 5.8 \Omega$	t _{d(off)}		2220		
Fall Time		t _f		1180		
Gate Charge		Q _T		4.5		nC
	$V_{GS} = 4.5 \text{ V}, V_{DS} = 40 \text{ V},$ $I_{D} = 2.6 \text{ A} \text{ (Note 3)}$	Q ₁		0.9		
	15 = 2.6 / (Note 6)	Q ₂		2.6		
Gate Charge		Q _T		3.9		nC
	$V_{GS} = 4.5 \text{ V}, V_{DS} = 15 \text{ V},$ $I_{D} = 1.5 \text{ A} \text{ (Note 3)}$	Q ₁		1.0		
	15 = 1.6 / (Note 6)	Q ₂		1.7		
SOURCE-DRAIN DIODE CHARACTE	RISTICS	•		•		
Forward On-Voltage	$I_S = 2.6 \text{ A}, V_{GS} = 0 \text{ V (Note 3)}$ $I_S = 2.6 \text{ A}, V_{GS} = 0 \text{ V}, T_J = 125^{\circ}\text{C}$	V _{SD}		0.81 0.66	1.5	V
Reverse Recovery Time		t _{rr}		730		ns
	$I_S = 1.5 \text{ A}, V_{GS} = 0 \text{ V},$ $dI_S/dt = 100 \text{ A}/\mu\text{s} \text{ (Note 3)}$	t _a		200		1
	αίζιαι – 100 / γμο (11010 0)	t _b		530		
Reverse Recovery Stored Charge	Q _{RR}		6.3		μC	
ESD CHARACTERISTICS (Note 4)		•	1	•	<u>I</u>	1
Electro-Static Discharge Capability	Human Body Model (HBM)	ESD	5000			V
	Machine Model (MM)	1	500			
	1		<u> </u>			

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- 3. Pulse Test: Pulse Width $\leq 300~\mu s,$ Duty Cycle $\leq 2\%.$
- 4. Not subject to production testing.
- 5. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

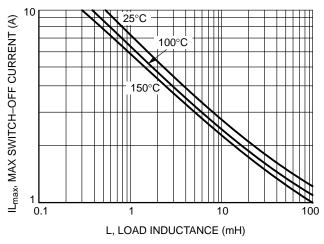


Figure 1. Single Pulse Maximum Switch-off Current vs. Load Inductance

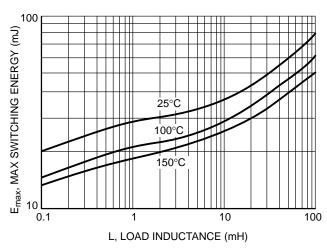
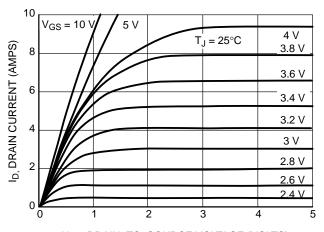


Figure 2. Single Pulse Maximum Switching Energy vs. Load Inductance



V_{DS}, DRAIN-TO-SOURCE VOLTAGE (VOLTS)

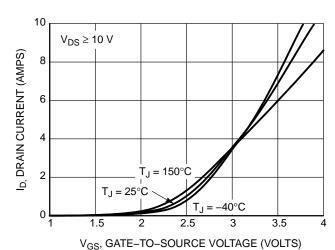


Figure 4. Transfer Characteristics



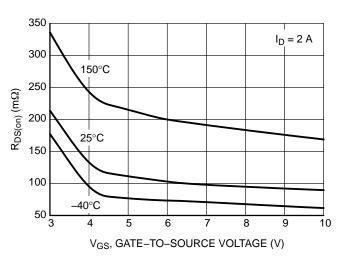


Figure 5. R_{DS(on)} vs. Gate-Source Voltage

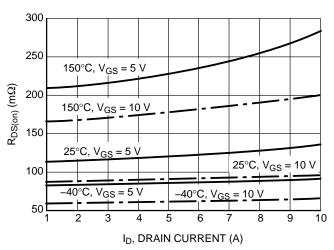


Figure 6. R_{DS(on)} vs. Drain Current

TYPICAL PERFORMANCE CURVES

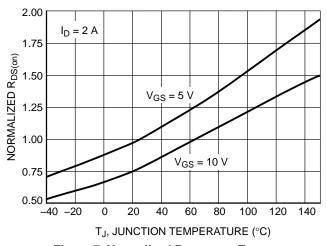


Figure 7. Normalized R_{DS(on)} vs. Temperature

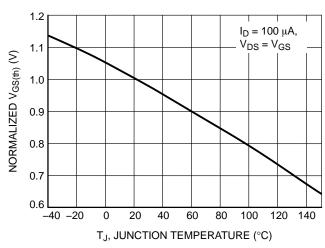


Figure 8. Normalized Threshold Voltage vs.
Temperature

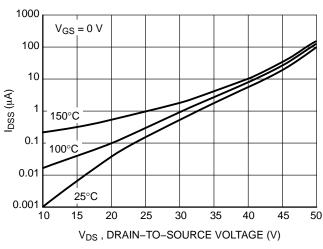


Figure 9. Drain-to-Source Leakage Current

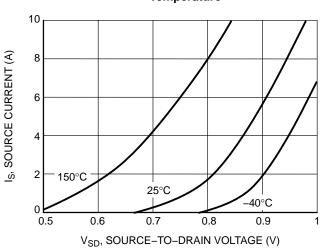
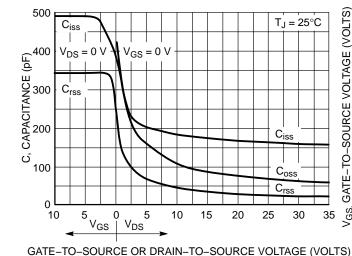


Figure 10. Source–Drain Diode Forward Characteristics



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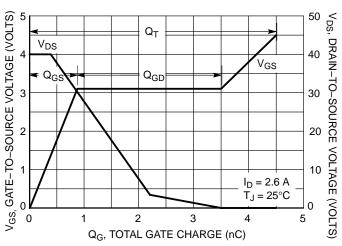


Figure 12. Gate-to-Source Voltage vs. Total Gate Charge

TYPICAL PERFORMANCE CURVES

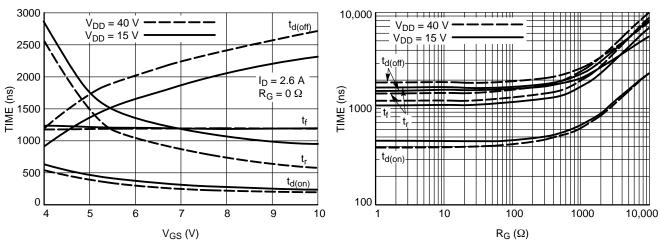


Figure 13. Resistive Load Switching Time vs.
Gate-Source Voltage

Figure 14. Resistive Load Switching Time vs. Gate Resistance ($V_{GS} = 5 \text{ V}, I_D = 2.6 \text{ A}$)

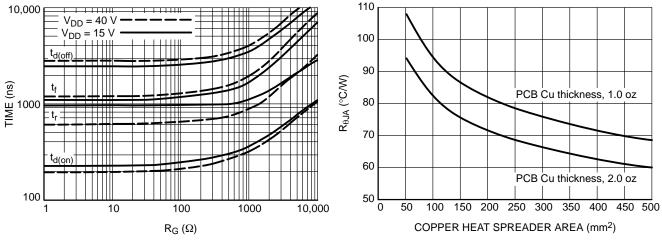


Figure 15. Resistive Load Switching Time vs. Gate Resistance ($V_{GS} = 10 \text{ V}, I_D = 2.6 \text{ A}$)

Figure 16. R_{0JA} vs. Copper Area

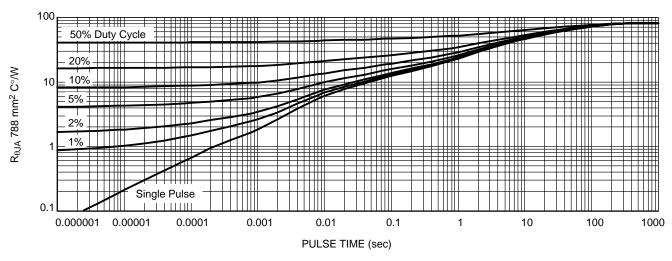


Figure 17. Transient Thermal Resistance

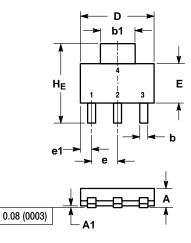
ORDERING INFORMATION

Device	Package	Shipping [†]		
NCV8440STT1G	SOT-223 (Pb-Free)	1000 / Tape & Reel		
NCV8440ASTT1G	SOT-223 (Pb-Free)	1000 / Tape & Reel		
NCV8440STT3G	SOT-223 (Pb-Free)	4000 / Tape & Reel		
NCV8440ASTT3G	SOT-223 (Pb-Free)	4000 / Tape & Reel		

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

SOT-223 (TO-261) CASE 318E-04



ISSUE N

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES			
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
Α	1.50	1.63	1.75	0.060	0.064	0.068	
A1	0.02	0.06	0.10	0.001	0.002	0.004	
b	0.60	0.75	0.89	0.024	0.030	0.035	
b1	2.90	3.06	3.20	0.115	0.121	0.126	
С	0.24	0.29	0.35	0.009	0.012	0.014	
D	6.30	6.50	6.70	0.249	0.256	0.263	
E	3.30	3.50	3.70	0.130	0.138	0.145	
е	2.20	2.30	2.40	0.087	0.091	0.094	
e1	0.85	0.94	1.05	0.033	0.037	0.041	
L	0.20			0.008	-		
L1	1.50	1.75	2.00	0.060	0.069	0.078	
HE	6.70	7.00	7.30	0.264	0.276	0.287	
θ	0°	_	10°	0°	_	10°	

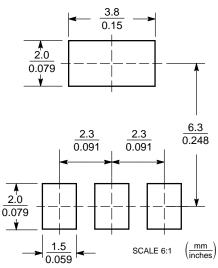
STYLE 3: PIN 1. GATE

2. DRAIN

SOURCE

4. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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