# NSS12200WT1G

# 12 V, 2 A, Low V<sub>CE(sat)</sub> PNP Transistor

ON Semiconductor's e<sup>2</sup>PowerEdge family of low  $V_{CE(sat)}$  transistors are miniature surface mount devices featuring ultra low saturation voltage ( $V_{CE(sat)}$ ) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical application are DC–DC converters and power management in portable and battery powered products such as cellular and cordless phones, PDAs, computers, printers, digital cameras and MP3 players. Other applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e<sup>2</sup>PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

## Features

- High Current Capability (3 A)
- High Power Handling (Up to 650 mW)
- Low V<sub>CE(s)</sub> (170 mV Typical @ 1 A)
- Small Size
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

#### Benefits

- High Specific Current and Power Capability Reduces Required PCB Area
- Reduced Parasitic Losses Increases Battery Life

## **MAXIMUM RATINGS** ( $T_A = 25^{\circ}C$ )

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V <sub>CEO</sub>	-12	Vdc
Collector-Base Voltage	V <sub>CBO</sub>	-12	Vdc
Emitter-Base Voltage	V <sub>EBO</sub>	-5.0	Vdc
Collector Current – Continuous – Peak	I <sub>C</sub> I <sub>CM</sub>	-2.0 -3.0	Adc
Electrostatic Discharge	ESD	HBM Class 3 MM Class C	

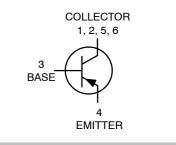
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



## **ON Semiconductor®**

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# $\begin{array}{c} 12 \text{ VOLTS} \\ 2.0 \text{ AMPS} \end{array} \\ \textbf{PNP LOW V}_{\text{CE(sat)}} \text{ TRANSISTOR} \\ \textbf{EQUIVALENT R}_{\text{DS(on)}} \text{ 163 m} \Omega \end{array}$





SC-88/SOT-363 CASE 419B STYLE 20

#### **DEVICE MARKING**



V2 = Specific Device Code

- M = Date Code
- = Pb–Free Package

#### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NSS12200WT1G	SOT-363 (Pb-Free)	3000 / Tape & Reel

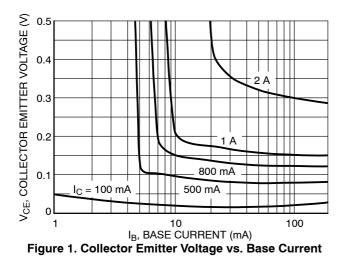
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

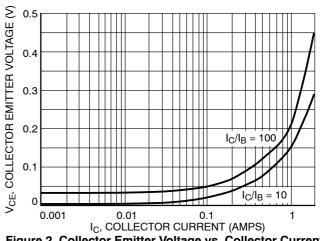
## THERMAL CHARACTERISTICS

Total Device Dissipation $T_A = 25^{\circ}C$ Derate above 25^{\circ}C     Thermal Resistance,     Junction-to-Ambient     Total Device Dissipation $T_A = 25^{\circ}C$ Derate above 25^{\circ}C     Thermal Resistance,     Junction-to-Ambient     Thermal Resistance,     Junction-to-Ambient     Thermal Resistance,     Junction-to-Lead 6	P <sub>D</sub> (Note R <sub>θJA</sub> (Not P <sub>D</sub> (Note R <sub>θJA</sub> (Not R <sub>θJL</sub> P <sub>D</sub> Sing	e 1) 2) e 2)	450 3.6 275 650 5.2 192 105	n	mW nW/°C °C/W mW nW/°C °C/W	
Thermal Resistance,     Junction-to-Ambient     Total Device Dissipation $T_A = 25^{\circ}C$ Derate above $25^{\circ}C$ Thermal Resistance,     Junction-to-Ambient     Thermal Resistance,     Junction-to-Ambient	P <sub>D</sub> (Note	2) e 2)	275 650 5.2 192	n	°C/W mW nW/°C	
T <sub>A</sub> = 25°C Derate above 25°C Thermal Resistance, Junction-to-Ambient Thermal Resistance,	R <sub>θJA</sub> (Not	e 2)	5.2 192		ı₩/°C	
Thermal Resistance, Junction-to-Ambient Thermal Resistance,	R <sub>θJL</sub>		192			
			105			
	P <sub>D</sub> Sing			Ň	°C/W	
Total Device Dissipation (Single Pulse < 10 sec.)		ie	1.4		W	
Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>		–55 to +15	0	°C	
<b>ELECTRICAL CHARACTERISTICS</b> ( $T_J = 25^{\circ}C$ unless otherwise not			1	1		
Characteristic	Symbol	Min	Тур	Мах	Unit	
OFF CHARACTERISTICS						
Collector – Emitter Breakdown Voltage, ( $I_C = -10 \text{ mAdc}$ , $I_B = 0$ )	V <sub>(BR)CEO</sub>	-12	-15	-	Vdc	
Collector – Base Breakdown Voltage, ( $I_{C} = -0.1 \text{ mAdc}, I_{E} = 0$ )	V <sub>(BR)CBO</sub>	-12	-25	-	Vdc	
Emitter – Base Breakdown Voltage, ( $I_E = -0.1 \text{ mAdc}, I_C = 0$ )	V <sub>(BR)EBO</sub>	-5.0	-7.0	-	Vdc	
Collector Cutoff Current, (V <sub>CB</sub> = $-12$ Vdc, I <sub>E</sub> = 0)	I <sub>CBO</sub>	-	-0.02	-0.1	μAdc	
Collector–Emitter Cutoff Current, ( $V_{CES} = -12 \text{ Vdc}$ , $I_E = 0$ )	I <sub>CES</sub>	-	-0.03	-0.1	μAdc	
Emitter Cutoff Current, (V <sub>EB</sub> = $-5.0$ Vdc, I <sub>E</sub> = 0)	I <sub>EBO</sub>	_	-0.03	-0.1	μAdc	
ON CHARACTERISTICS						
DC Current Gain (Note 3) ( $I_C = -0.5 A$ , $V_{CE} = -1.5 V$ ) ( $I_C = -0.8 A$ , $V_{CE} = -1.5 V$ ) ( $I_C = -1.0 A$ , $V_{CE} = -1.5 V$ )	h <sub>FE</sub>	100 100 100	180 165 160	_ 300 _		
Collector – Emitter Saturation Voltage (Note 3) ( $I_C = -0.5 \text{ A}, I_B = -10 \text{ mA}$ ) ( $I_C = -0.8 \text{ A}, I_B = -16 \text{ mA}$ ) ( $I_C = -1.0 \text{ A}, I_B = -20 \text{ mA}$ )	V <sub>CE(sat)</sub>		-0.10 -0.14 -0.17	-0.160 -0.235 -0.290	V	
Base – Emitter Saturation Voltage (Note 3) $(I_C = -1.0 \text{ A}, I_B = -20 \text{ mA})$	V <sub>BE(sat)</sub>	-	-0.84	-0.95	V	
Base – Emitter Turn–on Voltage (Note 3) ( $I_C = -1.0 \text{ A}, V_{CE} = -1.5 \text{ V}$ )	V <sub>BE(on)</sub>	-	-0.81	-0.95	V	
Cutoff Frequency ( $I_C = -100 \text{ mA}, V_{CE} = -5.0 \text{ V}, f = 100 \text{ MHz}$ )	fT	-	100	_	MHz	
Output Capacitance ( $V_{CB} = -1.5 \text{ V}, \text{ f} = 1.0 \text{ MHz}$ )	C <sub>obo</sub>	_	50	65	pF	

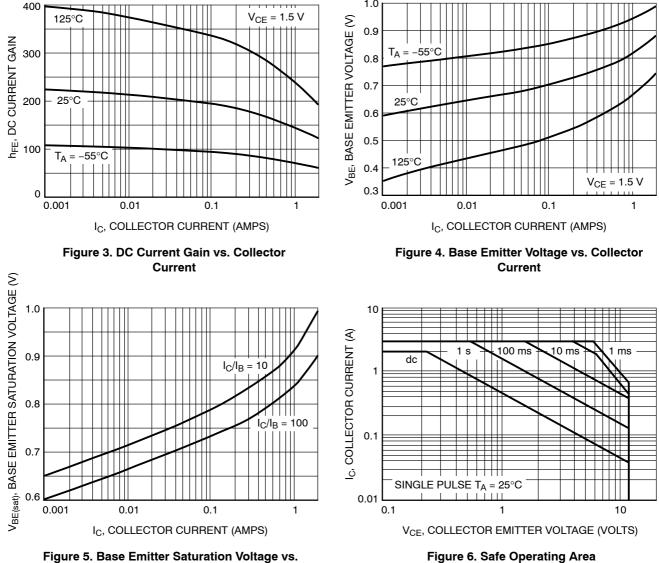
FR-4, Minimum Pad, 1 oz Coverage.
FR-4, 1" Pad, 1 oz Coverage.
Pulsed Condition: Pulse Width < 300 μsec, Duty Cycle < 2%.</li>

1.0









**Base Current** 

# NSS12200WT1G

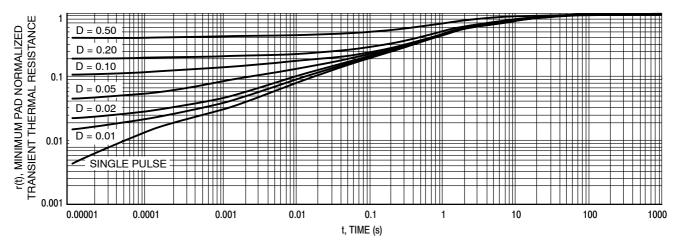


Figure 7. Normalized Thermal Response

#### PACKAGE DIMENSIONS

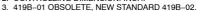
#### SC-88/SC70-6/SOT-363

CASE 419B-02 **ISSUE W** 

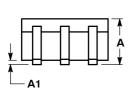
NOTES

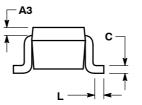
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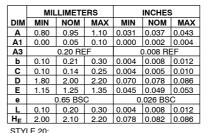
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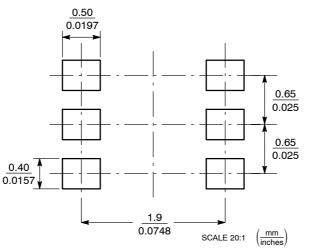
PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER



COLLECTOR 5.

6. COLLECTOR

#### **SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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