# NPN Silicon Planar Epitaxial Transistor

This NPN Silicon Epitaxial transistor is designed for use in industrial and consumer applications. The device is housed in the SOT–223 package which is designed for medium power surface mount applications.

SOT-223 package ensures level mounting, resulting in improved thermal conduction, and allows visual inspection of soldered joints. The formed leads absorb thermal stress during soldering, eliminating the possibility of damage to the die.

### **Features**

- High Current
- The SOT-223 Package can be Soldered Using Wave or Reflow
- Available in 12 mm Tape and Reel
  - Use PZT651T1G to Order the 7 inch/1000 Unit Reel
  - Use PZT651T3G to Order the 13 inch/4000 Unit Reel
- PNP Complement is PZT751T1G
- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant\*

### **MAXIMUM RATINGS** (T<sub>C</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V <sub>CEO</sub>	60	Vdc
Collector-Base Voltage	V <sub>CBO</sub>	80	Vdc
Emitter-Base Voltage	V <sub>EBO</sub>	5.0	Vdc
Collector Current	I <sub>C</sub>	2.0	Adc
Total Power Dissipation  @ T <sub>A</sub> = 25°C (Note 1)  Derate above 25°C	P <sub>D</sub>	0.8 6.4	W mW/°C
Storage Temperature Range	T <sub>stg</sub>	-65 to 150	°C
Junction Temperature	TJ	150	°C

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance from Junction-to-Ambient in Free Air	$R_{\theta JA}$	156	°C/W
Maximum Temperature for Soldering Purposes Time in Solder Bath	T <sub>L</sub>	260 10	°C Sec

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

 Device mounted on a FR-4 glass epoxy printed circuit board using minimum recommended footprint.



## ON Semiconductor®

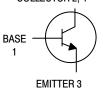
www.onsemi.com

# SOT-223 PACKAGE HIGH CURRENT NPN SILICON TRANSISTOR SURFACE MOUNT

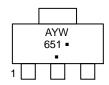


SOT-223 CASE 318E-04 STYLE 1

COLLECTOR 2, 4



### **MARKING DIAGRAM**



A = Assembly Location

Y = Year

WW = Work Week
■ = Pb–Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
PZT651T1G	SOT-223 (Pb-Free)	1,000 / Tape & Reel
SPZT651T1G	SOT-223 (Pb-Free)	1,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

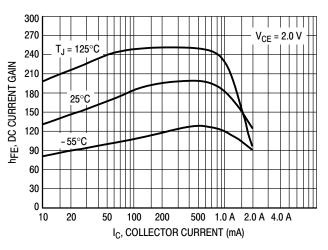
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting

# **ELECTRICAL CHARACTERISTICS** ( $T_A = 25^{\circ}C$ unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage $(I_C = 10 \text{ mAdc}, I_B = 0)$	V <sub>(BR)</sub> CEO	60	-	Vdc
Collector–Emitter Breakdown Voltage ( $I_C = 100 \mu Adc, I_E = 0$ )	V <sub>(BR)</sub> CBO	80	-	Vdc
Emitter–Base Breakdown Voltage ( $I_E = 10 \mu Adc, I_C = 0$ )	V <sub>(BR)EBO</sub>	5.0	_	Vdc
Base–Emitter Cutoff Current (V <sub>EB</sub> = 4.0 Vdc)	I <sub>EBO</sub>	-	0.1	μAdc
Collector–Base Cutoff Current (V <sub>CB</sub> = 80 Vdc, I <sub>E</sub> = 0)	I <sub>CBO</sub>	-	100	nAdc
ON CHARACTERISTICS (Note 2)			•	•
DC Current Gain $ \begin{aligned} &(I_C = 50 \text{ mAdc},  V_{CE} = 2.0 \text{ Vdc}) \\ &(I_C = 500 \text{ mAdc},  V_{CE} = 2.0 \text{ Vdc}) \\ &(I_C = 1.0 \text{ Adc},  V_{CE} = 2.0 \text{ Vdc}) \\ &(I_C = 2.0 \text{ Adc},  V_{CE} = 2.0 \text{ Vdc}) \end{aligned} $	h <sub>FE</sub>	75 75 75 40	- - - -	-
Collector–Emitter Saturation Voltages $(I_C = 2.0 \text{ Adc}, I_B = 200 \text{ mAdc})$ $(I_C = 1.0 \text{ Adc}, I_B = 100 \text{ mAdc})$	V <sub>CE(sat)</sub>	- -	0.5 0.3	Vdc
Base–Emitter Voltages (I <sub>C</sub> = 1.0 Adc, V <sub>CE</sub> = 2.0 Vdc)	V <sub>BE(on)</sub>	-	1.0	Vdc
Base–Emitter Saturation Voltage (I <sub>C</sub> = 1.0 Adc, I <sub>B</sub> = 100 mAdc)	V <sub>BE(sat)</sub>	-	1.2	Vdc
Current–Gain — Bandwidth (I <sub>C</sub> = 50 mAdc, V <sub>CE</sub> = 5.0 Vdc, f = 100 MHz)	f⊤	75	-	MHz

<sup>2.</sup> Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2.0%

# **TYPICAL CHARACTERISTICS**



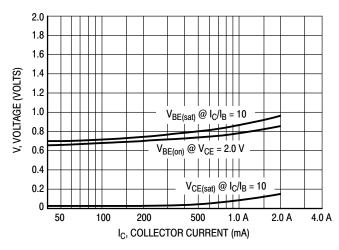


Figure 1. Typical DC Current Gain

Figure 2. On Voltages

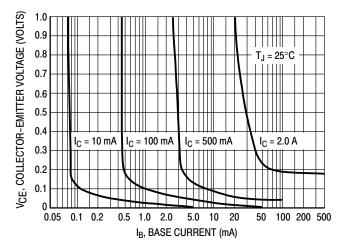
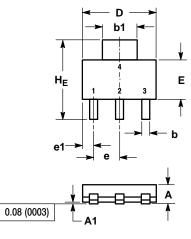


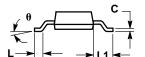
Figure 3. Collector Saturation Region

### PACKAGE DIMENSIONS

# SOT-223 (TO-261)

CASE 318E-04 **ISSUE N** 





NOTES:

DIMENSIONING AND TOLERANCING PER ASME Y14.5M,

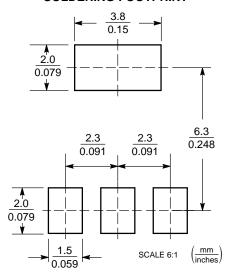
	CONTROLL	NG DIMENS	ION: INCH.			
	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
Α	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
С	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
е	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L	0.20			0.008		
L1	1.50	1.75	2.00	0.060	0.069	0.078
HE	6.70	7.00	7.30	0.264	0.276	0.287
A	0°	_	10°	0°	_	10°

STYLE 1: PIN 1. BASE

2. COLLECTOR 3. EMITTER

4. COLLECTOR

#### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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