# PNP Silicon Planar Epitaxial Transistor

This PNP Silicon Epitaxial transistor is designed for use in industrial and consumer applications. The device is housed in the SOT–223 package which is designed for medium power surface mount applications.

### Features

- High Current
- The SOT-223 Package can be soldered using wave or reflow.
- SOT-223 Package Ensures Level Mounting, Resulting in Improved Thermal Conduction, and Allows Visual Inspection of Soldered Joints. The Formed Leads Absorb Thermal Stress During Soldering, Eliminating the Possibility of Damage to the Die
- NPN Complement is PZT651T1G
- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q101 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant\*

#### MAXIMUM RATINGS (T<sub>C</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V <sub>CEO</sub>	-60	Vdc
Collector-Base Voltage	V <sub>CBO</sub>	-80	Vdc
Emitter-Base Voltage	V <sub>EBO</sub>	-5.0	Vdc
Collector Current	Ι <sub>C</sub>	-2.0	Adc
Total Power Dissipation @ T <sub>A</sub> = 25°C (Note 1) Derate above 25°C	P <sub>D</sub>	0.8 6.4	W mW/°C
Storage Temperature Range	T <sub>stg</sub>	-65 to 150	°C
Junction Temperature	TJ	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Device mounted on a FR-4 glass epoxy printed circuit board using minimum recommended footprint.

### THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance from Junction-to- Ambient in Free Air	$R_{\thetaJA}$	156	°C/W
Maximum Temperature for Soldering Purposes	ΤL	260	°C
Time in Solder Bath		10	Sec

\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

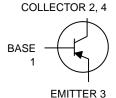


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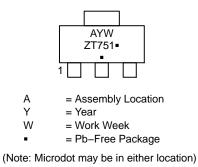
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## SOT-223 PACKAGE HIGH CURRENT NPN SILICON TRANSISTOR SURFACE MOUNT





## MARKING DIAGRAM



### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
PZT751T1G	SOT-223 (Pb-Free)	1,000 / Tape & Reel
SPZT751T1G	SOT-223 (Pb-Free)	1,000 / Tape & Reel

†For information on tape and reel specifications,

including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## PZT751

## **ELECTRICAL CHARACTERISTICS** (T<sub>A</sub> = $25^{\circ}C$ unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage $(I_C = -10 \text{ mAdc}, I_B = 0)$	V <sub>(BR)CEO</sub>	-60	_	Vdc
Collector–Emitter Breakdown Voltage $(I_C = -100 \ \mu Adc, I_E = 0)$	V <sub>(BR)CBO</sub>	-80	-	Vdc
Emitter–Base Breakdown Voltage $(I_E = -10 \ \mu Adc, I_C = 0)$	V <sub>(BR)EBO</sub>	-5.0	_	Vdc
Base–Emitter Cutoff Current (V <sub>EB</sub> = -4.0 Vdc)	I <sub>EBO</sub>	_	-0.1	μAdc
Collector–Base Cutoff Current ( $V_{CB} = -80 \text{ Vdc}, I_E = 0$ )	Ісво	_	-100	nAdc
ON CHARACTERISTICS (Note 2)				
DC Current Gain ( $I_C = -50 \text{ mAdc}, V_{CE} = -2.0 \text{ Vdc}$ ) ( $I_C = -500 \text{ mAdc}, V_{CE} = -2.0 \text{ Vdc}$ ) ( $I_C = -1.0 \text{ Adc}, V_{CE} = -2.0 \text{ Vdc}$ ) ( $I_C = -2.0 \text{ Adc}, V_{CE} = -2.0 \text{ Vdc}$ )	h <sub>FE</sub>	75 75 75 40		-
Collector–Emitter Saturation Voltages $(I_C = -2.0 \text{ Adc}, I_B = -200 \text{ mAdc})$ $(I_C = -1.0 \text{ Adc}, I_B = -100 \text{ mAdc})$	V <sub>CE(sat)</sub>	-	-0.5 -0.3	Vdc
Base-Emitter Voltages ( $I_C = -1.0 \text{ Adc}, V_{CE} = -2.0 \text{ Vdc}$ )	V <sub>BE(on)</sub>	_	-1.0	Vdc
Base–Emitter Saturation Voltage ( $I_C = -1.0$ Adc, $I_B = -100$ mAdc)	V <sub>BE(sat)</sub>	_	-1.2	Vdc
Current–Gain–Bandwidth ( $I_C = -50$ mAdc, $V_{CE} = -5.0$ Vdc, f = 100 MHz)	f <sub>T</sub>	75	_	MHz

2. Pulse Test: Pulse Width  $\leq$  300 µs, Duty Cycle = 2.0%.

## PZT751

## TYPICAL CHARACTERISTICS

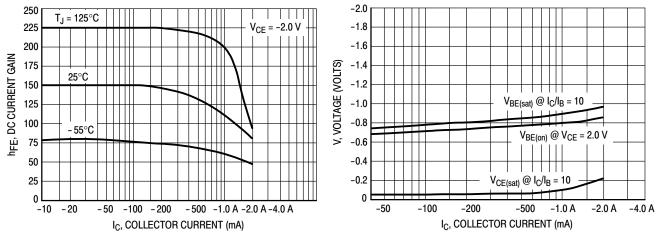


Figure 1. Typical DC Current Gain

Figure 2. On Voltages

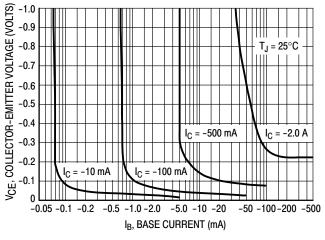
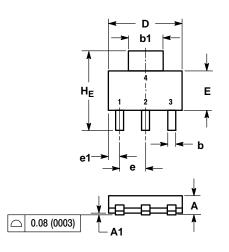


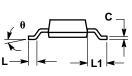
Figure 3. Collector Saturation Region

## PZT751

#### PACKAGE DIMENSIONS

SOT-223 (TO-261) CASE 318E-04 ISSUE N



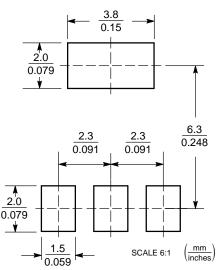


NOTES: 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,

1994 CONTROLLING DIMENSION: INCH MILLIMETERS INCHES DIM MIN NOM MAX MIN NOM MAX 0.060 0.064 0.068 1.50 1.63 A1 0.02 0.06 0.10 0.001 0.002 0.004 0.60 0.89 0.024 0.030 0.035 b 0.75 b1 2.90 3.06 3.20 0.115 0.121 0.126 0.24 0.29 0.35 0.009 0.012 0.014 C D 6.30 6.50 6.70 0.249 0.256 0.263 3.30 3.50 3.70 0.130 0.138 0.145 Е е 2.20 2.30 2.40 0.087 0.091 0.094 e1 0.85 0.94 1.05 0.033 0.037 0.041 0.20 0.008 1.50 1.75 2.00 0.060 0.069 0.078 L1 ΗE 6.70 7.00 7.30 0.264 0.276 0.287 A 09  $10^{\circ}$ 00 10°



#### **SOLDERING FOOTPRINT\***



\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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