

## N-channel 100 V, 0.02 $\Omega$ typ., 32 A STripFET™ F7 Power MOSFET in a DPAK package

Datasheet – production data

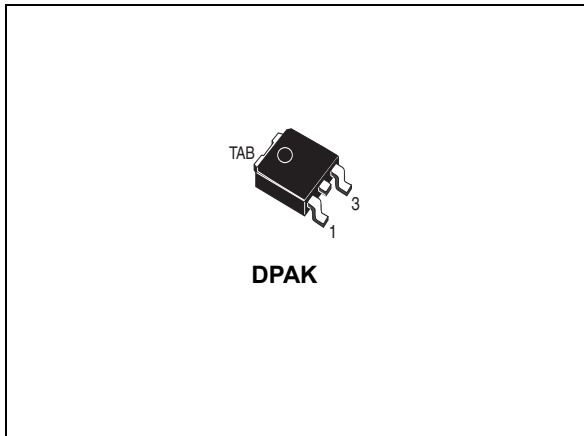
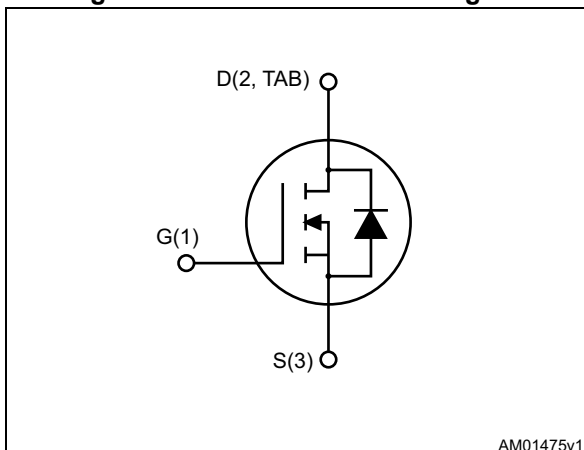


Figure 1. Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>	P <sub>TOT</sub>
STD30N10F7	100 V	0.024 $\Omega$	32 A	50 W

- Among the lowest R<sub>DS(on)</sub> on the market
- Excellent figure of merit (FoM)
- Low C<sub>rss</sub>/C<sub>iss</sub> ratio for EMI immunity
- High avalanche ruggedness

### Applications

- Switching applications

### Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1. Device summary

Order code	Marking	Package	Packing
STD30N10F7	30N10F7	DPAK	Tape and reel

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	100	V
$V_{GS}$	Gate- source voltage	20	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ °C}$	32	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ °C}$	23	A
$I_{DM}^{(1)}$	Drain current (pulsed) $T_C = 25\text{ °C}$	132	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ °C}$	50	W
$T_J$	Operating junction temperature range	-55 to 175	°C
$T_{stg}$	Storage temperature range		

1. Pulse width limited by safe operating area.

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	50	°C/W
$R_{thj-case}$	Thermal resistance junction-case max	3	°C/W

1. When mounted on 1 inch<sup>2</sup> FR-4 board, 2 oz Cu

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 250\ \mu A$	100			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 100\ V$			1	$\mu A$
		$V_{GS} = 0, V_{DS} = 100\ V, T_C = 125\text{ °C}$			100	$\mu A$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0, V_{GS} = +20\ V$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu A$	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on- resistance	$V_{GS} = 10\ V, I_D = 16\ A$		0.02	0.024	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\ V, f = 1\ MHz, V_{GS} = 0$	-	1270	-	pF
$C_{oss}$	Output capacitance		-	290	-	pF
$C_{rss}$	Reverse transfer capacitance		-	24	-	pF
$Q_g$	Total gate charge	$V_{DD} = 50\ V, I_D = 32\ A, V_{GS} = 10\ V$ (see <a href="#">Figure 14</a> )	-	19	-	nC
$Q_{gs}$	Gate-source charge		-	9	-	nC
$Q_{gd}$	Gate-drain charge		-	4.5	-	nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\ V, I_D = 16\ A, R_G = 4.7\ \Omega, V_{GS} = 10\ V$ (see <a href="#">Figure 13</a> )	-	12	-	ns
$t_r$	Rise time		-	17.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	22	-	ns
$t_f$	Fall time		-	5.6	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 32 \text{ A}$ , $V_{GS} = 0$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 32 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 80 \text{ V}$ , $T_J = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 15</a> )	-	41		ns
$Q_{rr}$	Reverse recovery charge		-	47		nC
$I_{RRM}$	Reverse recovery current		-	2.3		A

1. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

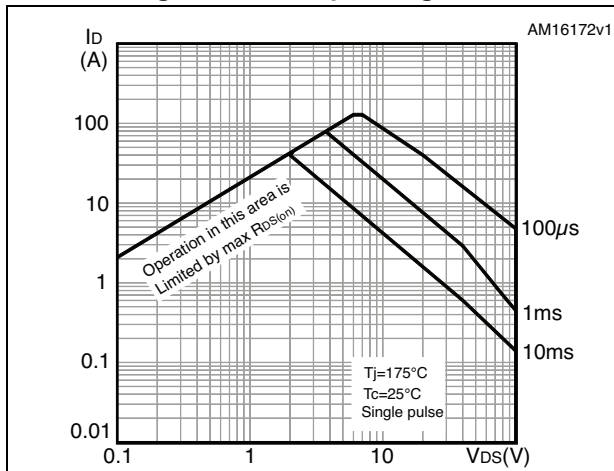


Figure 3. Thermal impedance

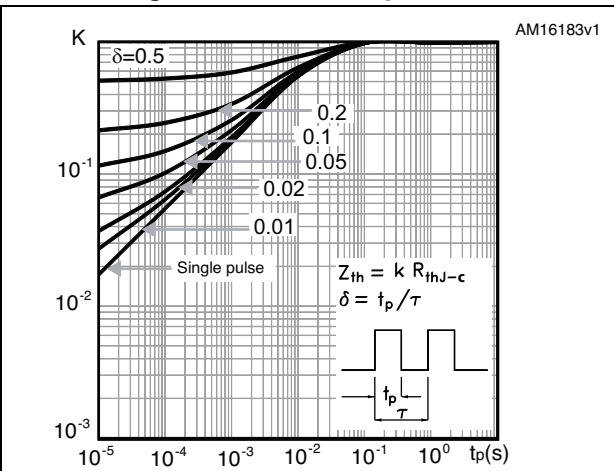


Figure 4. Output characteristics

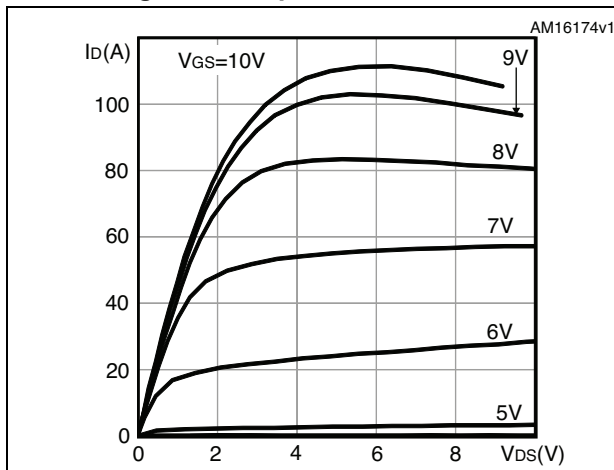


Figure 5. Transfer characteristics

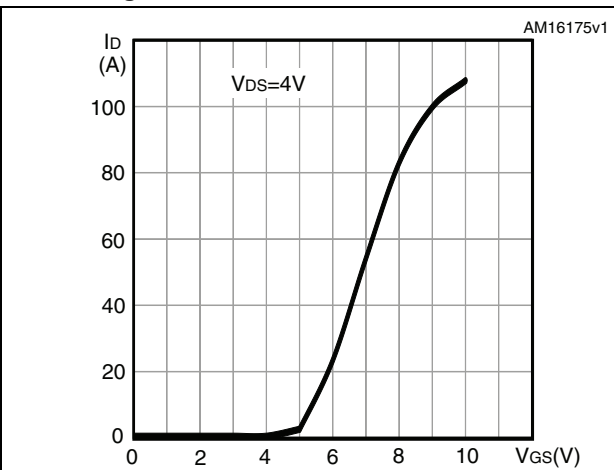


Figure 6. Gate charge vs gate-source voltage

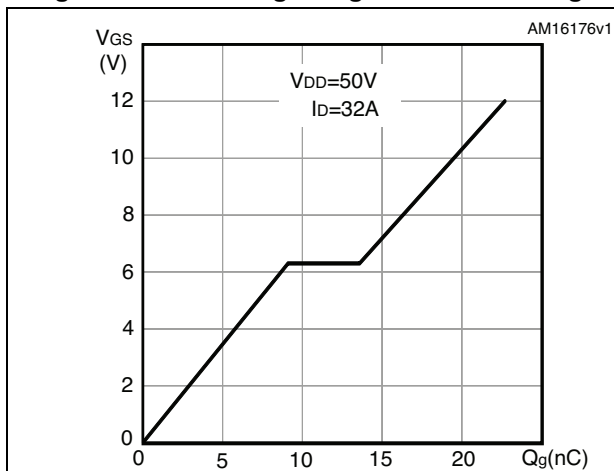


Figure 7. Static drain-source on-resistance

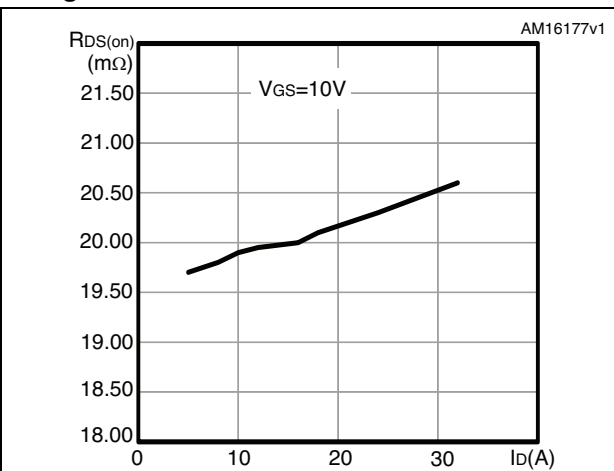


Figure 8. Capacitance variations

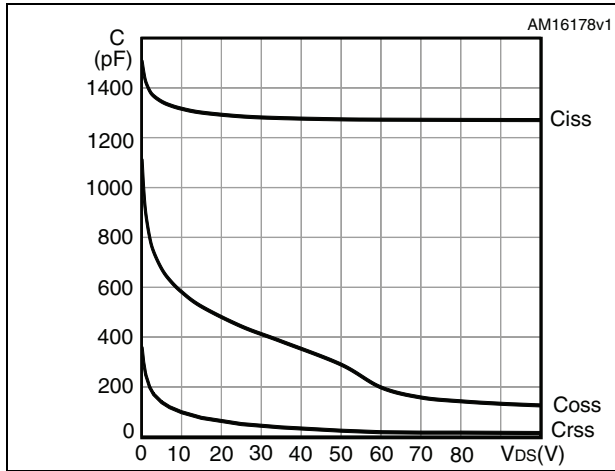


Figure 9. Normalized gate threshold voltage vs temperature

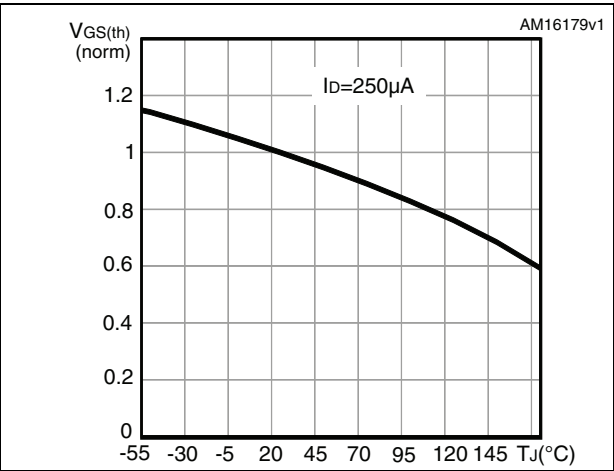


Figure 10. Normalized on-resistance vs temperature

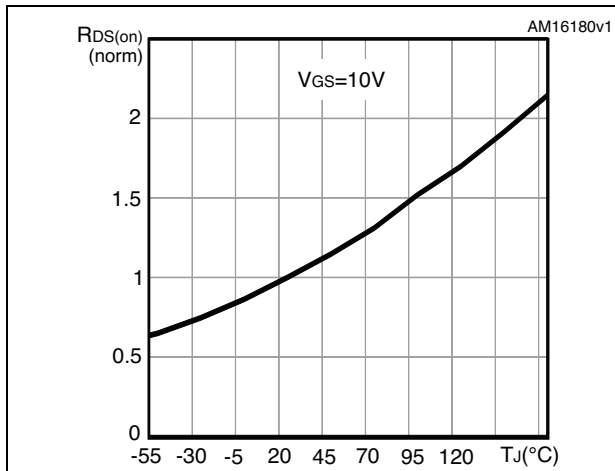


Figure 11. Normalized  $V_{(BR)DSS}$  vs temperature

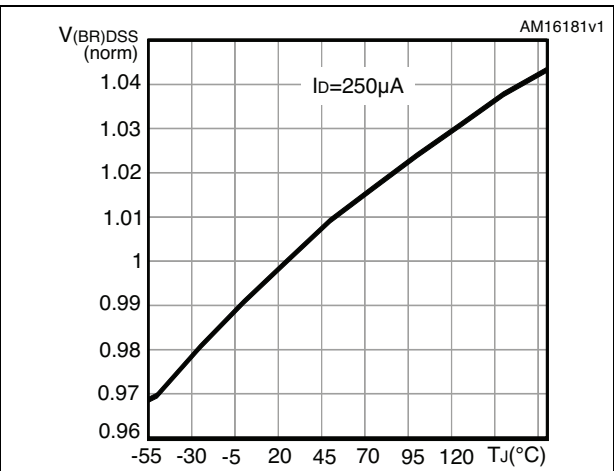
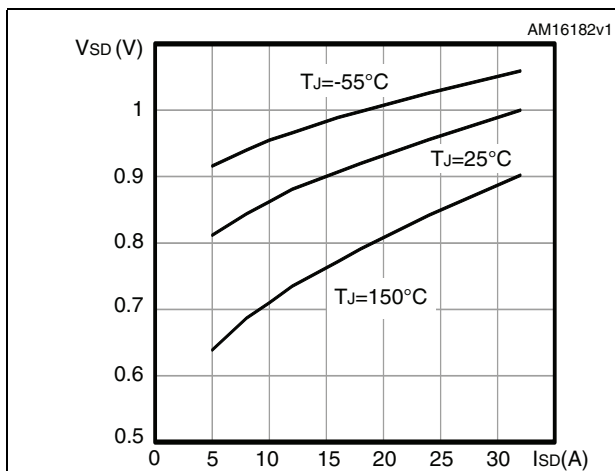
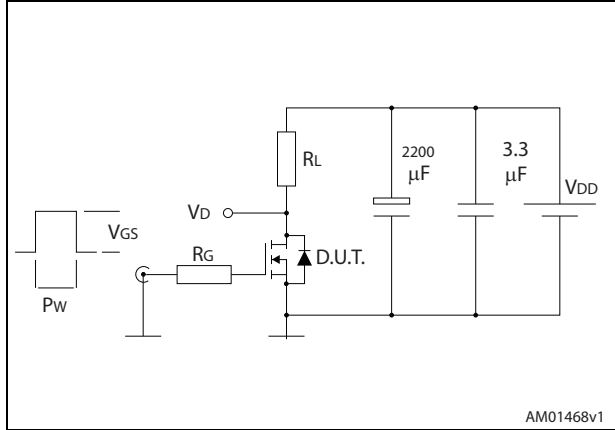


Figure 12. Source-drain diode forward characteristics

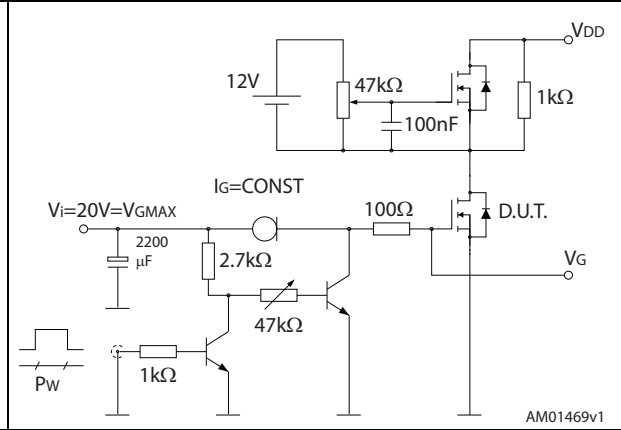


### 3 Test circuits

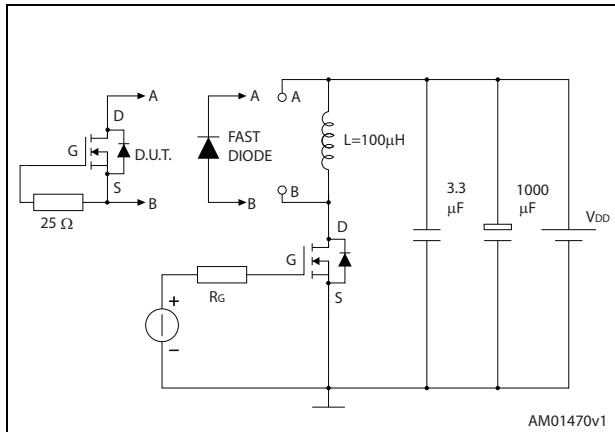
**Figure 13. Switching times test circuit for resistive load**



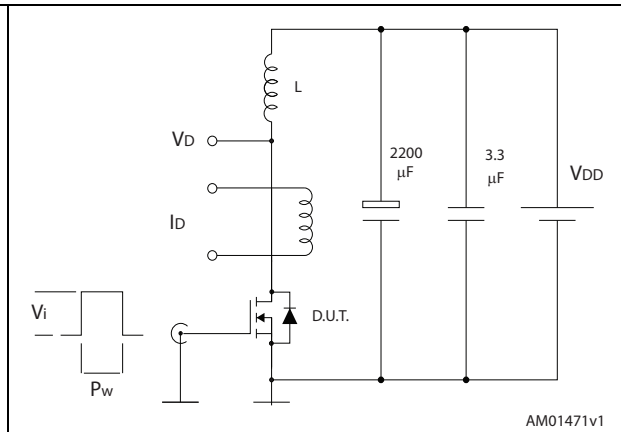
**Figure 14. Gate charge test circuit**



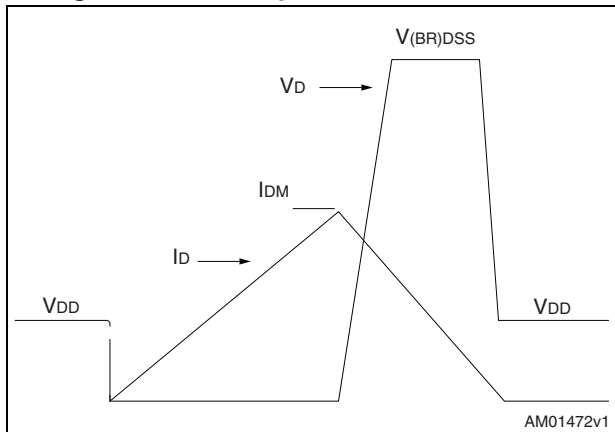
**Figure 15. Test circuit for inductive load switching and diode recovery times**



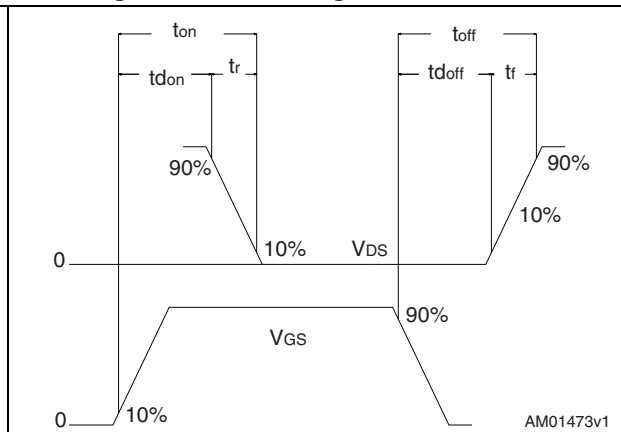
**Figure 16. Unclamped inductive load test circuit**



**Figure 17. Unclamped inductive waveform**



**Figure 18. Switching time waveform**





## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 4.1 DPAK, STD30N10F7

Figure 19. DPAK (TO-252) type A package outline

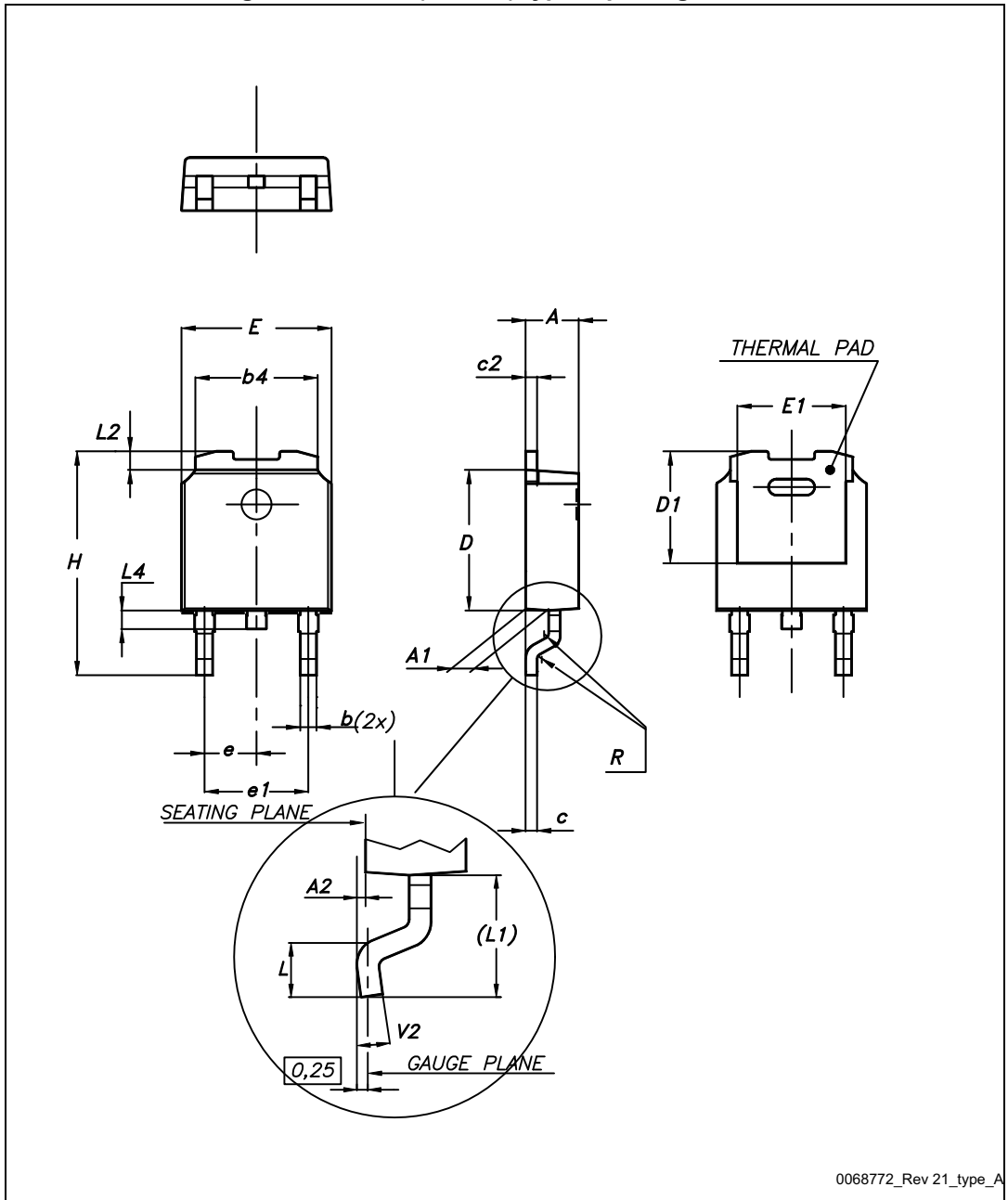
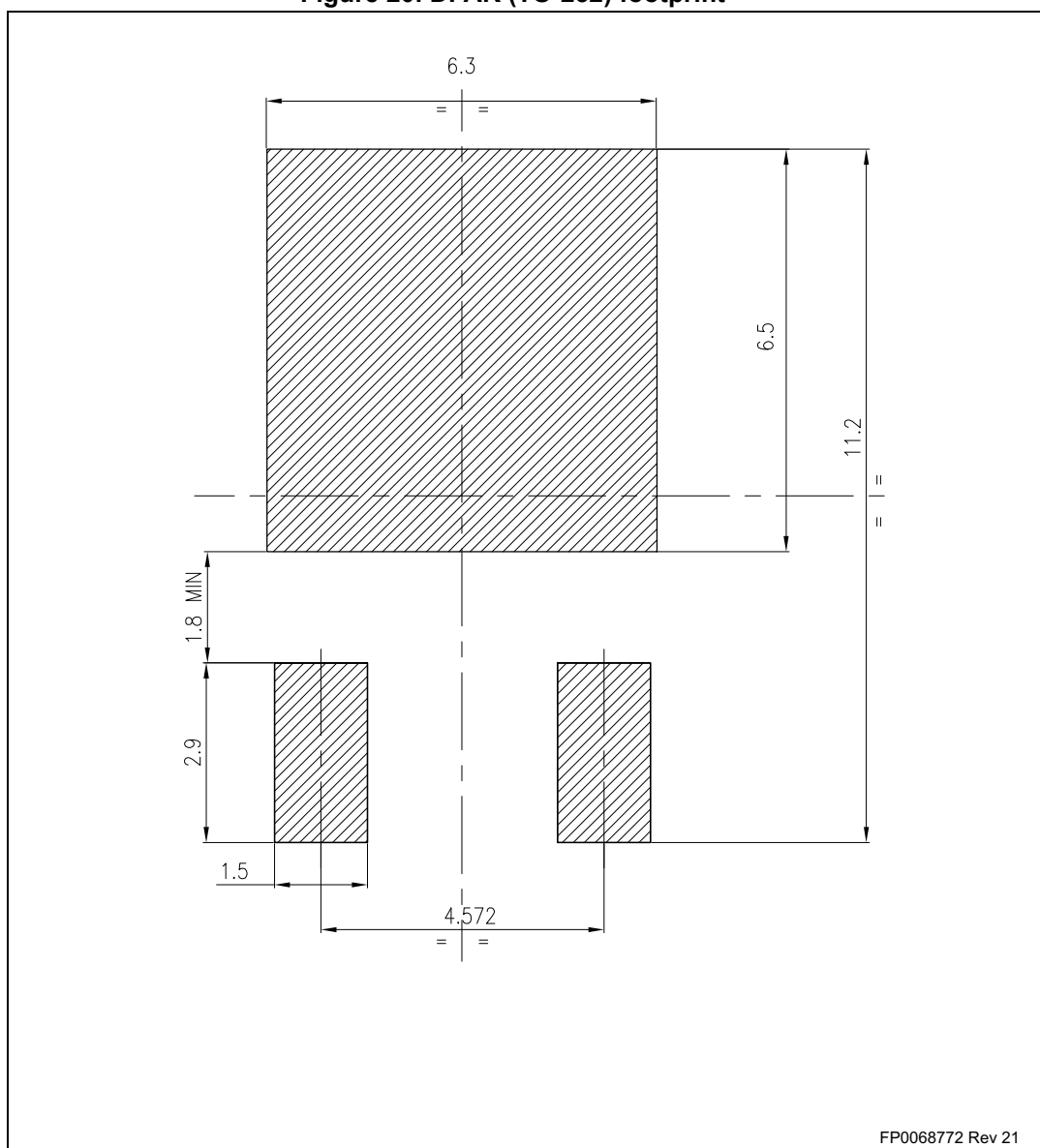


Table 8. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 20. DPAK (TO-252) footprint (a)



a. All dimensions are in millimeters

# 5 Packing information

Figure 21. Tape for DPAK (TO-252)

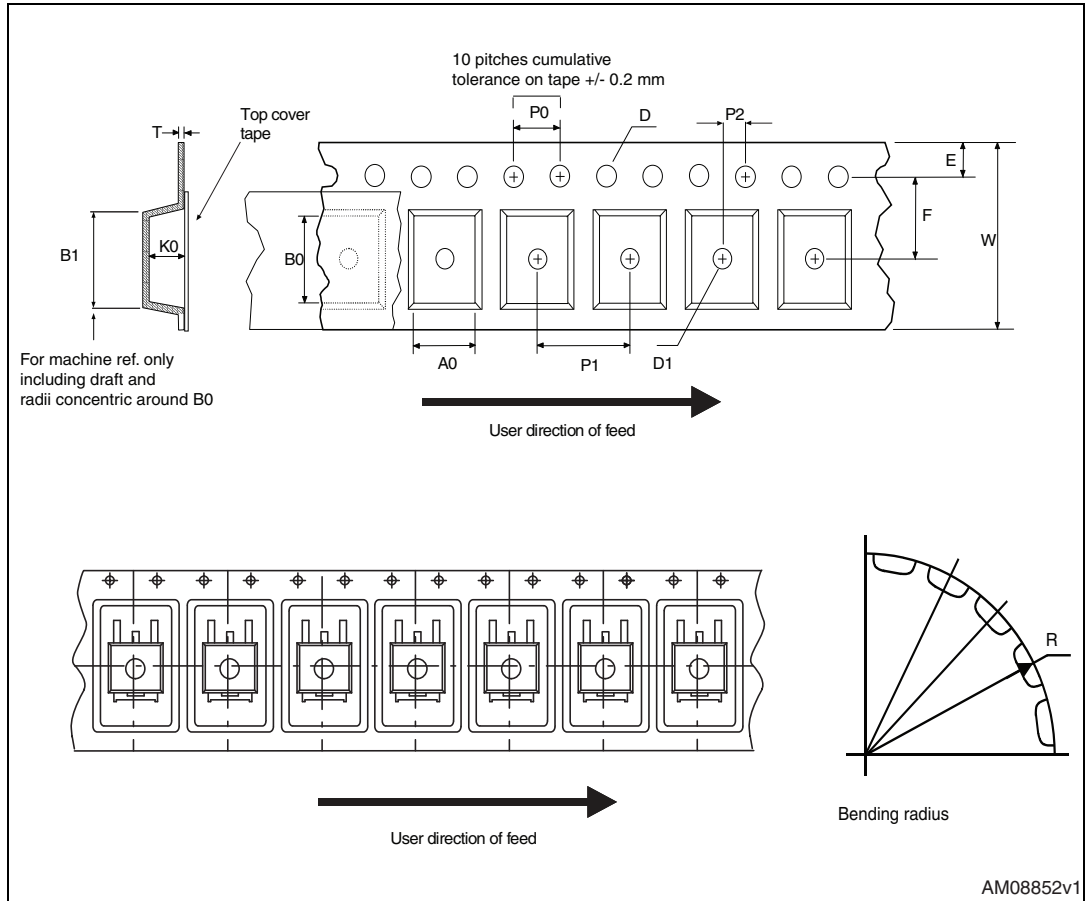


Figure 22. Reel for DPAK (TO-252)

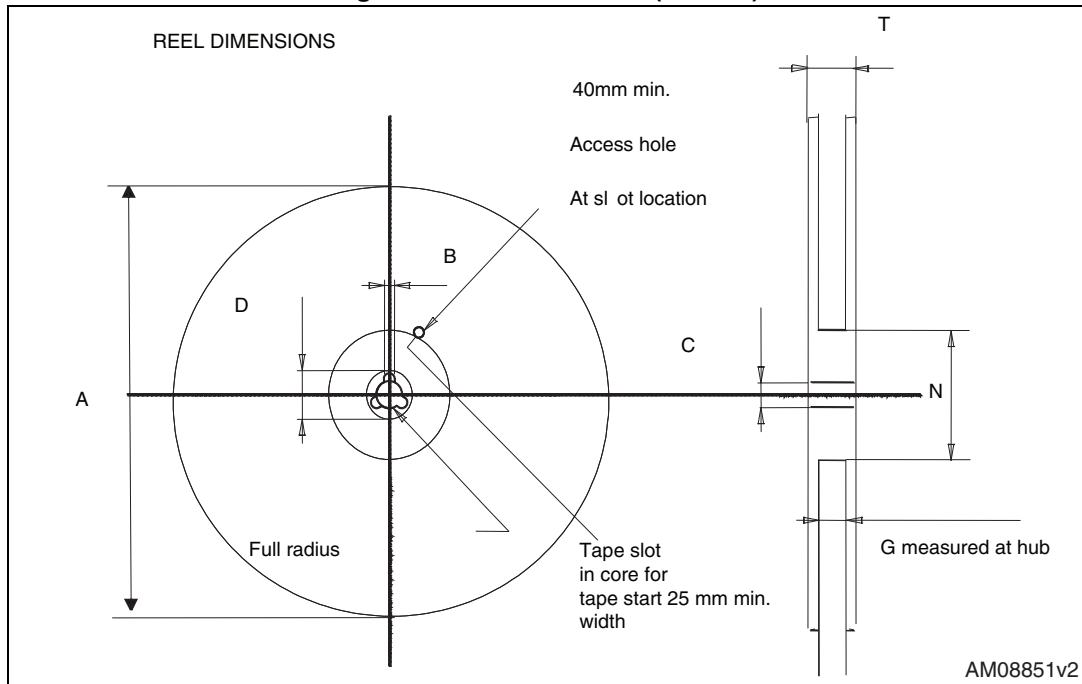


Table 9. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1		Base qty.	2500
P1	7.9	8.1		Bulk qty.	2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## 6 Revision history

Table 10. Document revision history

Date	Revision	Changes
28-Nov-2013	1	First release.
03-Apr-2014	2	<ul style="list-style-type: none"><li>– Updated: Figure 13,14,15 and Figure 16</li><li>– Updated: Section 4.1: DPAK,STD30N10F7</li><li>– Minor text changes.</li></ul>
27-Jan-2016	3	<ul style="list-style-type: none"><li>– Updated title</li><li>– Updated <a href="#">Section 2: Electrical characteristics</a></li><li>– Updated <a href="#">Section 4: Package information</a></li><li>– Minor text changes.</li></ul>

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