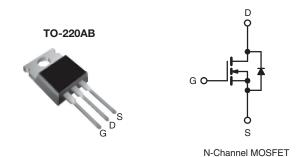


Power MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	60			
R _{DS(on)} (Ω)	V _{GS} = 5.0 V 0.028			
Q _g (Max.) (nC)	66			
Q _{gs} (nC)	12			
Q _{gd} (nC)	43			
Configuration	Single			



FEATURES

- Dynamic dV/dt Rating
- · Logic-Level Gate Drive
- R_{DS(on)} Specified at V_{GS} = 4 V and 5 V
- 175 °C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Load (Dh) fros	IRLZ44PbF
Lead (Pb)-free	SiHLZ44-E3
SnPb	IRLZ44
SIFD	SiHLZ44

ABSOLUTE MAXIMUM RATINGS (TC	= 25 °C, unl	ess otherwis	se noted)			
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V_{DS}	60	V	
Gate-Source Voltage			V_{GS}	± 10	V	
Continuous Drain Currente	\/ at F.O.\/	$T_{\rm C} = 25 ^{\circ}{\rm C}$ $T_{\rm C} = 100 ^{\circ}{\rm C}$	1	50		
Continuous Drain Current	V _{GS} at 5.0 V	T _C = 100 °C	I _D	36	Α	
Pulsed Drain Current ^a		I _{DM}	200	1		
Linear Derating Factor			1.0	W/°C		
Single Pulse Avalanche Energy ^b			E _{AS}	400	mJ	
Maximum Power Dissipation $T_C = 25 ^{\circ}C$		P _D	150	W		
Peak Diode Recovery dV/dt ^c			dV/dt	4.5	V/ns	
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 175	°C	
Soldering Recommendations (Peak Temperature)d	nperature) ^d for 10 s			300]	
Mounting Torque	6-32 or M3 screw			10	lbf ⋅ in	
Mounting Torque				1.1	N · m	

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. $V_{DD} = 25 \text{ V}$, starting $T_J = 25 \,^{\circ}\text{C}$, $L = 179 \, \mu\text{H}$, $R_g = 25 \, \Omega$, $I_{AS} = 51 \, \text{A}$ (see fig. 12). c. $I_{SD} \le 51 \, \text{A}$, $dV/dt \le 250 \, \text{A/s}$, $V_{DD} \le V_{DS}$, $T_J \le 175 \,^{\circ}\text{C}$.
- d. 1.6 mm from case.
- e. Current limited by the package, (die current = 51 A).

^{*} Pb containing terminations are not RoHS compliant, exemptions may apply



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R _{thJA}	-	62	
Case-to-Sink, Flat, Greased Surface	R _{thCS}	0.50	-	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	-	1.0	

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static		1			·		ı
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0	V, I _D = 250 μA	60	_	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference t	o 25 °C, I _D = 1 mA	-	0.070	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{c}$	_{GS} , I _D = 250 μA	1.0	-	2.0	V
Gate-Source Leakage	I _{GSS}	Vo	_{GS} = 10 V	-	-	± 100	nA
Zero Osto Vellere Burio Oscort	I _{DSS}	$V_{DS} = 6$	V _{DS} = 60 V, V _{GS} = 0 V		-	25	
Zero Gate Voltage Drain Current		$V_{DS} = 48 \text{ V}, V_{0}$	_{GS} = 0 V, T _J = 150 °C	-	-	250	μA
Duein Course On Otata Basistana	Б	V _{GS} = 5.0 V	I _D = 31 A ^b	-	-	0.028	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 4.0 V	I _D = 25 A ^b	-	-	0.039	Ω
Forward Transconductance	9fs	V _{DS} = 2	5 V, I _D = 31 A ^b	23	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V	_{GS} = 0 V,	-	3300	-	
Output Capacitance	C _{oss}	V _C	$_{0S} = 25 \text{ V},$	-	1200	-	pF
Reverse Transfer Capacitance	C _{rss}	f = 1.0 f	MHz, see fig. 5	-	200	-	
Total Gate Charge	Q_g			-	-	66	
Gate-Source Charge	Q _{gs}	V _{GS} = 5.0 V	$I_D = 51 \text{ A}, V_{DS} = 48 \text{ V},$ see fig. 6 and 13 ^b	=	-	12	nC
Gate-Drain Charge	Q_{gd}			-	-	43]
Turn-On Delay Time	t _{d(on)}			-	17	-	
Rise Time	t _r	V_{DD} = 30 V, I_{D} = 51 A, R_{g} = 4.6 Ω, R_{D} = 0.56 Ω, see fig. 10 ^b		-	230	-	ns
Turn-Off Delay Time	t _{d(off)}			-	42	-	
Fall Time	t _f			=	110	-	
Internal Drain Inductance	L_{D}	Between lead, 6 mm (0.25") from		-	4.5	-	ъЦ
Internal Source Inductance	L _S	package and cei die contact	nter of	-	7.5	-	- nH
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I _S	MOSFET symbo		-	-	50°	Α
Pulsed Diode Forward Current ^a	I _{SM}	integral reverse p - n junction diode		200			
Body Diode Voltage	V_{SD}	T _J = 25 °C, I _S	$_{S} = 51 \text{ A}, V_{GS} = 0 \text{ V}^{b}$	-	-	2.5	V
Body Diode Reverse Recovery Time	t _{rr}	T 25 °C 1	E1 A dl/dt = 100 A/h	-	130	180	ns
Body Diode Reverse Recovery Charge	Q _{rr}	IJ = 25 ⁻ U, I _F = 1	51 A, dl/dt = 100 A/μs ^b	-	0.84	1.3	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-or			minated b	y L _S and	L _D)

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width \leq 300 μ s; duty cycle \leq 2 %.
- c. Current limited by the package, (die current = 51 A).



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

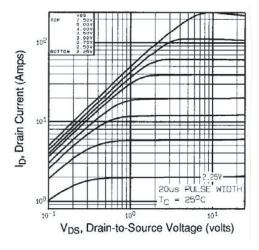


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

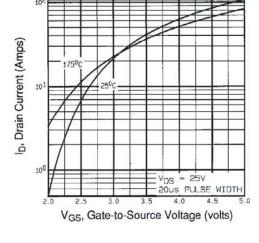


Fig. 3 - Typical Transfer Characteristics

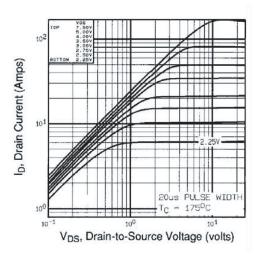


Fig. 2 - Typical Output Characteristics, T_C = 175 °C

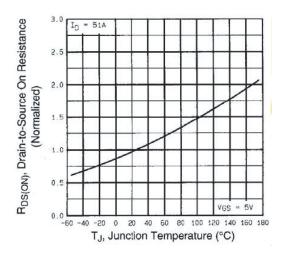


Fig. 4 - Normalized On-Resistance vs. Temperature



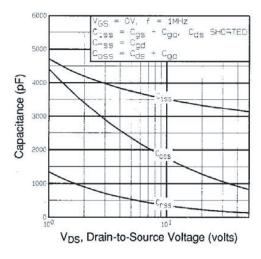


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

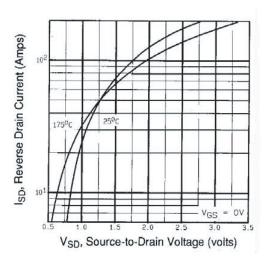


Fig. 7 - Typical Source-Drain Diode Forward Voltage

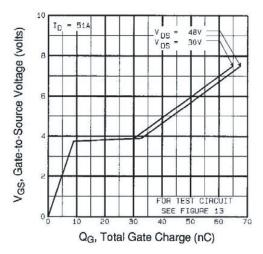


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

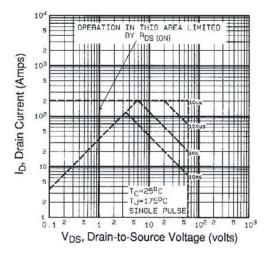


Fig. 8 - Maximum Safe Operating Area





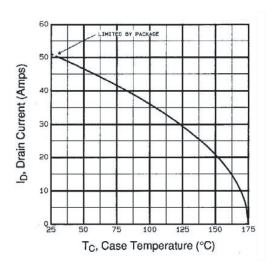


Fig. 9 - Maximum Drain Current vs. Case Temperature

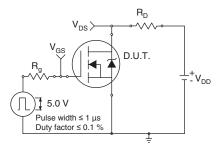


Fig. 10a - Switching Time Test Circuit

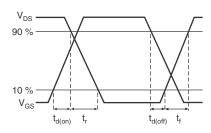


Fig. 10b - Switching Time Waveforms

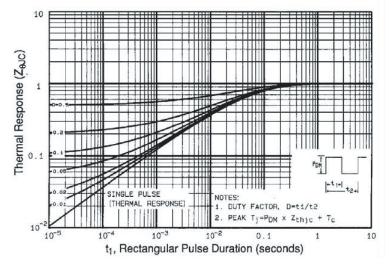
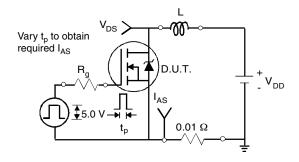


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case





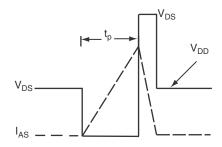


Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

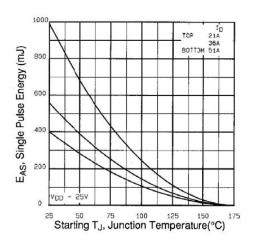


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

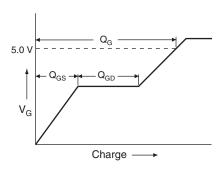


Fig. 13a - Basic Gate Charge Waveform

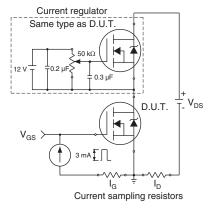
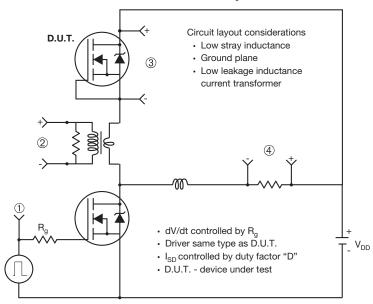


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



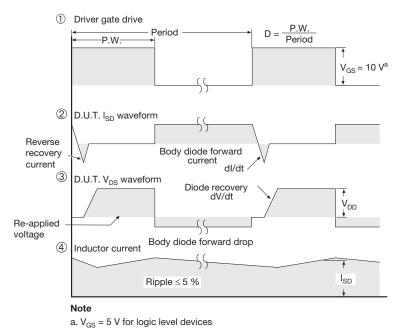


Fig. 14 - For N-Channel

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TO-220-1



DIM.	MILLIN	METERS	INCHES		
	MIN.	MAX.	MIN.	MAX.	
Α	4.24	4.65	0.167	0.183	
b	0.69	1.02	0.027	0.040	
b(1)	1.14	1.78	0.045	0.070	
С	0.36	0.61	0.014	0.024	
D	14.33	15.85	0.564	0.624	
Е	9.96	10.52	0.392	0.414	
е	2.41	2.67	0.095	0.105	
e(1)	4.88	5.28	0.192	0.208	
F	1.14	1.40	0.045	0.055	
H(1)	6.10	6.71	0.240	0.264	
J(1)	2.41	2.92	0.095	0.115	
L	13.36	14.40	0.526	0.567	
L(1)	3.33	4.04	0.131	0.159	
ØР	3.53	3.94	0.139	0.155	
Q	2.54	3.00	0.100	0.118	

Note

 \bullet $M^{\star}=0.052$ inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM



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