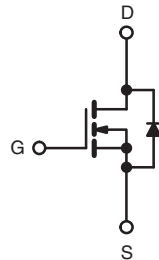
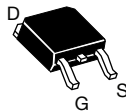


## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	50	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V	0.20
$Q_g$ (Max.) (nC)	10	
$Q_{gs}$ (nC)	2.6	
$Q_{gd}$ (nC)	4.8	
Configuration	Single	

**DPAK  
(TO-252)**


N-Channel MOSFET

### FEATURES

- Low Drive Current
- Surface Mount
- Fast Switching
- Ease of Paralleling
- Excellent Temperature Stability
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS  
COMPLIANT**

### DESCRIPTION

The power MOSFET technology is the key to Vishay's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery  $dV/dt$  capability.

The power MOSFET transistors also feature all of the well established advantages of MOSFET'S such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

Surface mount packages enhance circuit performance by reducing stray inductances and capacitance. The DPAK (TO-252) surface mount package brings the advantages of power MOSFET's to high volume applications where PC Board surface mounting is desirable. The surface mount option IRFR9012, SiHFR9012 is provided on 16 mm tape. The straight lead option IRFU9012, SiHFU9012 of the device is called the IPAK (TO-251).

They are well suited for applications where limited heat dissipation is required such as, computers and peripherals, telecommunication equipment, dc-to-dc converters, and a wide range of consumer products.

ORDERING INFORMATION	
Package	DPAK (TO-252)
Lead (Pb)-free	IRFR010PbF
	SiHFR010-E3

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		$V_{DS}$	50	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current	$V_{GS}$ at 10 V	$I_D$	$T_C = 25$ °C	8.2
			$T_C = 100$ °C	5.2
Pulsed Drain Current <sup>a</sup>		$I_{DM}$	33	A
Avalanche Current <sup>b</sup>		$I_{AS}$	1.5	
Linear Derating Factor			0.20	W/°C
Maximum Power Dissipation	$T_C = 25$ °C	$P_D$	25	W
Peak Diode Recovery $dV/dt$ <sup>c</sup>		$dV/dt$	2.0	V/ns
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature) <sup>d</sup>	for 10 s		300	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25$  V, starting  $T_J = 25$  °C,  $L = 100$   $\mu$ H,  $R_g = 25$   $\Omega$ .
- $I_{SD} \leq 8.2$  A,  $di/dt \leq 130$  A/ $\mu$ s,  $V_{DD} \leq 40$  V,  $T_J \leq 150$  °C.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).



THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	$R_{thJA}$	-	-	110	°C/W	
Case-to-Sink	$R_{thCS}$	-	1.7	-		
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	-	5.0		

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		50	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 500$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		-	-	250	$\mu\text{A}$
		$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	1000	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 4.6\text{ A}^b$	-	0.16	0.20	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} \geq 50\text{ V}, I_D = 3.6\text{ A}$		2.1	3.1	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz, see fig. 10}$		-	250	-	$\mu\text{F}$
Output Capacitance	$C_{oss}$			-	150	-	
Reverse Transfer Capacitance	$C_{rss}$			-	29	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 7.3\text{ A}, V_{DS} = 40\text{ V},$ see fig. 6 and 13 <sup>b</sup>	-	6.7	10	nC
Gate-Source Charge	$Q_{gs}$			-	1.8	2.6	
Gate-Drain Charge	$Q_{gd}$			-	3.2	4.8	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 25\text{ V}, I_D = 7.3\text{ A}, R_g = 24\text{ }\Omega, R_D = 3.3\text{ }\Omega,$ see fig. 10 <sup>b</sup>		-	11	17	ns
Rise Time	$t_r$			-	33	50	
Turn-Off Delay Time	$t_{d(off)}$			-	12	18	
Fall Time	$t_f$			-	23	35	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact <sup>c</sup>		-	4.5	-	nH
Internal Source Inductance	$L_S$			-	7.5	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	8.2	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	33	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 8.2\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.6	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 7.3\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$		41	86	190	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			0.15	0.33	0.78	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

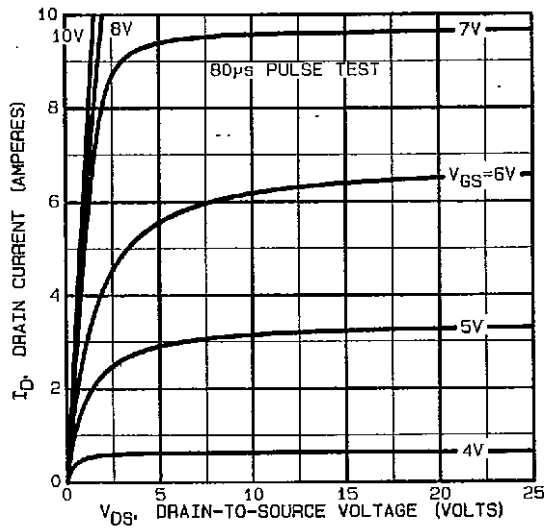


Fig. 1 - Typical Output Characteristics

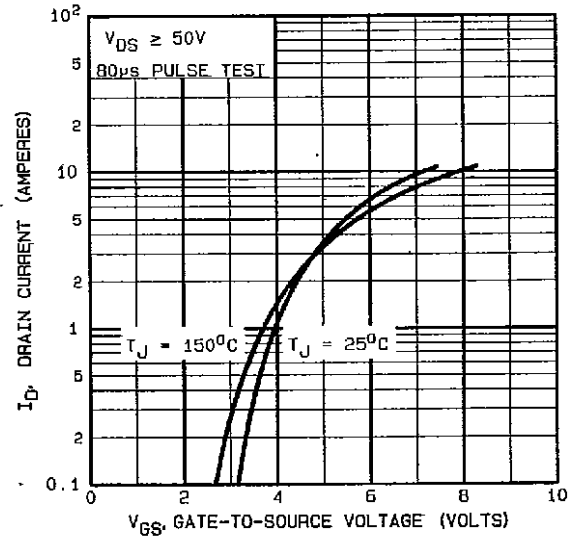


Fig. 3 - Typical Transfer Characteristics

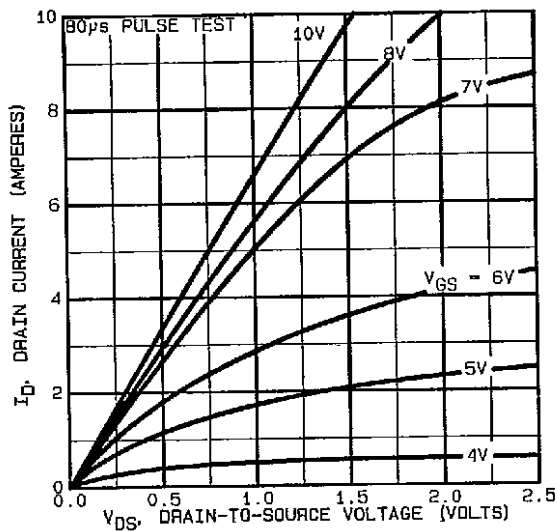


Fig. 2 - Typical Output Characteristics

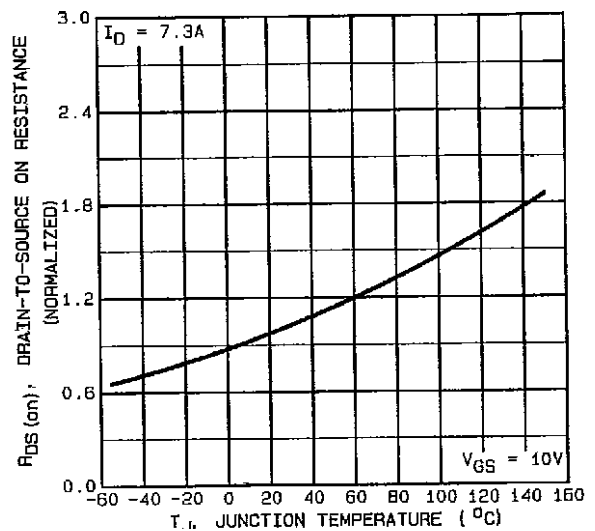


Fig. 4 - Normalized On-Resistance vs. Temperature

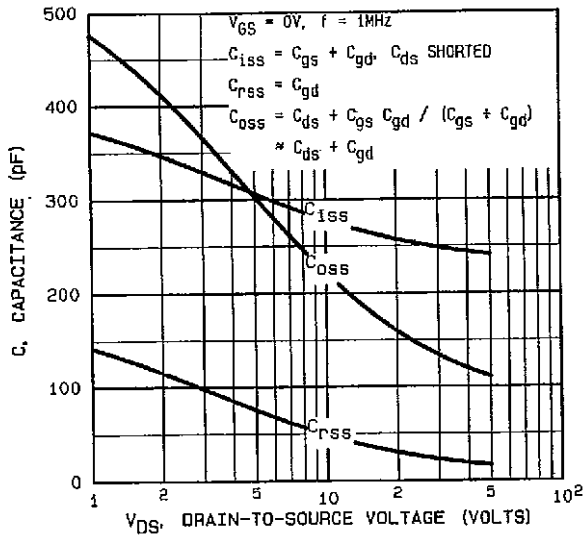


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

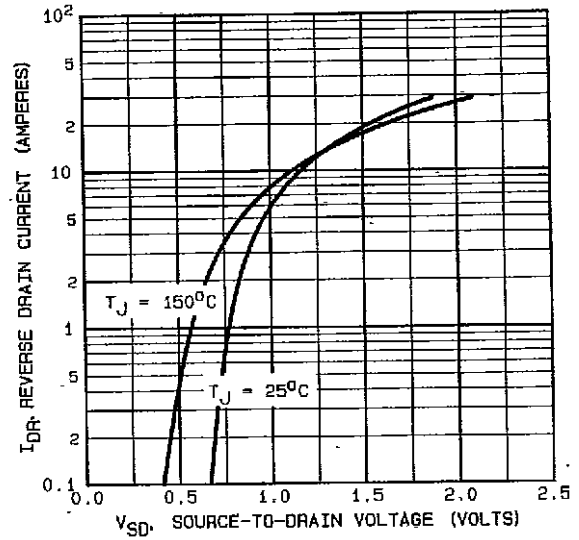


Fig. 7 - Typical Source-Drain Diode Forward Voltage

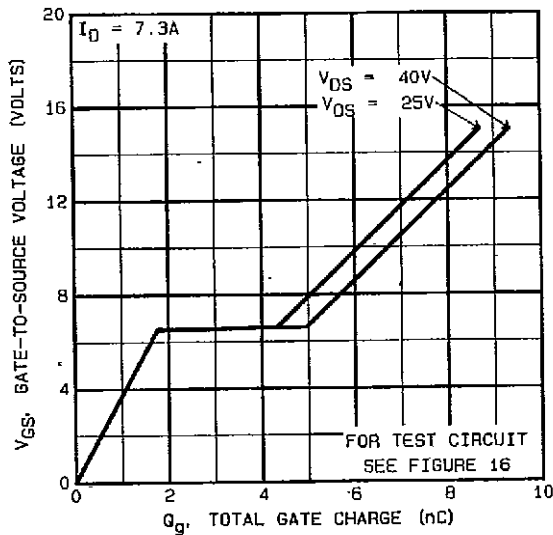


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

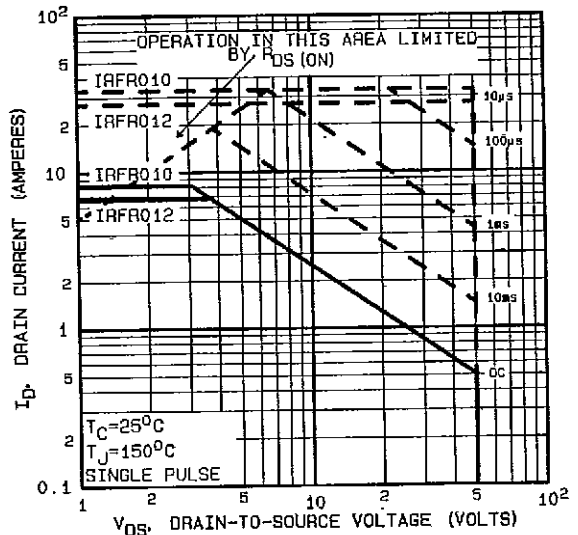


Fig. 8 - Maximum Safe Operating Area

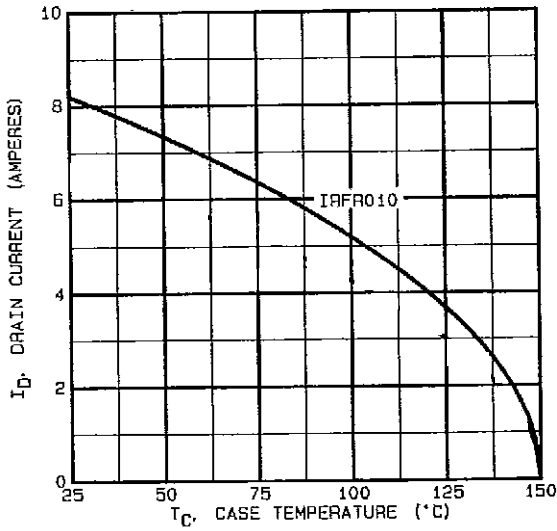


Fig. 9 - Maximum Drain Current vs. Case Temperature

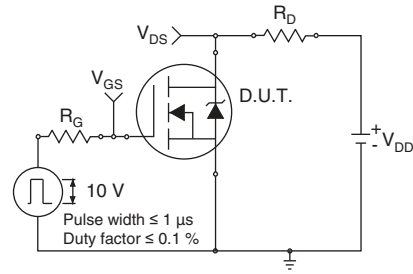


Fig. 10a - Switching Time Test Circuit

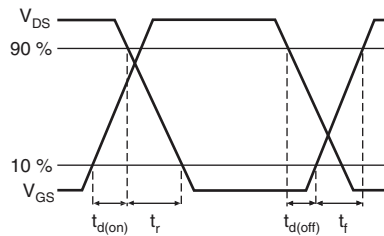


Fig. 10b - Switching Time Waveforms

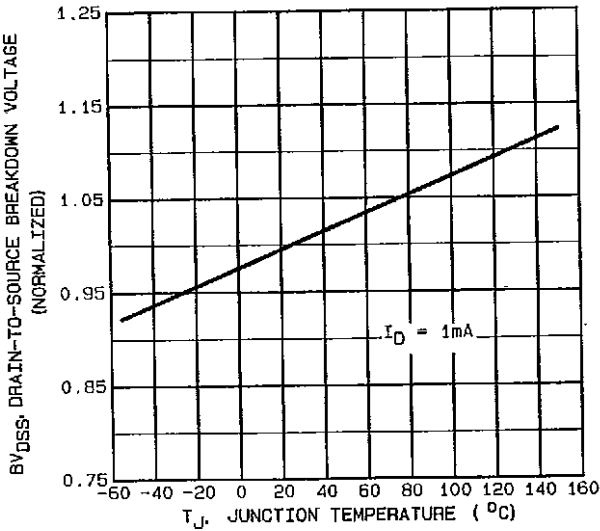


Fig. 10 - Breakdown Voltage vs. Temperature

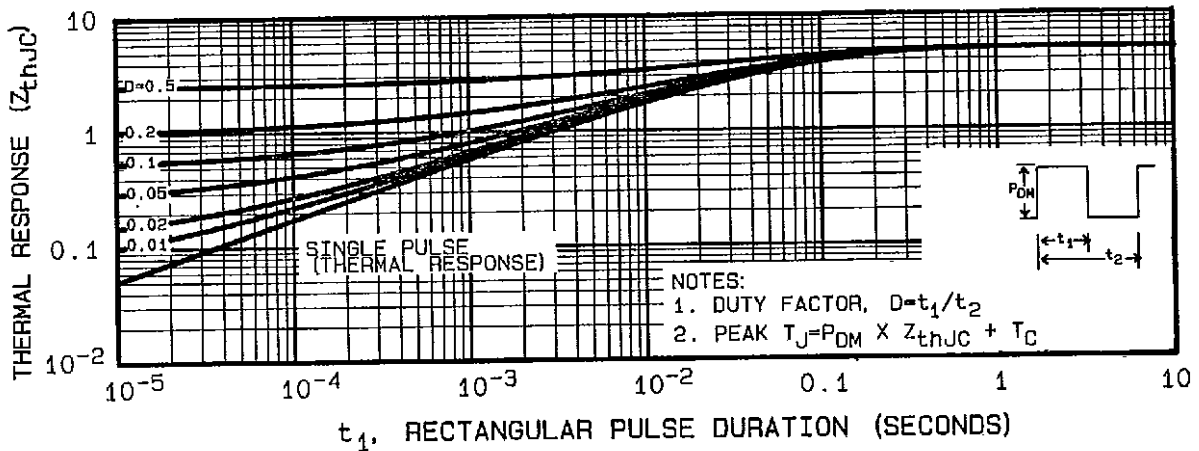


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

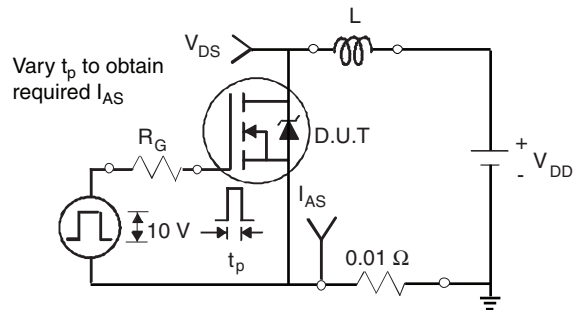


Fig. 12a - Unclamped Inductive Test Circuit

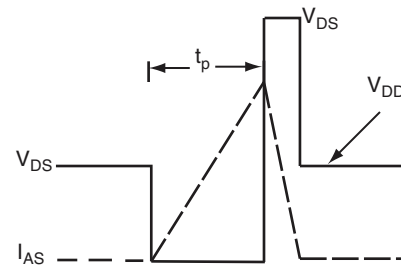


Fig. 12b - Unclamped Inductive Waveforms

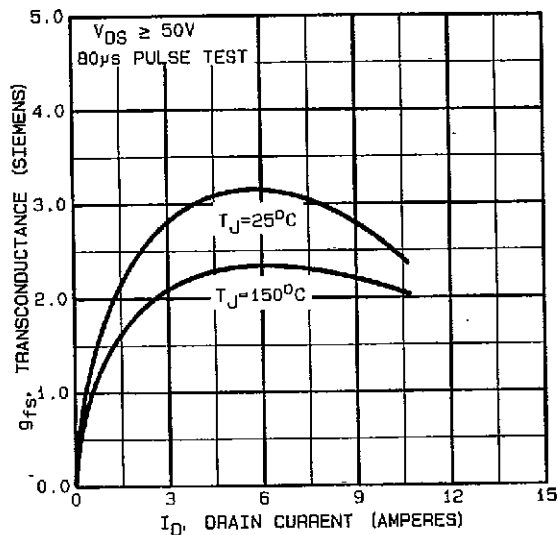


Fig. 12c - Typical Transconductance vs. Drain Current

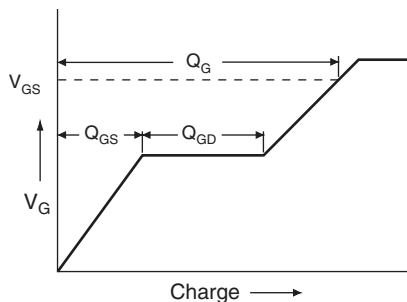


Fig. 13a - Basic Gate Charge Waveform

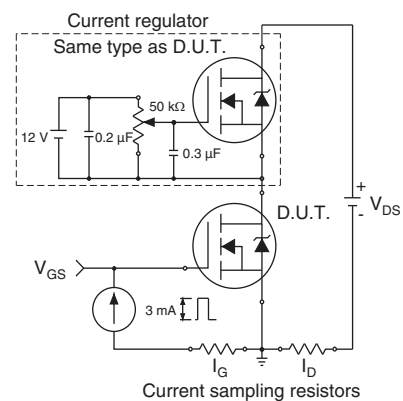
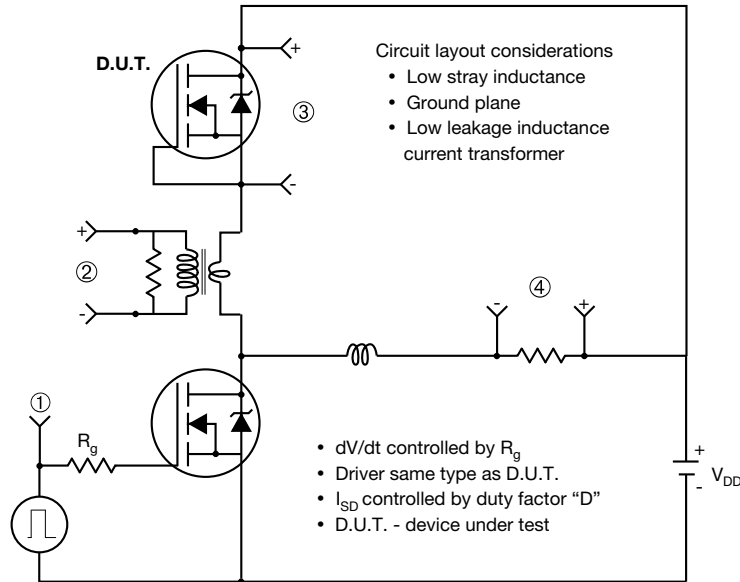


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a.  $V_{GS} = 5\text{ V}$  for logic level devices

Fig. 14 - For N-Channel

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### TO-252AA Case Outline



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T16-0236-Rev. P, 16-May-16 DWG: 5347				

**Notes**

- Dimension L3 is for reference only.



## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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